Final Report

Cooperative Agreement: NAG4-210
Glenn Research Center

"Mitigation of High Altitude and Low Earth Orbit Radiation Effects on Microelectronics via Shielding or Error Detection and Correction Systems"

FY 2000 Faculty Awards for Research (FAR)

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I. Background

The NASA Cooperative Agreement NAG4-210 was granted under the FY2000 Faculty Awards for Research (FAR) Program. The project was proposed to examine the effects of charged particles and neutrons on selected random access memory (RAM) technologies. The concept of the project was to add to the current knowledge of Single Event Effects (SEE) concerning RAM and explore the impact of selected forms of radiation on Error Detection and Correction Systems.

The project was established as an extension of a previous FAR awarded to Prairie View A&M University (PVAMU), under the direction of Dr. Richard Wilkins as principal investigator. The NASA sponsored Center for Applied Radiation Research (CARR) at PVAMU developed an electronic test-bed to explore and quantify SEE on RAM from charged particles and neutrons. The test-bed was developed using 486DX microprocessor technology (PC-104) and a custom test board to mount RAM integrated circuits or other electronic devices. The test-bed had two configurations – a bench test version for laboratory experiments and a 400 Hz powered rack version for flight experiments. The objectives of this project were to:

1. Upgrade the Electronic Test-bed (ETB) to a Pentium configuration
2. Accommodate more than only 8 Mbytes of RAM
3. Explore Error Detection and Correction Systems for radiation effects
4. Test modern RAM technologies in radiation environments

II. Technical Approach

The technical approach to the project was divided into three components; (1) Update of hardware and software, (2) Integration of recent SRAM technologies and (3) Exploration of Error Detection and Correction. Each project component is described in more detail in the Appendences A, B and C, respectively. A brief description of the activities and accomplishments of each component is provided below. A full discussion is provided at the appendences.

A. Update of Hardware and Software

The first effort was to seek a Pentium configuration for the ETB. Appendix A is the documented approach to the updated ETB. The project report of master degree student, Kevin Brewer, documents this project component. Please refer to the appendix for details.

B. Integration of Recent SRAM Technologies

As a technical solution, it was recommended that the SRAM memory cards be used as an alternative memory test solution for single event effects testing. Appendix A proposes 8 Mbytes SRAM cards based on the conditions that each card is 8 Mbytes and has a self-contained battery for storage life up to six months. Although the 8 Mbytes cards were proposed, the 8 Mbytes cards were not available and very costly. Thus the 6 Mbytes SRAM cards were purchased for testing. Preliminary testing at the Los Alamos (Neutrons) facility revealed the following results:

(1) The cards were not affected at all by the neutrons
(2) There was evidence that some memory locations were changed
(3) Some cards were non-operational after exposure to the neutron beam line

These preliminary results were reviewed and it was determined that our design of experiment was not appropriate to actually characterize the response of the SRAM cards. We could determine that the neutrons had an effect on the memory cards; however, we were not able to describe in detail what and how the effect occurred.

C. Exploration of Error Detection and Correction

The exploration of Error Detection and Correction was an exhaustive search to determine if error detection and correction algorithms were feasible to consider in radiation effects applications. The research considered the use of fuzzy logic control systems to aid possible Error Detection and Correction algorithms. The research revealed the following:

(1) Error Detection and Correction (EDC) implementations in electronic and memory systems is proprietary, which limits access to problem solutions
(2) EDC algorithms are public information, although the implementation method is desired to truly analyze the efficiency and application of the implementation to radiation effects
(3) The concepts of error correction and fuzzy logic control systems were examined for possible implementations in the radiation effects environments.

Appendix C presents the approach and more detailed analyses of problems and conclusions. The EDC implementations will continue to be explored in memory systems as applicable to radiation effects. The EDC concept in data communications is very complex and well documented throughout technical literature. The concept of correcting memory bit flips from radiation induced energy will be further explored with other techniques.

III. Designs and Experiments

The activities of this project revealed that the design of each experiment is very critical concerning radiation effects. Bit changes in memory cells can result from several sources. The ability to determine the time and source of the change is critical to determine how to protect the memory system from the radiation threat. We are currently redesigning our approach to radiation induced effects on memory systems with the augmentation of radiation dosimetry. We are designing experiments to characterize radiation particles through active radiation dosimetry, in conjunction with SEE analyses on memory systems. Proportional Counters will be utilized to characterize the radiation particles which may impact the memory systems.

In addition, we are consulting with the manufacturers of the SRAM cards and the software developers in efforts to access the cards by memory locations. Current access to the cards is limited to the standard disc drive capabilities. Since the card functions as an independent disc drive with a self-contained power source, we require additional information to access the SRAM card as a continuous storage space. We are seeking to access the memory cards through locally

developed programs, which will identify specific memory locations and times of SEE or bit changes. Such information, in conjunction with dosimetry data, will better characterize the SEE on RAM.

Follow-on experiments will be conducted within laboratories of controlled radiation sources. The SRAM cards will be tested with Proportional Counters to characterize the radiation exposure. The combined experiment will help characterize SEE within RAM systems. After the experiments in the laboratories are conducted, the combined experiment will be flown aboard the ER-2 Aircraft and gas balloons for high altitude experiments. The preliminary design of the SRAM System 20 Pod is provided at Appendix B.

IV. Results and Conclusions

A. Personnel: The FAR project has been very vital to the development and experience of the principal investigator. In addition, several other persons have contributed to the development and results of the project:
    (1) Dr. Earl Smith: Recent PhD recipient developed report on Error Correction, Control Systems and Fuzzy Logic.
    (2) Mr. Harold Huff: Staff Engineer to assist with radiation tests at Los Alamos
    (3) Mr. Kevin Brewer: Master degree student in Electrical Engineering to implement hardware update
    (4) Mr. Justin Voros: Undergraduate Computer Science major assisted in the development of the software upgrade
    (5) Mr. Noah Rattler: System 20 Pod Design for SRAM Cards
    (6) Mr. Frederick Tompkins: Master degree candidate assisted on hardware and software upgrade reviews
    (7) Ms. Monica Bibbs: Master degree candidate assisted with hardware upgrades

B. Equipment: The project will maintain the 6 Mbytes SRAM cards for follow-on experiments within laboratory facilities, experimental aircraft and gas balloons.
C. Budget: The project has ended and the budget has approximately $4,000.00, which will not be expended. It is expected that NASA will reduce or retract the funds remaining as non-committed.

V. Future Work

Much of the future work has been mentioned. This project was instrumental in conducting research to help personnel resources at PVAMU develop knowledge and skills associated with radiation and SEE. The follow-on work will be funded or piggy-back other radiation dosimetry experiments supported by other sources. The follow-on activities include the following:

(1) Developing joint experiments which include dosimetry devices – proportional counters.
(2) Gaining total access and control of the SRAM cards for detailed programming.
(3) Designing experiments within laboratories, experimental aircraft and gas balloons.

Appendix A

Updated Electronic Test-bed System

UPDATED ELECTRONIC TESTBED SYSTEM

by

KEVIN L. BREWER

A paper submitted to the Center for Applied Radiation Research
in partial fulfillment of the requirement
for the degree of
Master of Science in Electrical Engineering
2001

ELEG 5993: Independent Study

Advisor: Kelvin Kirby

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Introduction

As we continue to advance in exploring space frontiers, technology must also advance. The need for faster data recovery and data processing is crucial. In this, the less equipment used, and lighter that equipment is, the better.

Because integrated circuits become more sensitive in high altitude, experimental verification and quantification is required. The Center for Applied Radiation Research (CARR) at Prairie View A&M University was awarded a grant by NASA to participate in the NASA ER-2 Flight Program, the APEX balloon flight program, and the Student Launch Program. These programs are to test anomalous errors in integrated circuits due to single event effects (SEE).

CARR had already begun experiments characterizing the SEE behavior of high speed and high density SRAM's. The research center built a error testing system using a PC-104 computer unit, an Iomega Zip drive for storage, a test board with the components under test, and a latchup detection and reset unit. A test program was written to continuously monitor a stored data pattern in the SRAM chip and record errors. The devices under test were eight 4Mbit memory chips totaling 4Mbytes of memory.

CARR was successful at obtaining data using the Electronic TestBed System (EBS) in various NASA ER-2 test flights. These series of high altitude flights of up to 70,000 feet, were effective at yielding the conditions which single event effects usually occur. However, the data received from the series of flights indicated one error per twenty-four hours. Because flight test time is very expensive, the initial design proved not to be cost effective. The need for orders of magnitude with more memory became essential.

Therefore, a project which could test more memory within a given time was created. The goal of this project was not only to test more memory within a given time, but also to have a system with a faster processing speed, and which used less peripherals. This paper will describe procedures used to build an updated Electronic Testbed System.

Objectives

Figure 1 illustrates a brief diagram of the current testbed system. It is composed of the following components listed on A through C. This system was secured in the Superpod area of the ER-2 shown in figure 2.

However, the new testbed system will be secured in the ER-2's System 20 Pod area also shown in figure 2. Also, the new system will be installed in a cylinder tube, shown in figure 3.
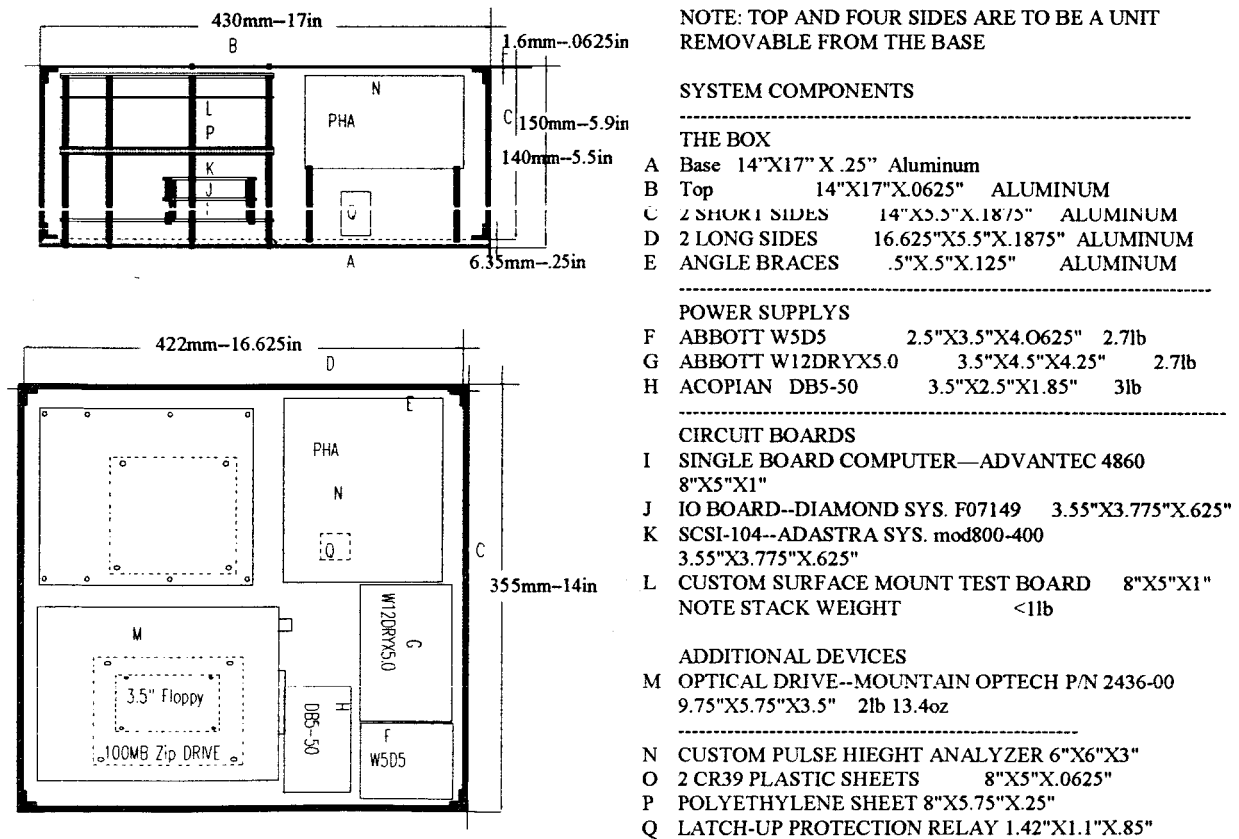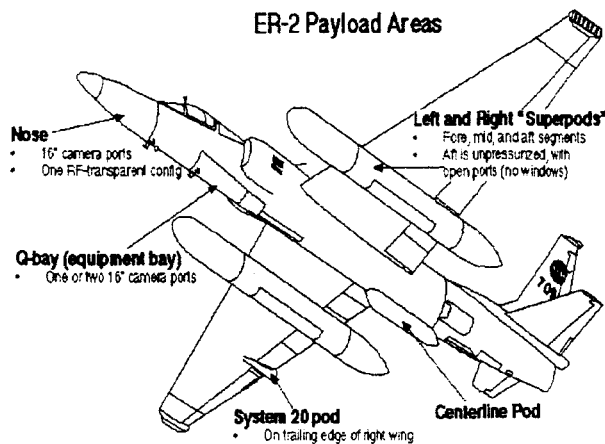
NOTE: TOP AND FOUR SIDES ARE TO BE A UNIT
REMOVABLE FROM THE BASE

SYSTEM COMPONENTS

THE BOX
A   Base   14"X17" X .25" Aluminum
B   Top   14"X17"X.0625"   ALUMINUM
C   2 SHORT SIDES   14"X5.5"X.1875"   ALUMINUM
D   2 LONG SIDES   16.625"X5.5"X.1875" ALUMINUM
E   ANGLE BRACES   .5"X.5"X.125"   ALUMINUM

POWER SUPPLYS
F   ABBOTT W5D5   2.5"X3.5"X4.0625" 2.7lb
G   ABBOTT W12DRYX5.0   3.5"X4.5"X4.25"   2.7lb
H   ACOPIAN DB5-50   3.5"X2.5"X1.85"   3lb

CIRCUIT BOARDS
I   SINGLE BOARD COMPUTER—ADVANTEC 4860
    8"X5"X1"
J   IO BOARD--DIAMOND SYS. F07149   3.55"X3.775"X.625"
K   SCSI-104--ADASTRA SYS. mod800-400
    3.55"X3.775"X.625"
L   CUSTOM SURFACE MOUNT TEST BOARD   8"X5"X1"
    NOTE STACK WEIGHT   <1lb

ADDITIONAL DEVICES
M   OPTICAL DRIVE--MOUNTAIN OPTECH P/N 2436-00
    9.75"X5.75"X3.5"   2lb 13.4oz

N   CUSTOM PULSE HIEGHT ANALYZER 6"X6"X3"
O   2 CR39 PLASTIC SHEETS   8"X5"X.0625"
P   POLYETHYLENE SHEET 8"X5.75"X.25"
Q   LATCH-UP PROTECTION RELAY 1.42"X1.1"X.85"

Figure 1

ER-2 Payload Areas

Nose
- 16" camera ports
- One RF-transparent config be

Q-bay (equipment bay)
- One or two 16" camera ports

Left and Right "Superpods"
- Fore, mid, and aft segments
- Aft is unpressurized, with open ports (no windows)

System 20 pod
- On trailing edge of right wing

Centerline Pod

Its normal cruise profile of flying at high altitude of (60 to 70) thousand feet will yield conditions necessary for Single Event Effects with the aircraft operating above 90% of the earth's shielding atmosphere.

Figure 2

Cylinder, which will hold new EBT, will be secured in System 20 Pod of ER-2.
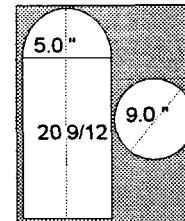
Figure 3

Goals

The following goals were set in order to find ways of accomplishing the objective of upgrading the current Electronic Testbed System:

- Conduct a market search for Pentium III motherboards and develop a selection process.
- Conduct a market search for Random Access Memory (RAM) Modules – SRAM & DRAM.
- Develop a design for the upgrade to the ETB.
- Evaluate the ETB software system.
- Recommend upgrades to the ETB software.
- Develop the design for the software upgrade.
- Integrate the Pentium III and upgraded software.
- Document the upgraded hardware and software.
- Conduct post-operational tests on the Pentium III system.

Market search for PC/104 Motherboard.

The research process began with a market search for an upgraded PC/104 motherboard with a pre-installed Intel Pentium III microprocessor. This was selected because it was one the fastest processors on the market. The PC/104 motherboard also needed to have a SCSI interface. The reason for the SCSI interface will be explained later.

What are PC/104 motherboards?

PC/104 based systems are used in a variety of places. For example, they are used in factories, laboratories, processing plants, vehicles, and almost anywhere devices must be controlled by a programmable computer. They are small systems and usually have low power requirements so they are great for applications that simply do not have the space for a full-blown desktop PC. Additionally, PC/104 systems are designed to be more rugged than desktop systems. Building a system using PC/104 modules usually costs more than a commercial PC, but usually less than a rack mount ISA bus system.

The PC/104 form factor motherboard was first developed by Ampro Computers in California in the late 1980's. The specification was published in 1992 in order to enhance popularity. Over 150 vendors manufacture PC/104 compatible products including controller cards, software, and accessories. The PC/104 Consortium was established to maintain the specifications, publish resource guides, participate in standards activities, and to promote PC/104 at trade shows and news releases.

PC/104 gets its name from the popular desktop personal computers initially designed by IBM called the PC, and from the number of pins used to connect the cards together (104). PC/104 cards are much smaller than ISA-bus cards found in PC's and

stack together which eliminates the need for a motherboard, backplane, and/or card cage. Power requirements and signal drive are reduced to meet the needs of an embedded system. Because PC/104 is essentially a PC with a different form factor, most of the program development tools used for PC's can be used for a PC/104 system. This reduces the cost of purchasing new tools and also greatly reduces the learning curve for programmers and hardware designers.

There are many modules available for the PC/104. This includes common functions like CPUs, Serial I/O ports, and Video Controllers; but also more exotic modules like GPS receivers, vehicle power supplies, wireless communications. A stack of PC/104 modules can be attached as a component of a larger circuit board, or simply put in a small enclosure for stand-alone operation.

Which PC/104 board was selected?

After doing a comprehensive market search for the updated PC/104 motherboard, it was decided that the CARR research center would use the vendor, Toronto Microelectronics Inc. The vendor 5811 PC/104 motherboard, shown below in figure 4, can be manufactured using the following configurations listed in Table 1
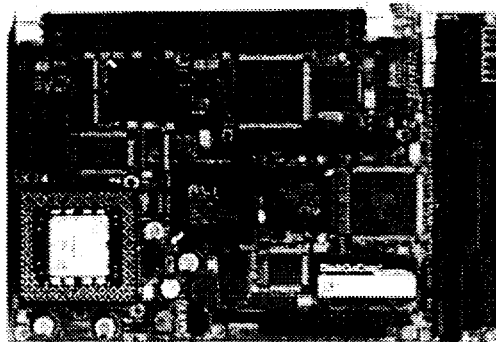
TME 5811 PC/104 Board with SCSI Interface

Figure 4

CPU
- Supports Intel low power MMX processor with 1.9V Core and 2.5V I/O
- Supports Intel MMX Pentium and AMD K6, K6-2, K6 2/3D
- Processor speeds of 166, 233, 266, 300, 333, 400, 450 MHz.
- 66, 75, 83 or 100 MHz system bus speed

CPU Production Selection
- Pentium 166 MHz MMX
- Pentium 233 MHz MMX
- Pentium 266 MHz MMX
- AMD K6-2 333 MHz
- AMD K6-2/3D 400 MHz

CHIPSETS
- Alladin V Core
- C&T B69000 / B69030 video
- Intel 82558 10/100Base-T
- SYMBIOS 53C875 SCSI

THERMAL MANAGEMENT
- Overheat protection
- Overheat slow down
- Thermal controlled CPU & system fan connectors

DRAM MEMORY
- Two 168-pin DIMM sockets
- Supports up to 512 MB of SDRAM
- Supports 3.3V EDO or SDRAM
- Supports non-parity, parity and ECC

CACHE MEMORY
- Standard 512 KB L2 Synchronous Burst Cache.

FLASH MEMORY / SOLID STATE DRIVE
- M-System Disk-On-Chip (DOC) with up to 144 MB of Flash with built-in EDC/ECC
- Support DOS, Windows NT, Window CE, Windows 95, QNX, pSOS and VxWorks OS

I/O SPECIFICATIONS: GENERAL PURPOSE STANDARD I/O PACKAGE:
- 7 DMA Channels (8237 compatible).
- 15 Interrupt channels (8259 compatible).
- 50 PPM accuracy and Y2K compliance
- Built-in removable lithium battery pack supports up to 10 years
- Floppy controller includes 2.88 Mbyte support on 2x17 shrouded header.
- three 16C550 RS-232C COM port with FIFO buffering and 15KV ESD protection.
- One 16C550 RS-232C COM port with FIFO buffering and 15KV ESD protection with optional RS-485.
- Parallel Printer port with ECP/EPP support.
- Dual independent EIDE supports Ultra 33 DMA
- Supports up to 4 drives on 2x22
- PS/2 mouse and keyboard ports on 6-pin mini DIN connector. Keyboard inhibit port
- Two USB Ports.
- On-board 2x8 shrouded header supports keyboard, mouse, keyboard inhibit, reset and external buffer.

ULTRA SCSI
- Ultra SCSI interface supports up to 40 MB/s data transfer rates using SYMBIOS 53C875
- Supports fixed disk, removable media drives, SCSI printer, rewrite optical drives, CD-ROM drives, tape drive, DAT, MO, scanner, Photo-CD support and other

OPERATING SYSTEM
- Windows 95, Windows 98, WindowsNT 4.0, UNIX, SCO UNIX, LINUX, LYNX, VxWorks, QNX, BANYAN, NOVELL, OS/2, LANtastic and more*

TOUCHSCREEN
- DYNAPRO-compatible touch-screen interface supports 4, 5 or 8 wires touch-screen

EMBEDDED PC SYSTEM FEATURES
- Watchdog timer with software or hardware disables
- 128 bytes of SEEPROM for CMOS data backup
- 128 bytes of SEEPROM for manufacturing information
- 256 bytes of SEEPROM of user
- Up to 64 KB of extension ROM using on-board programmable flash memory for user firmware
- AT-compatible Real-Time clock with 50 PPM accuracy
- 15KV ESD protection on serial ports
- Power Failure detection circuitry
- 7 year Lithium battery for Battery–Backed SRAM
- 5 Year product availability support (subject to component availability)
- Warranty of product consistency

EMBEDDED SYSTEM BIOS FEATURES
- Full AT compatible BIOS.
- BIOS stored in Flash EPROM to faciliate remote firmware update capability
- Optional no-fail boot, Fast Boot, and Secured-boot
- Optional batteryless operation.
- Optional Customer sign on message at boot up
- Advanced firmware setup utility for system parameters and I/O configuration
- Power saving mode with "green PC"

BUS
- 16-bit Pc/104 interface for optional sound, CompactFlash, Battery-Backed SRAM, additional serials ports, and additional network interface
- 32-bit PCI bus PC/104-Plus bus.
- Supports 33 MHz PCI bus clock

OPTIONAL ON-BOARD I/O FEATURES:
- Video Interface
- On-board Flat Panel & CRT display interface using C&T 69000 with optional C&T B69030
- Support for LCD monochrome, S/S and D/D STN, TFT, EL and gas plasma Flat Panel displays to 1280x1024 resolution.
- Supports 3.3V or 5V Flat Panel display.
- Supports up to 36-bit LCD on both TTL and LVDS interface.
- Capable of driving high resolution LCD at distances up to 20'
- Supports ZV port
- 2 MB of SDRAM display memory on C&T B69000
- 4 MB of SDRAM display memory on C&T B69030

Table 1

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Table 1 continued

NETWORK FEATURES
- Intel 82558 Device
- 32-bit PCI local BUS interface
- Supports 10/100Base-T/TX
- Supports PCI BUS Master
- Supports Remote Boot-ROM for diskless system
- Supports IEEE 802.3 standard
- Supports Ethernet standard
- Configuration information stored in EEPROM for jumperless configuration
- Device Drivers for DOS/Windows, Windows NT, Windows95, SCO UNIX, UNIX, Novell, OS/2 and more...

DIMENSIONS
- 5.75" X 8" EBX form factor

ENVIRONMENTAL Operation
- Temp: 0° C to 65° C @ no airflow (with CPU fan sink only)
- -40° C to +80° C available upon request
- Humidity: 5% to 90% non-condensing

STORAGE
- Temp: -40°C to 95°C
- Humidity: 5% to 95% non-condensing.

Note: Please refer to TME's web-site for more information at http://www.tme-inc.com.

The TME motherboards with Intel Pentium 266 MHz MMX and AMD K6-2/3D 550 MHz were selected. They were the faster processors by Intel and AMD which came on PC/104 motherboards at the time. Intel Pentium III processors were not available on the PC/104. For now, they only come on the standard personal computer motherboards. The selected motherboard also can with Dual Ultra DMA/33 EIDE and floppy interface, four serial ports, one parallel port, and two USB ports.

The major advantage of the TME PC/104 motherboard that we selected is the 16Mbyte fully bootable single-chip flash disk. This on board solution is called *DiskOnChip 2000* made by M-Systems. It has high performance read/write for data reliability. As a result, this alleviates the need for the 1.44M floppy drive, which was necessary on the previous TestBed system to run the operating system. The previous system was started by a Microsoft Windows 95 boot-disk. The updated system uses the full version of Dos 6.0.

DiskOnChip 2000

Figure 5

The *DiskOnChip 2000*, shown above in figure 5, is a unique data storage solution. It offers cost effective data storage beyond that of traditional hard disks. Because the *DiskOnChip 2000* is integrated into PC/104 motherboard, it allows more space in for additional storage devices.

It is a perfect solution for running the application program used for retrieving data from Single Event Effects on DRAM and SRAM storage devices. The old Test-Bed uses the Iomega Zip Drive to run TestBed software program, and result data. The Disk on Chip, however, is more cost effective in reducing the need for a 1.44M floppy Drive and omega Zip Drive. It can boot-up the system, run the TestBed program, and store result data.

Storage Solution(s)

DRAM Storage-Device

The reason the PC/104 motherboard with a SCSI interface was chosen is because of the DRAM Storage device. This device is the primary Device Under Test (DIT) for the new TestBed system. The DRAM storage device holds the high capacity storage need to test orders of magnitude more memory. After doing a comprehensive search of a DRAM storage device, it was decided to use the Curtis, Inc. Clipper(II) storage device. This device can hold up to 8.6GB of memory. This capacity of memory is significantly larger than the 8Mbytes tested on the previous Test-Bed system.

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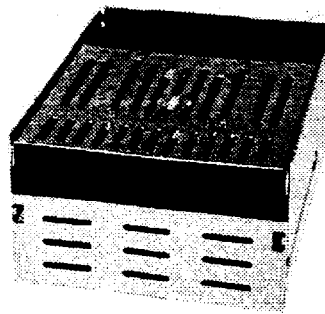
Curtis, Inc. Clipper II Storage Device

Figure 6

The Clipper II, shown above, in figure 6, is a "plug and play" device. Thus, it is easy to

install, and appears on the system like other standard hard drives. It is available with

Ultra2 SCSI interface, which makes the Clipper II a flexible device for the TME PC/104

motherboard. Table 2 lists the data sheet for the Clipper II storage device.

Specifications Description
- Desktop/Rackmount Solid State Disk
- Interface: Ultra2SCSI or FibreChannel

Models and Capacities
Ultra2 SCSI Interface Models
- CLIP2-DSK-1GB........................1GB
- CLIP2-DSK-2GB.....................2.1GB
- CLIP2-DSK-3GB.....................3.2GB
- CLIP2-DSK-4GB.....................4.3GB
- CLIP2-DSK-8GB.....................8.6GB

Physical Specifications
Desktop Models Ultra2SCSI/FibreChannel
- Height.............................6.7"/ 12.4"
- Width...............................7.5" / 9.5"
- Depth..............................12" / 12.3"
- Weight.............................20 / 25 lbs

Reliability
- MTBF.......................>1,000,000 Hours
- Integrated ECC Memories.............72bit
  (64Data/8ECC) modified Hamming Code
  meets/surpasses server memory requirements

Environmental Characteristics
- Operating Temperature.....0 to 50°C
- Non-Condensing Humidity....10 to 90%
- Altitude...............................10000 ft.

High Performance
- Access Time..........................60mS
- I/O (transactions/sec)..............>10000
- Interface Transfer Rate
  (U2SCSI).............................80MB/sec
- Data Transfer Rate
  (sustained)..........................>68MB/sec

Power Requirements
- 115/230V AC 65W

Data Retention and Power Management
- External AC/DC Backup Power Supply
- Integrated Lead Acid Battery and Charger: minimum
  2 hours data retention in battery backup mode
- Optional internal mechanical disk backup available

Table 2

SRAM Storage Cards

The use of SRAM card is an alternative way of recording Single Event Effects. Unlike the DRAM storage device, the SRAM cards do not need to be connect to tests system during test flight. The SRAM cards act as the secondary (DUT). Data files are stored on the devices before the test flight. The device data files are not be evaluated until the flight test is completed.

After doing a comprehensive search of SRAM storage cards, it was decided to use the MagicRAM Industrial 8Meg SRAM Memory cards, shown in figure 7. They are packaged in a PCMCIA Type II housing with x8/x16 PCMCIA Standard Interface. The cards are based on advanced CMOS technology, providing very low power and reliable data retention characteristics. The MagicRAM Industrial SRAM cards contain a rechargeable lithium battery and recharge circuitry, eliminating the need for replaceable batteries. They have an extended battery backup time of 2.5 months. The recharge feature eliminates the danger of battery failure and data loss during critical times, as well as risk of damage to the host and module components when batteries are removed or inserted.

MagicRAM Industrial SRAM cards

Figure 7

The MagicRAM Industrial SRAM card battery is encased in an ultra-sonically welded housing, thereby offering greater resistance to shock and vibration. They can operate in standard (0°C - +70°C) and extended temperature (-40°C - +85°C).

The SRAM cards will be stacked on top of one another in the test tube. Therefore 20 cards will provide 160Meg of additional memory to SEE evaluation process. After being flown at high altitudes, the pre-flight stored image/pattern will be compared to the original stored on a computer at CARR.

Software Program

In order to make the update Test-Bed computer work efficiently with the DRAM and SRAM memory devices, a software program was written. The updated test program design was similar to the previous test-bed program shown below in Figure 8.
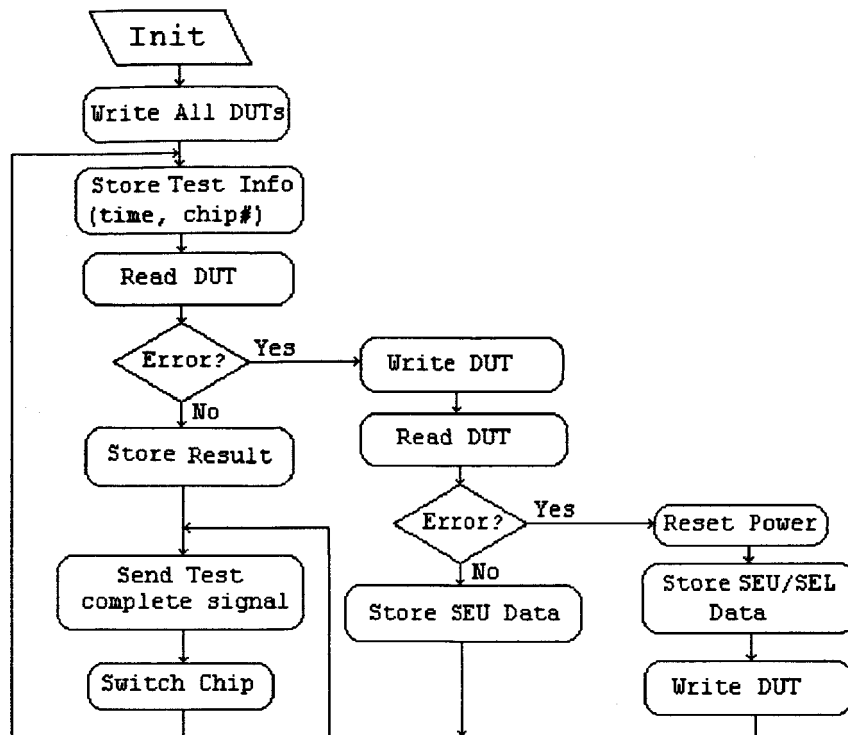
ER-2 Memory Test Flow

Figure 8

Figure 7 shows the flow chart of the test program, which was developed using the C programming language. In this program, time is continuously recorded to the output file. The data pattern is written to all of the Device Under Test, in this case, 8 4Mbit Chips. Then the test program checks each chip for errors. When an error is detected, the data pattern is rewritten to the DUT and checked again to identify any radiation effects (Single Event Upset/Single Event Latchup) to the DUT, or even the testing device itself. If there is an error in the testing device, the power is reset.

In writing the program, a few things warranted special consideration. The updated Test-Bed system contained integrated circuits which were vulnerable to Single Event Effects. As a result, a WatchDog-Timer was required. This unit receives a signal from the CPU module at certain intervals indicating that the test

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program is functioning correctly. When the CPU module fails to send the signal, this indicates that a Single Event Effect occurred in the TestBed system. This detection causes the TestBed system computer to restart. Each time the test program is cycled, it stores the time and begins processing. The program does not end until the power is turned off or manually interrupted.
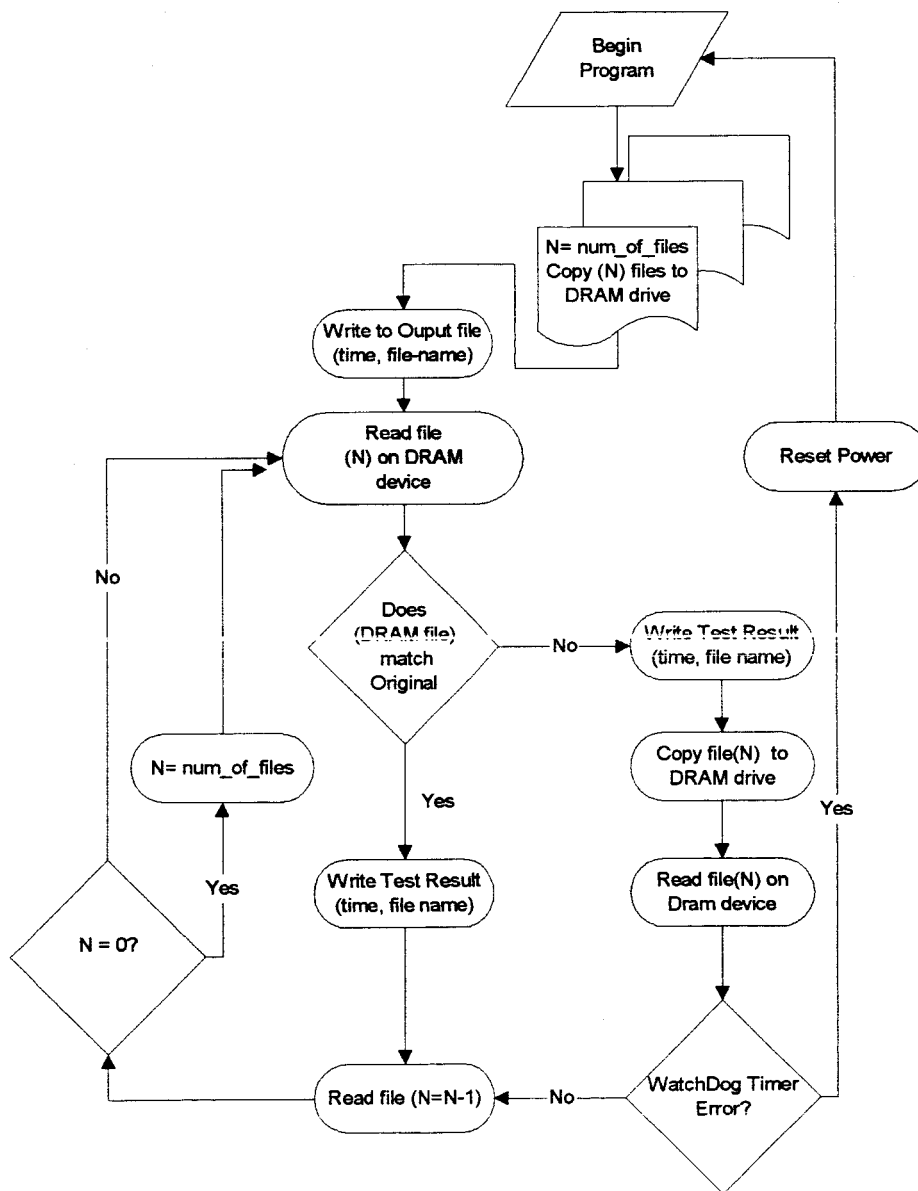

Figure 9

Figure 9 illustrates updated test program. Throughout the program, the time continually recorded to the output file. Multiple data files are copied from the Disk-on-Chip to the DRAM storage device. These files are repeatedly compared to the original, just as the each chip was tested for errors in the previous Test-Bed program. In the new system, when an error is detected the data is rewritten to the file and checked again to verify if a Single Event Effect has occured, or if there is an error in the testing device. If an error is identified by the WatchDog Timer, the testing device power resets. This process continues to repeat throughout the test flight.

Figure 10 shows the flow chart of the updated test program for the SRAM storage chips. In this program, data files are read into the storage device before the flight test begins. However, unlike the two programs mentioned previously, data files are not read until the end of the test flight. Therefore, there is no need for theses devices to be connected throughout the test flight. Data can then be compared to its original files stored in the research center.
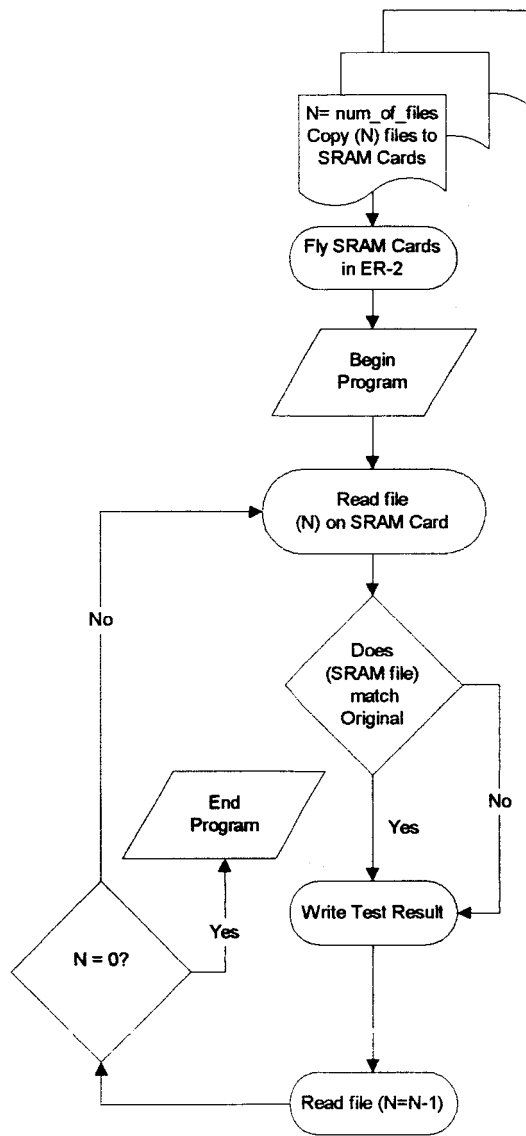
Figure 10

Conclusion

This projected was designed to accomplish two objectives. First, to update the current TestBed system, and second, to test orders of magnitude more memory. These objectives were accomplished by setting the following goals:

- Conduct a market search for Pentium III motherboards and develop a selection process.
- Conduct a market search for Random Access Memory (RAM) Modules – SRAM & DRAM.
- Develop a design for the upgrade to the ETB.
- Evaluate the ETB software system.
- Recommend upgrades to the ETB software.
- Develop the design for the software upgrade.
- Integrate the Pentium III and upgraded software.
- Document the upgraded hardware and software.
- Conduct post-operational tests on the Pentium III system.

Most of the goals were met. Unable to find a Pentium III processor, a substitution was made with the fastest processor available on a PC/104 motherboard. This processor was the AMD K6-2/3D 400 MHz. The motherboard, was created by Toronto Microelectronics Inc,(TME). The flask disk chip on the TME motherboard, allowed the upgrade of the current system significantly. The DiskOnChip storage device reduced the need for a 1.44M floppy drive, and a 100M Iomega Zip Drive. As a result, this yielded more space for Devices Under Test.

In conclusion, there was success in locating SRAM and DRAM devices. However, both devices are still on order. A final design and integration of the Electronic Test Bed software upgrade will not be complete until the storage devices are received. The current software has been evaluated, and upgrades have been recommended. This

information will be helpful in continuing the Electronic TestBed project. Figure 11 illustrates the updated TestBed System once all components have been complete integrated.

After all equipment is received the, a post-operational test can be conducted on the system at the Texas A&M University Cyclotron Institute and the EBT can then be run on the ER/2. All work to date has been documented and placed in the Center for Applied Radiation Research Library.
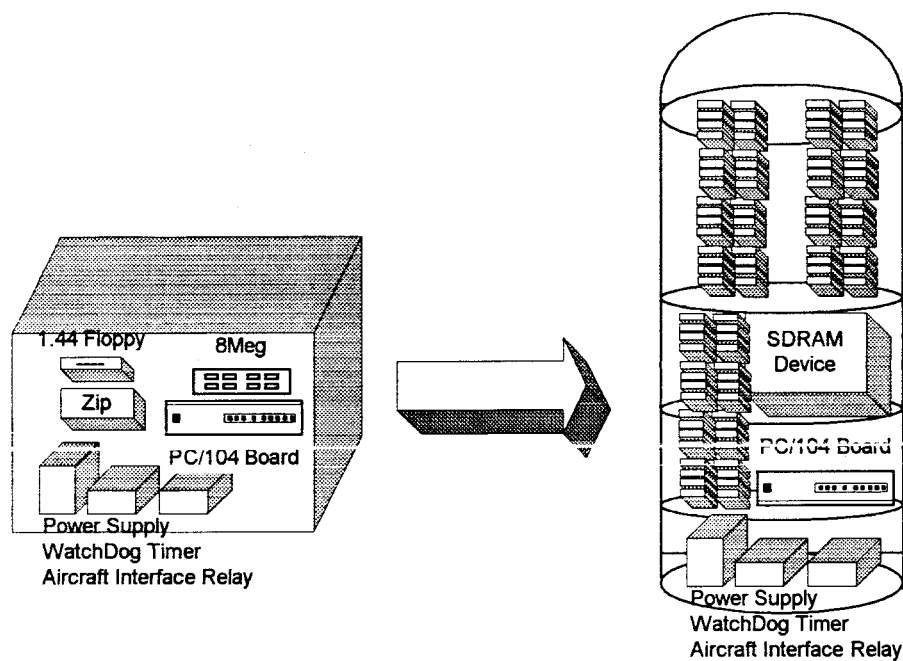
Updated TestBed System with Integrated Components

Figure 11

Acknowledgements

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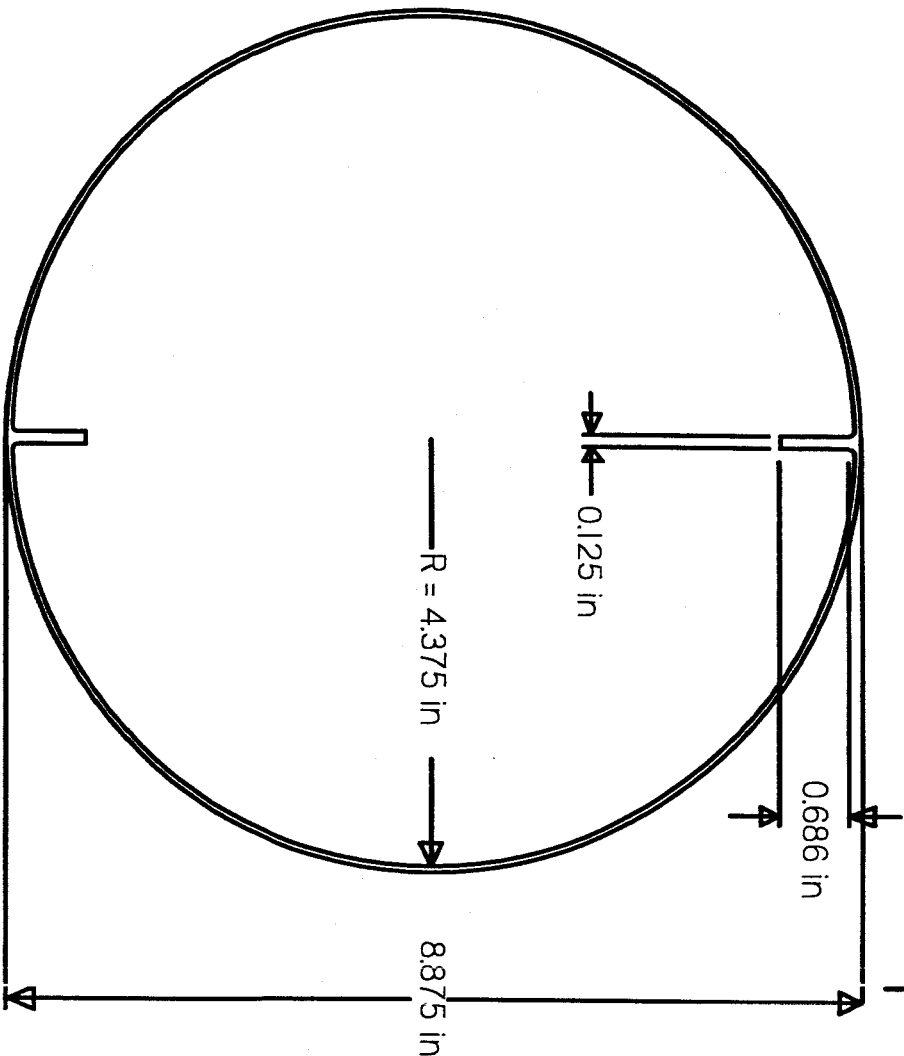
http:\\ www.mncurtis.com
http:\\www.pc104.com
http:\\www.m-sys.com
http:\\www.tme-inc.com

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Appendix B

System 20 Pod / SRAM Mounting System

System 20 Pod / S-RAM
Mounting System
N.A.S.A. CARR
Noah Rattler

R = 4.375 in

0.125 in

0.686 in

8.875 in

	REVISION HISTORY		
REV	DESCRIPTION	DATE	APPR

	NAME	DATE
DRAWN	meclass	03/17/03
CHECKED		
ENG APPR		
MGR APPR		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
ANGLES ±X.X°
2 PL ±XXX 3 PL ±XXXX

SOLID EDGE
EDS-PLM SOLUTIONS

TITLE
System 20 Front

SIZE	DWG NO
A	

FILE NAME: Sys20POD.dft

SCALE: | WEIGHT: | SHEET 1 O

8.875 in

17.25 in

7.250 in

	REVISION HISTORY		
REV	DESCRIPTION	DATE	APPR

	NAME	DATE
DRAWN	meclass	03/17/03
CHECKED		
ENG APP'R		
MGR APP'R		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
ANGLES ±X.X°
2 PL ±XXX 3 PL ±X.XXX

SOLID EDGE
EDS-PLM SOLUTIONS

TITLE
System 20 Side

SIZE	DWG NO
A	

FILE NAME: Sys20PODside.dft

| SCALE: | WEIGHT: | SHEET 1 O |

R=.622 in

0.125 in

R = 4.875 in

2.125 in

.125 in

D = .375 in

3.250 in

9.25 in
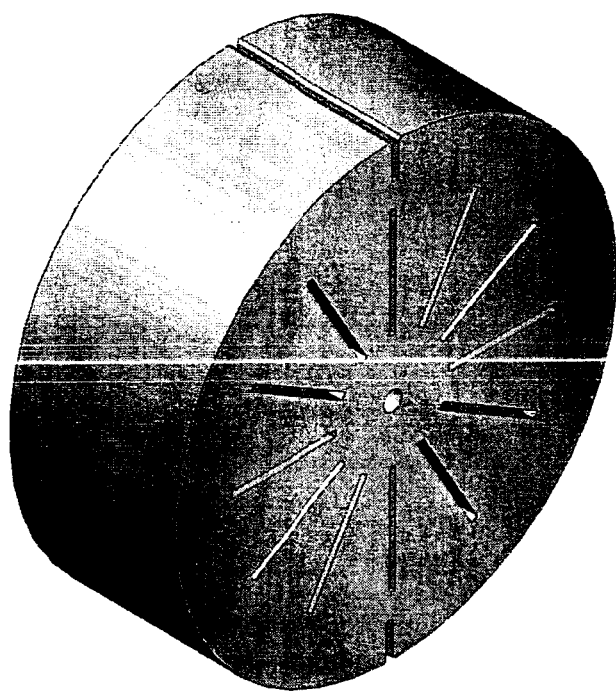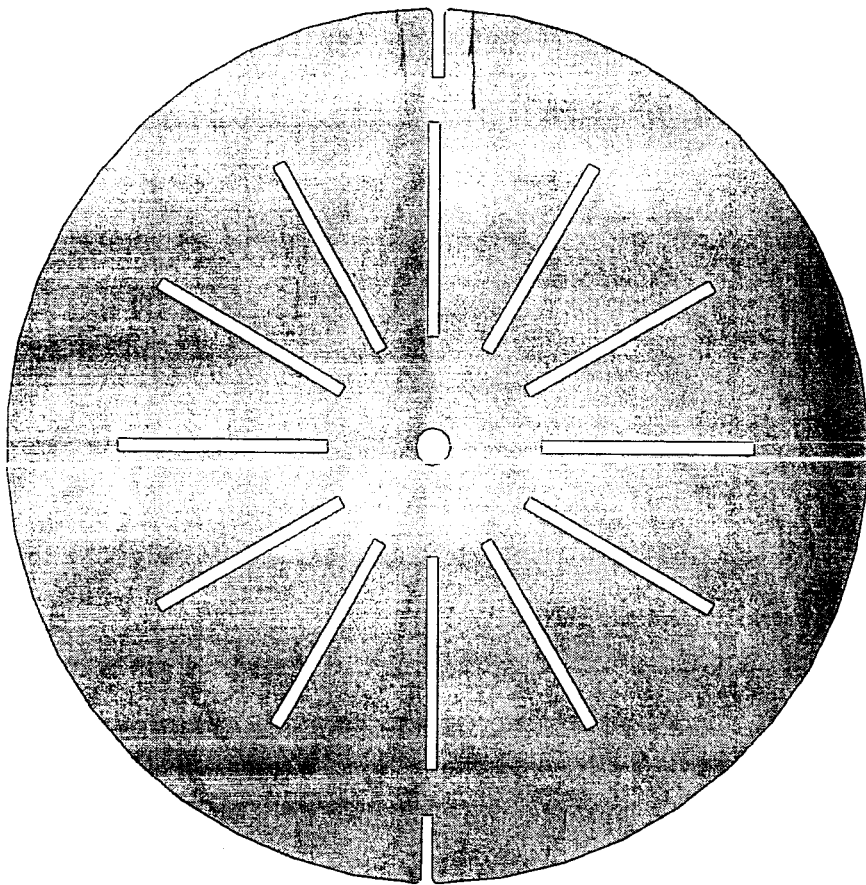
	REVISION HISTORY		
REV	DESCRIPTION	DATE	APPRC

	NAME	DATE
DRAWN	meclass	03/17/03
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ENG APPR		
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UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
ANGLES ±X.X°
2 PL ±XXX 3 PL ±XXXX

SOLID EDGE
EDS–PLM SOLUTIONS

TITLE
Outside Sponge Dimensions

SIZE	DWG NO		
A			
FILE NAME: Spongeout.dft			
SCALE:	WEIGHT:		SHEET 1 C

R=.622 in

R = 4.625 in

0.125 in

2.125 in

.125 in

D = .375 in

8.75 in

3.250 in

	REVISION HISTORY		
REV	DESCRIPTION	DATE	APPROV

	NAME	DATE
DRAWN	meclass	03/17/03
CHECKED		
ENG APPR		
MGR APPR		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
ANGLES ±XX°
2 PL ±XXX 3 PL ±XXXX
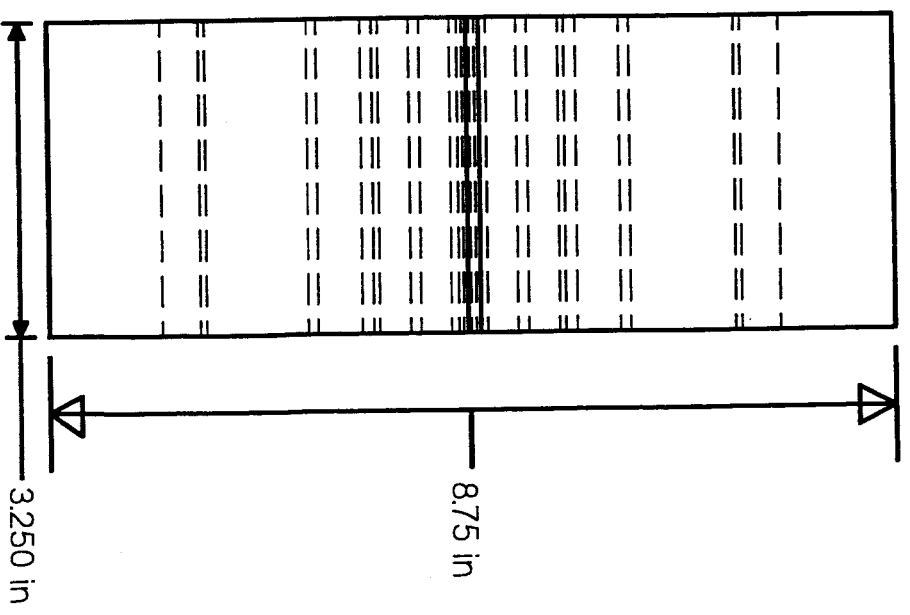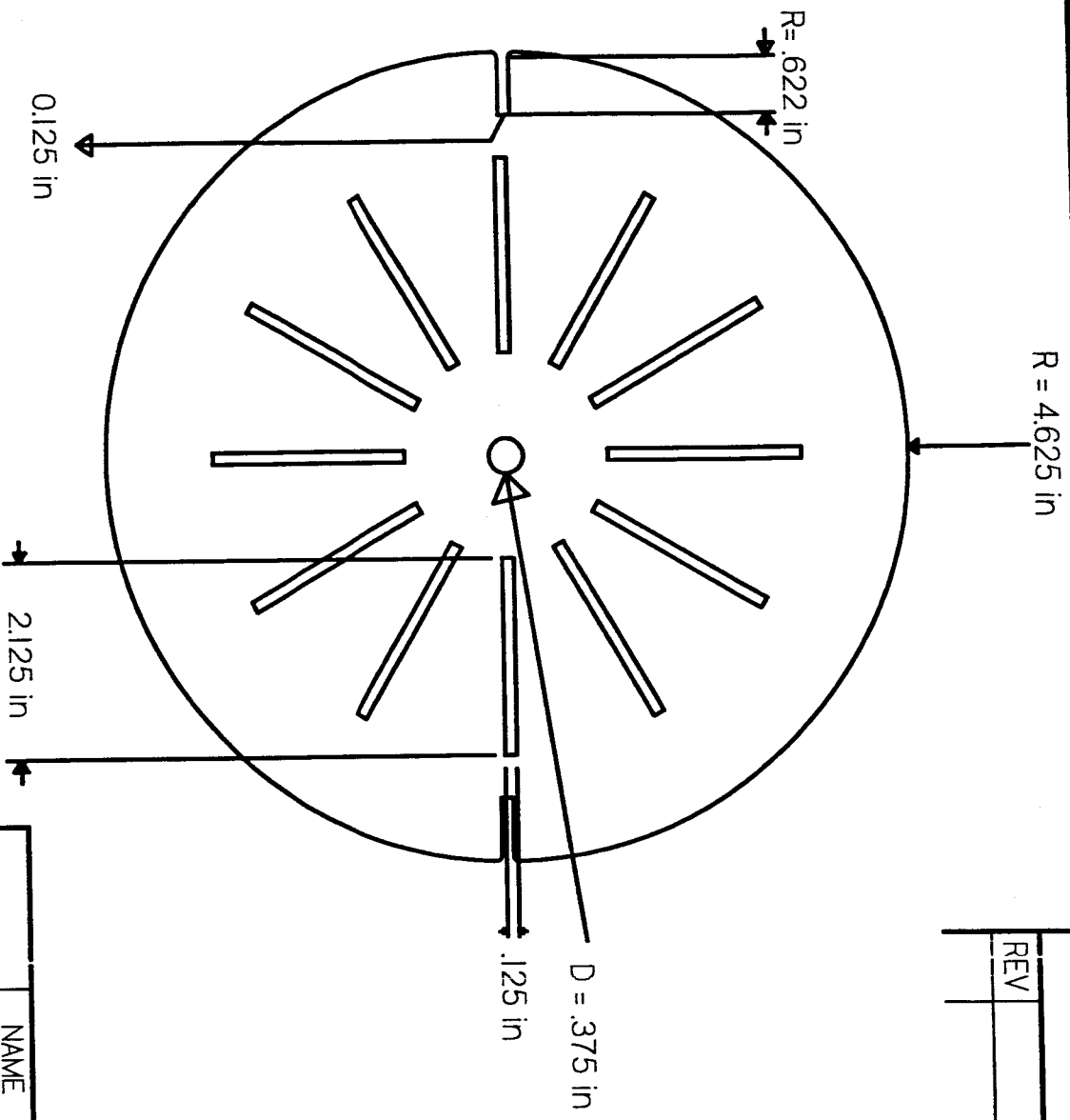
SOLID EDGE
EDS-PLM SOLUTIONS

TITLE
Inside Sponge Dimensions

SIZE	DWG NO
A	

FILE NAME: Spongein.dft

SCALE: WEIGHT: SHEET 1 0

d = 0.2813 in

8.875 in

0.125 in

REVISION HISTORY

REV	DESCRIPTION	DATE	APPRO

	NAME	DATE
DRAWN	meclass	03/17/03
CHECKED		
ENG APPR		
MGR APPR		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
ANGLES ±XX°
2 P_ ±XXX 3 PL ±XXXX

SOLID EDGE
EDS-PLM SOLUTIONS

TITLE
Aluminum End Piece

SIZE	DWG NO
A	

FILE NAME: TopBtm.dft

SCALE: | WEIGHT: | SHEET 1 O

D = 4.375 in

D = 0.375 in

8.750 in
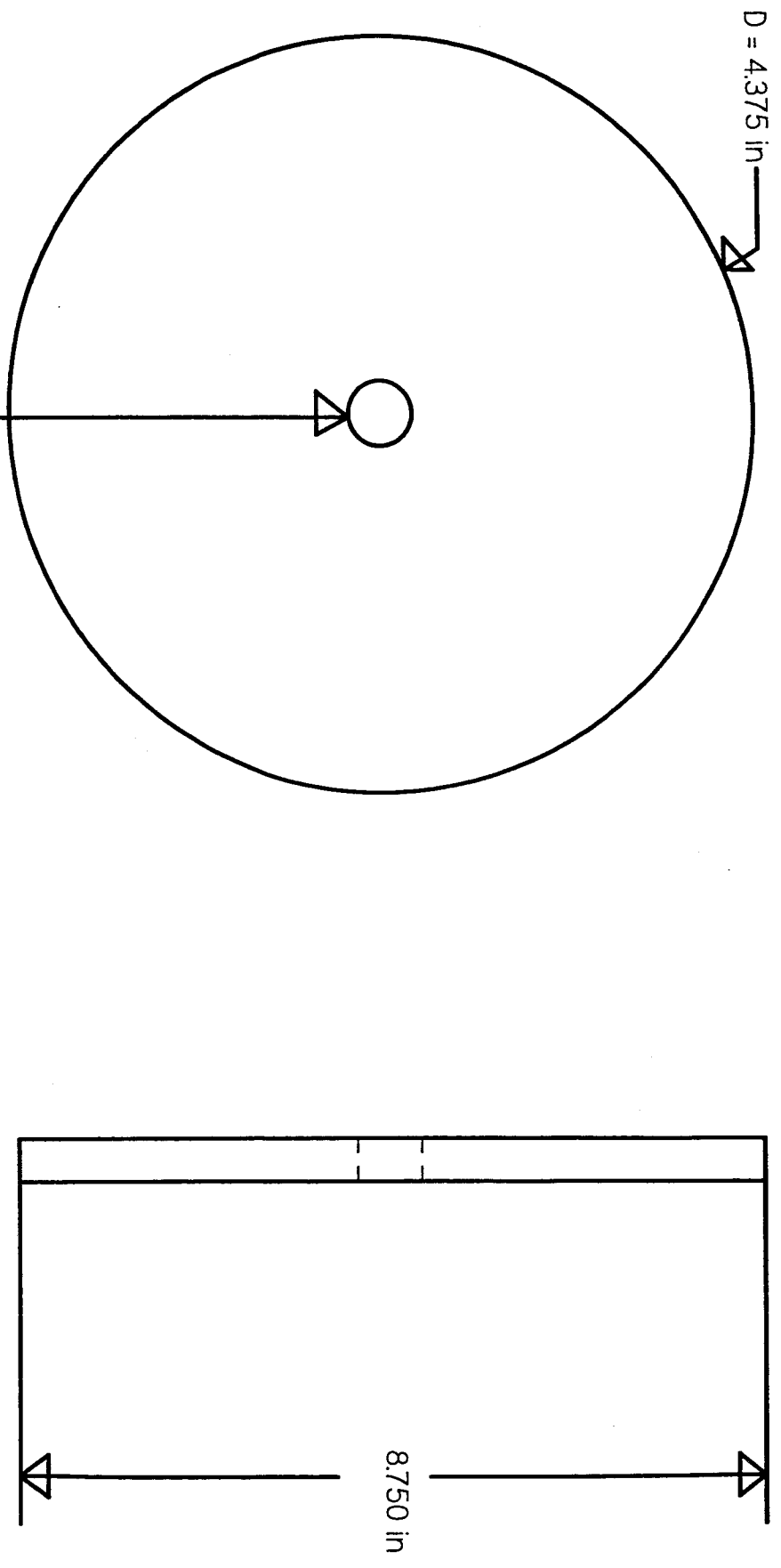
	NAME	DATE
DRAWN	meclass	Error: Not defined.
CHECKED		
ENG APPR.		
MGR APPR.		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
ANGLES ±X.X°
2 PL ±X.XX 3 PL ±X.XXX

SOLID EDGE
EDS-PLM SOLUTIONS

TITLE
Intermidiate Piece

SIZE A	DWG NO	

| FILE NAME: Draft3 | | |
| SCALE: | WEIGHT: | SHEET 1 OF |

Front View

1/4 - 20 thread

1/4 - 20 thread

.643 kpsi

0.5 in

17.25 in

D = 0.25 in

Top View

1:1

D = 0.643 in

	NAME	DATE
DRAWN	meclass	03/19/03
CHECKED		
ENG APPR		
MGR APPR		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
ANGLES ±X.X°
2 PL ±.XXX 3 PL ±.XXXX

SOLID EDGE
EDS-PLM SOLUTIONS

TITLE
Connection Rod

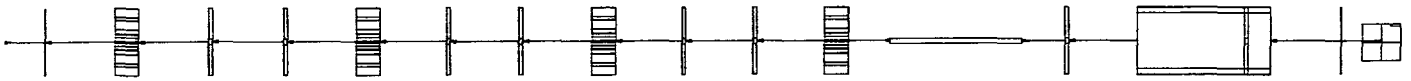| SIZE	DWG NO
A	

FILE NAME: CnnctRddft

SCALE: | WEIGHT: | SHEET 1 OF
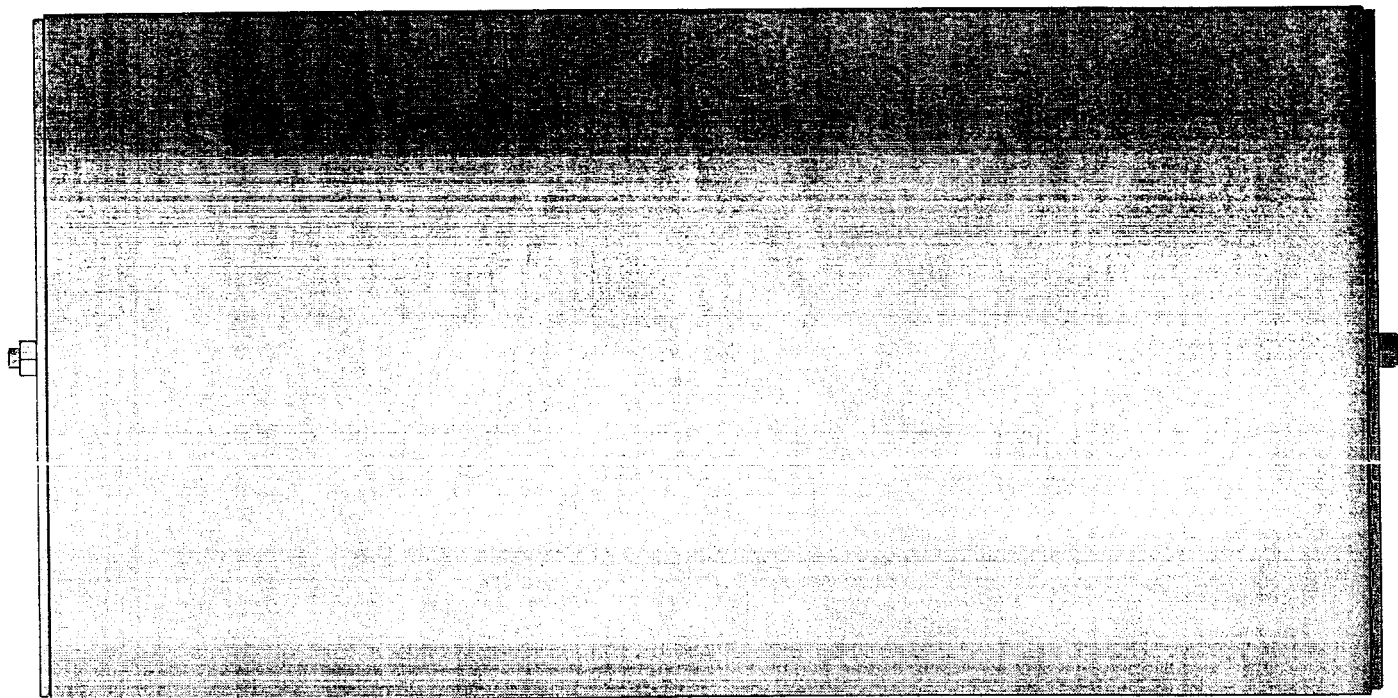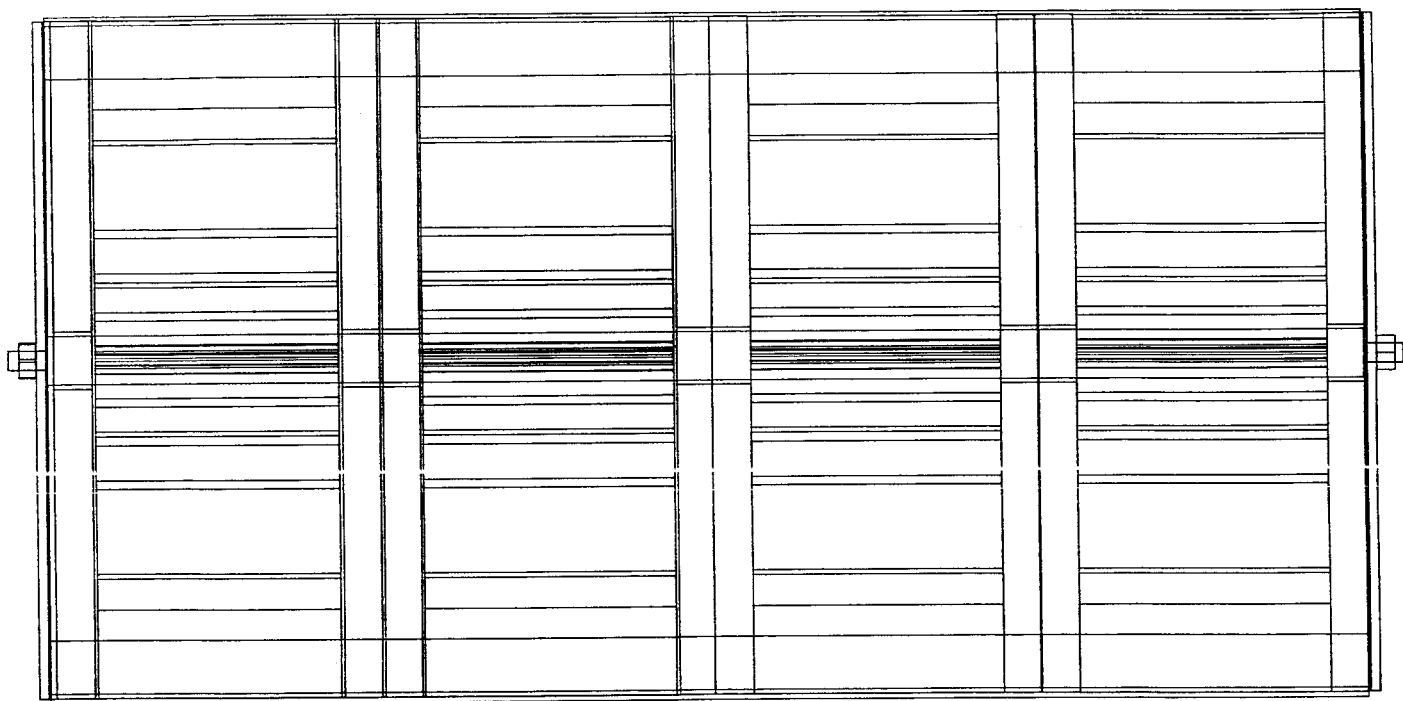
Appendix C

Error Detection and Correction – Control Systems

ERROR CORRECTION, CONTROL SYSTEMS AND FUZZY LOGIC
By Earl B. Smith

Abstract

This paper will be a discussion on dealing with errors. While error correction and communication is important when dealing with spacecraft vehicles, the issue of control system design is also important. There will be certain commands that one wants a motion device to execute. An adequate control system will be necessary to make sure that the instruments and devices will receive the necessary commands. As it will be discussed later, the actual value will not always be equal to the intended or desired value. Hence, an adequate controller will be necessary so that the gap between the two values will be closed.

Introduction

The point of this research was to find a suitable link between control systems design and error correction and detection. This was sought as to basically enhance both techniques. One reason of thinking was that if the error correction algorithm was made more efficient that it would make it easier for the control system or systems to function. Also, if the control system is stable, the thinking is that the pressure would be taken off of the error detection and correction, parity, and checksum techniques in order for them to function at its highest capability.

It should be stated that error correction is necessary to combat the errors caused by radiation, regardless of the control system. It is necessary so that as many errors as possible are corrected. So a control system should not be used in place of error

correction and detection. The same or similar things could be said of a control system being replaced.

So the paper is set up as follows. The paper primary focuses on control systems as oppose to error correction and detection, parity, and checksums. This is done because of the author primary has a background in control systems, and control systems do deal with error.

The next section briefly discusses control systems and control system design. The discussion primary centers on the error that is obtained in a closed loop system. The use of the controller is mentioned to state, a little, on how the error, the difference between the actual and desired values, is reduced.

In the conclusion and recommendations, findings and ideas on future work are presented.

Error, Correction and Detection, Control Systems and Fuzzy Logic

In his example of using one's eyes, Pretzel in [1] stated how the eyes are able to use experience to find out or understand the correct image that is being seen. Then the brain uses various techniques to sort out the possible conclusions.

He also discusses another method of correcting error where the language restrictions are used as oppose to experience.

Pless in [2] defined error correcting as "the art of adding redundancy efficiency so that most messages, if distorted, can be correctly decoded." As stated in various works, the transmission of data that is redundant is compared for agreement, or the lack thereof, purposes [1-10].

2

Yet, when the issue of error is discussed in control systems, it has to do with the error or actuating signal [11-15]. Its values are obtained from a closed loop transfer function where it is the input into the controller. Consider in figure one the variables R, C, and E. Let R be the reference or desired input. Let C the actual or controlled output. And let E the error or actuating signal. Also, let there be unity feedback and no gain at the input as it is shown in Figure One. Then the error, E, is equal to C-R [11-15]. Any value of E not equal to zero may require some kind of compensator, lead or lag, to be added to the controller [11, 12]. With the changes in the controller, there may be increased stability, more robustness, and a bigger chance of the actual value reaching the desired value.
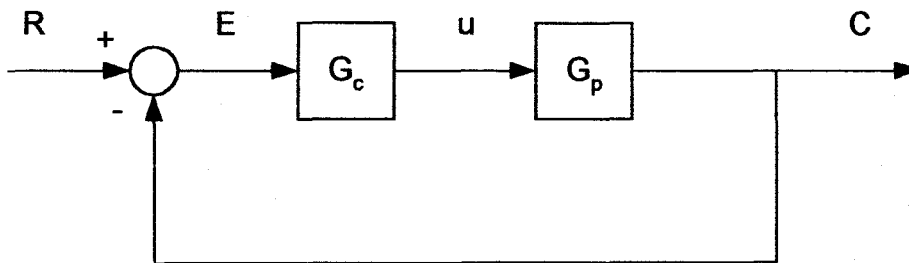
Figure One. Block Diagram with unity feedback.

If there is a gain at the input as shown in Figure Two, it is called the filter gain. Non-unity feedback is referred to as the feedback compensator. Then the error, E or E(s), could be equal to HC-G_fR where H is for the feedback compensation and G_f is the input filter [11, 12, 15].
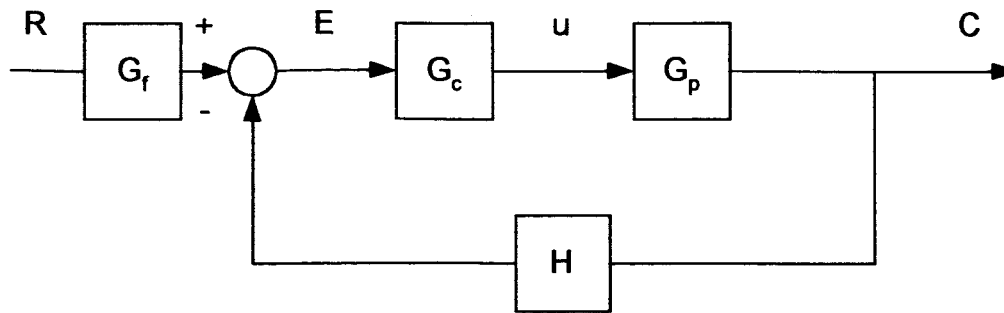
Figure Two. Block Diagram with non-unity feedback and filter input.

Some issues that deal with control systems are the temperature inside, temperature of other compartments, the speed, and direction. In physics terms speed with direction can be combined for the velocity, a vector. Some of this will be discussed later.

Also, it is desirable to make sure that the control system is very stable, robust and have little steady-state error. Regardless the types of control systems, this could be done by a variety of ways. Those ways include using the linguistics of a fuzzy logic control system, designing a suitable compensator or comparator, and adequate feedback [11-15].

Control systems can be either continuous, discrete or both [12]. Robotic systems, automonous, pre-programmed or teleoperated, can contain control systems that are continuous and discrete. As Stadler stated in [16] logic gates and binary concepts are important in understanding encoders and decoders. Encoders and decoders are an integral part of the electronics of a robotic system, especially when it comes to sending messages. This includes the operational amplifiers, semiconductor devices, solid-state devices, and logic circuits.

Needless to say, the operation of the sensors is paramount to how the robotic systems take commands and function [17]. When the sensor takes in the analog value from the medium or the outside, the quantity (or image) that the observer accepts may not

4

be exactly the same value as the analog value [16]. The analog signal, or value, that comes in from the medium, or outside, is detected and later manipulated and measured for the observer [16]. Or as Jones and Flynn stated in [18], the input from the sensors are gathered and interpolated. Then the world model is developed, and the planning and execution comes. Yet due to errors and uncertainty, we are not able to 100% completely sense what we want to measure [16, 18].

Some sensors that are used on robots are ultrasonic, tactical, vision and force sensors [16-18]. The expenses to get the best and/or most accurate ones can get very high [15]. However, in the case of ultrasonic sensors, very expensive sensors are not absolutely necessary. For example, crude ultrasonic sensors will not always get the exact image. Yet, due to a soft computing paradigm like fuzzy logic, Tunstel et al explained how expensive and accurate sensors are not absolutely necessary [19, 20]. This is because fuzzy logic uses imprecision and uncertainty in order to get to a conclusion [13, 14, 19, 20].

Hence, a fuzzy logic controller can use linquistic variables in its execution [13, 14, 19, 20]. The fuzzy logic controller uses IF-THEN statements in testing for a change in error. In the IF-THEN statement, the IF part is the antecedent while the THEN part is the consequent. As stated earlier the output of the controller is generally the input to the plant.

Let's consider some problems that may exist due to computer errors.

1. Vehicle is not in its proper orbit,

2. Vehicle is not going at the desired speed,

3. Vehicle is not at the proper thrust in the beginning,

4. Less than adequate or poor communication between mission control and outer space,

5. Robotic arm does not function properly (angle and speed),

6. Improper or bad landing,

7. Temperature on the inside is not at its desired value,

8. Vehicle is not going in the proper direction,

9. Poor circulation of air inside the vehicle,

10. Entry into Earth's atmosphere will be a concern,

11. Cameras or vision sensors do not rotate (to the intended image) or function properly,

12. Cameras do not get the proper image for the crew to see,

13. Engine temperature is not at its proper value,

14. Sensors that give the speed, inside temperature, coordinates, engine temperature, etc. do not function properly.

Some of these items are related like numbers seven, nine and 14. In essence it is possible to partially fix some other problems while one is being fixed. It depends on the relation of one problem to another.

Let's take a brief look at number seven. For instance, someone sets the inside temperature, where the astronauts are, to (Let's say.) 78°F. Let's say that the controller is a fuzzy based one. Let the membership functions (a graphical representation of a fuzzy set) for measured temperature are COLD, COOL, WARM, and HOT. Let the temperature of 78°F be considered WARM. Any actual temperature that is above or below, especially if the temperature is significantly above or below 78 degrees, would

cause the controller to act to where the actual output, or temperature, would become more in line with the desired output, or temperature. So if the temperature's actual output was at 68, a human operator could come up with the following IF-THEN statement in their mind: IF ACTUAL TEMP is COOL, THEN AIR RELEASED is WARM. But the controller could have a command such as: IF error is "positive" AND change in error is "positive" THEN change in input is "positive." For more on fuzzy logic control see the works by Ross in [13] and Langari and Yen in [14].

The previous paragraph was an example on how the fuzzy controller (as stated before) corrects the error that exists in the closed loop transfer function. For instance, if a vehicle is moving in a direction too far to the left, there are commands, especially in fuzzy logic control, that can steer towards a more rightward direction. Consider this. Let's say that the steering is set up in angles. Let a direction of zero be directly in front, the negative angles be to the left, and the positive angles be to the right. If the vehicle is suppose to move in a direction that is straight ahead but is moving to the left, then a command can state that the vehicle should turn in a rightward direction, or a positive angle direction. Hence, the vehicle would be moving in the correct direction.

Conclusions and Recommendations

A strong or closed link between error correction and control systems was not determined in this research. In his dissertation in [21], Tsao applied the use of fuzzy sets in order to make fuzzy the observations for wind and current. Tsao also talked about error detection modules looking for inconsistencies between something modeled and observed. But the object that was modeled and observed had to do with marine oil spills.

In robotics control and sensing are affect by the inaccuracy and errors. Also, there is uncertainty about the environment's geometry, which Bruce calls the model error in [22]. He also talks about Error Detection and Recovery (EDR) strategy is, loosely interpretated, when a strategy gets to a reachable goal that is recognized but yet issues failure. However, as was stated earlier and by Tunstel and others, soft computing paradigms like fuzzy logic and neural networks have been used in robotics to overcome the uncertainty and imprecision, especially of what is being sensed, that may occur through the sensors' readings [19, 20].

Recommendations

As was stated before, the desire was to see how fuzzy logic control could directly enhance error correction and detection and vice versa. But despite the lack of findings, there are some things that one could consider.

1. One should keep a stable control system for obvious reasons. An unstable control system could cause system malfunctions, bad data, and very inaccurate performance by the system [11-15]. Consider this. If the control system for the temperature is not stable, the chances would be very low that one could get the accurate readings. In other words the reading of the output value will not be accurate. And the operator would not know what the actual temperature is.

2. As was stated earlier, use of an adequate control system, especially with the use of fuzzy logic, may allow one to use inexpensive sensors [19, 20]. With the use of fuzzy logic, one does not have to worry too much about the imprecision and uncertainty of the images sensed by the sensors. Since fuzzy logic uses approximation and not the absolute analysis of crisp or classical logic,

imprecision can actually be beneficial in stability or giving commands. (This makes fuzzy logic more flexible.) The reduce cost in sensors should help in reducing the cost in the overall equipment.

3. Included with the cost, one should see if the type of control system will have an affect on any other system or algorithm. This includes error correction and detection, parity and checksum. While fuzzy systems may allow for inexpensive sensors, the type of controller and algorithm can influence the hardware. What effect will the type of hardware have on error correction? If the effect is negative, how will one have to change the control system? Or will there be an effect at all? Will any other system have to be changed because of the controller or control system? These are some questions that may have to be answered.

4. In relation to numbers two and three, the issues of the controller and hardware can be related. Problems that can arise are the rewiring and replacing of the electronics. Other issues dealing with analog controllers can be difficult, clumsy and inexpensive. The availability of the circuit is a concern as well. But Jacob stated in [15] that digital control can solve these problems with less cost while introducing the microprocessor, single-chip microprocessor and intelligence in the manufacturing process. Ross in [14] and Yen and Langari in [13] showed that intensive mathematics are not always, if ever, needed while using fuzzy logic. In essence the choice of the type of controller is important when it comes to the cost and hardware as well at the stability of the system. Some of the questions in number three can apply hear as well.

These recommendations for the control systems were basically stated in order to reduce the chances of system malfunction, damaged or last data or worse life threatening situations [3]. There were stated so that the cost of operation and the parts are reduced. While there may not be the strong link between error correction techniques and control system, fuzzy logic and fuzzy logic design, it is hoped that the upkeep of the control systems will not aversely affect the other systems, techniques or algorithms.

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