UPDATED ELECTRONIC TESTBED SYSTEM

by

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Introduction

As we continue to advance in exploring space frontiers, technology must also advance. The need for faster data recovery and data processing is crucial. In this, the less equipment used, and lighter that equipment is, the better.

Because integrated circuits become more sensitive in high altitude, experimental verification and quantification is required. The Center for Applied Radiation Research (CARR) at Prairie View A&M University was awarded a grant by NASA to participate in the NASA ER-2 Flight Program, the APEX balloon flight program, and the Student Launch Program. These programs are to test anomalous errors in integrated circuits due to single event effects (SEE).

CARR had already begun experiments characterizing the SEE behavior of high speed and high density SRAM's. The research center built a error testing system using a PC-104 computer unit, an Iomega Zip drive for storage, a test board with the components under test, and a latchup detection and reset unit. A test program was written to continuously monitor a stored data pattern in the SRAM chip and record errors. The devices under test were eight 4Mbit memory chips totaling 4Mbytes of memory.

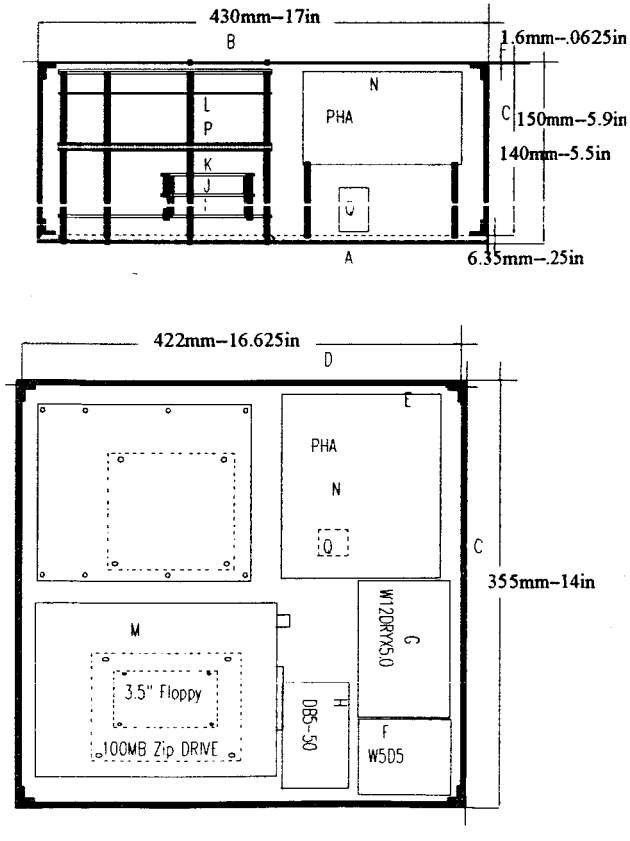
CARR was successful at obtaining data using the Electronic TestBed System (EBS) in various NASA ER-2 test flights. These series of high altitude flights of up to 70,000 feet, were effective at yielding the conditions which single event effects usually occur. However, the data received from the series of flights indicated one error per twenty-four hours. Because flight test time is very expensive, the initial design proved not to be cost effective. The need for orders of magnitude with more memory became essential.

Therefore, a project which could test more memory within a given time was created. The goal of this project was not only to test more memory within a given time, but also to have a system with a faster processing speed, and which used less peripherals. This paper will describe procedures used to build an updated Electronic Testbed System.

Objectives

Figure 1 illustrates a brief diagram of the current testbed system. It is composed of the following components listed on A through C. This system was secured in the Superpod area of the ER-2 shown in figure 2.

However, the new testbed system will be secured in the ER-2's System 20 Pod area also shown in figure 2. Also, the new system will be installed in a cylinder tube, shown in figure 3.



NOTE: TOP AND FOUR SIDES ARE TO BE A UNIT REMOVABLE FROM THE BASE

SYSTEM COMPONENTS

THE BOX

A Base 14"X17" X .25" Aluminum
B Top 14"X17"X.0625" ALUMINUM
C 2 SHORT SIDES 14"X5.5"X.1875" ALUMINUM
D 2 LONG SIDES 16.625"X5.5"X.1875" ALUMINUM
E ANGLE BRACES .5"X.5"X.125" ALUMINUM

POWER SUPPLYS

F ABBOTT W5D5 2.5"X3.5"X4.0625" 2.7lb
G ABBOTT W12DRYX5.0 3.5"X4.5"X4.25" 2.7lb
H ACOPIAN DB5-50 3.5"X2.5"X1.85" 3lb

CIRCUIT BOARDS

I SINGLE BOARD COMPUTER—ADVANTEC 4860 8"X5"X1"
J IO BOARD--DIAMOND SYS. F07149 3.55"X3.775"X.625"
K SCSI-104--ADASTRA SYS. mod800-400 3.55"X3.775"X.625"
L CUSTOM SURFACE MOUNT TEST BOARD 8"X5"X1"
NOTE STACK WEIGHT <1lb

ADDITIONAL DEVICES

M OPTICAL DRIVE--MOUNTAIN OPTECH P/N 2436-00 9.75"X5.75"X3.5" 2lb 13.4oz

---

N CUSTOM PULSE HIEGHT ANALYZER 6"X6"X3"
O 2 CR39 PLASTIC SHEETS 8"X5"X.0625"
P POLYETHYLENE SHEET 8"X5.75"X.25"
Q LATCH-UP PROTECTION RELAY 1.42"X1.1"X.85"

Figure 1

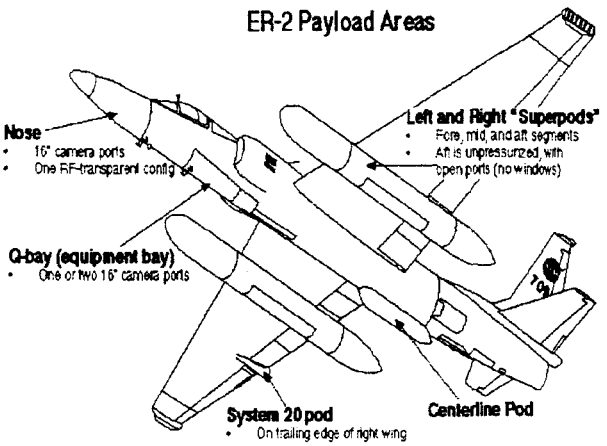


Figure 2

Its normal cruise profile of flying at high altitude of (60 to 70) thousand feet will yield conditions necessary for Single Event Effects with the aircraft operating above 90% of the earth's shielding atmosphere.

Cylinder, which will hold new EBT, will be secured in System 20 Pod of ER-2.

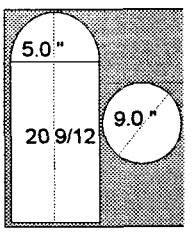


Figure 3

Goals

The following goals were set in order to find ways of accomplishing the objective of upgrading the current Electronic Testbed System:

- Conduct a market search for Pentium III motherboards and develop a selection process.
- Conduct a market search for Random Access Memory (RAM) Modules – SRAM & DRAM.
- Develop a design for the upgrade to the ETB.
- Evaluate the ETB software system.
- Recommend upgrades to the ETB software.
- Develop the design for the software upgrade.
- Integrate the Pentium III and upgraded software.
- Document the upgraded hardware and software.
- Conduct post-operational tests on the Pentium III system.

Market search for PC/104 Motherboard.

The research process began with a market search for an upgraded PC/104 motherboard with a pre-installed Intel Pentium III microprocessor. This was selected because it was one the fastest processors on the market. The PC/104 motherboard also needed to have a SCSI interface. The reason for the SCSI interface will be explained later.

What are PC/104 motherboards?

PC/104 based systems are used in a variety of places. For example, they are used in factories, laboratories, processing plants, vehicles, and almost anywhere devices must be controlled by a programmable computer. They are small systems and usually have low power requirements so they are great for applications that simply do not have the space for a full-blown desktop PC. Additionally, PC/104 systems are designed to be more rugged than desktop systems. Building a system using PC/104 modules usually costs more than a commercial PC, but usually less than a rack mount ISA bus system.

The PC/104 form factor motherboard was first developed by Ampro Computers in California in the late 1980's. The specification was published in 1992 in order to enhance popularity. Over 150 vendors manufacture PC/104 compatible products including controller cards, software, and accessories. The PC/104 Consortium was established to maintain the specifications, publish resource guides, participate in standards activities, and to promote PC/104 at trade shows and news releases.

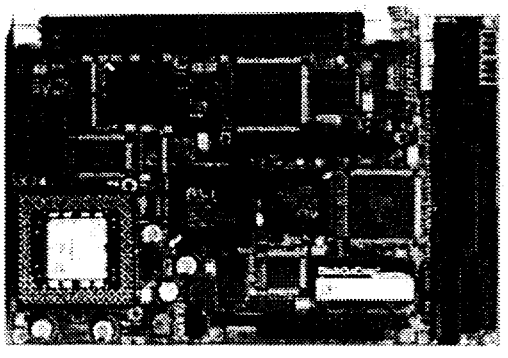
PC/104 gets its name from the popular desktop personal computers initially designed by IBM called the PC, and from the number of pins used to connect the cards together (104). PC/104 cards are much smaller than ISA-bus cards found in PC's and

stack together which eliminates the need for a motherboard, backplane, and/or card cage. Power requirements and signal drive are reduced to meet the needs of an embedded system. Because PC/104 is essentially a PC with a different form factor, most of the program development tools used for PC's can be used for a PC/104 system. This reduces the cost of purchasing new tools and also greatly reduces the learning curve for programmers and hardware designers.

There are many modules available for the PC/104. This includes common functions like CPUs, Serial I/O ports, and Video Controllers; but also more exotic modules like GPS receivers, vehicle power supplies, wireless communications. A stack of PC/104 modules can be attached as a component of a larger circuit board, or simply put in a small enclosure for stand-alone operation.

Which PC/104 board was selected?

After doing a comprehensive market search for the updated PC/104 motherboard, it was decided that the CARR research center would use the vendor, Toronto Microelectronics Inc. The vendor 5811 PC/104 motherboard, shown below in figure 4, can be manufactured using the following configurations listed in Table 1



TME 5811 PC/104 Board with SCSI Interface

Figure 4

CPU

- Supports Intel low power MMX processor with 1.9V Core and 2.5V I/O
- Supports Intel MMX Pentium and AMD K6, K6-2, K6 2/3D
- Processor speeds of 166, 233, 266, 300, 333, 400, 450 MHz.
- 66, 75, 83 or 100 MHz system bus speed

CPU Production Selection

- Pentium 166 MHz MMX
- Pentium 233 MHz MMX
- Pentium 266 MHz MMX
- AMD K6-2 333 MHz
- AMD K6-2/3D 400 MHz

CHIPSETS

- Alladin V Core
- C&T B69000 / B69030 video
- Intel 82558 10/100Base-T
- SYMBIOS 53C875 SCSI

THERMAL MANAGEMENT

- Overheat protection
- Overheat slow down
- Thermal controlled CPU & system fan connectors

DRAM MEMORY

- Two 168-pin DIMM sockets
- Supports up to 512 MB of SDRAM
- Supports 3.3V EDO or SDRAM
- Supports non-parity, parity and ECC

CACHE MEMORY

- Standard 512 KB L2 Synchronous Burst Cache.

FLASH MEMORY / SOLID STATE DRIVE

- M-System Disk-On-Chip (DOC) with up to 144 MB of Flash with built-in EDC/ECC
- Support DOS, Windows NT, Window CE, Windows 95, QNX, pSOS and VxWorks OS

I/O SPECIFICATIONS: GENERAL PURPOSE STANDARD I/O PACKAGE:

- 7 DMA Channels (8237 compatible).
- 15 Interrupt channels (8259 compatible).
- 50 PPM accuracy and Y2K compliance
- Built-in removable lithium battery pack supports up to 10 years
- Floppy controller includes 2.88 Mbyte support on 2x17 shrouded header.
- three 16C550 RS-232C COM port with FIFO buffering and 15KV ESD protection.
- One 16C550 RS-232C COM port with FIFO buffering and 15KV ESD protection with optional RS-485.
- Parallel Printer port with ECP/EPP support.
- Dual independent EIDE supports Ultra 33 DMA
- Supports up to 4 drives on 2x22
- PS/2 mouse and keyboard ports on 6-pin mini DIN connector. Keyboard inhibit port
- Two USB Ports.
- On-board 2x8 shrouded header supports keyboard, mouse, keyboard inhibit, reset and external buffer.

ULTRA SCSI

- Ultra SCSI interface supports up to 40 MB/s data transfer rates using SYMBIOS 53C875
- Supports fixed disk, removable media drives, SCSI printer, rewrite optical drives, CD-ROM drives, tape drive, DAT, MO, scanner, Photo-CD support and other

OPERATING SYSTEM

- Windows 95, Windows 98, WindowsNT 4.0, UNIX, SCO UNIX, LINUX, LYNX, VxWorks, QNX, BANYAN, NOVELL, OS/2, LANtastic and more*

TOUCHSCREN

- DYNAPRO-compatible touch-screen interface supports 4, 5 or 8 wires touch-screen

EMBEDDED PC SYSTEM FEATURES

- Watchdog timer with software or hardware disables
- 128 bytes of SEEPROM for CMOS data backup
- 128 bytes of SEEPROM for manufacturing information
- 256 bytes of SEEPROM of user
- Up to 64 KB of extension ROM using on-board programmable flash memory for user firmware
- AT-compatible Real-Time clock with 50 PPM accuracy
- 15KV ESD protection on serial ports
- Power Failure detection circuitry
- 7 year Lithium battery for Battery–Backed SRAM
- 5 Year product availability support (subject to component availability)
- Warranty of product consistency

EMBEDDED SYSTEM BIOS FEATURES

- Full AT compatible BIOS.
- BIOS stored in Flash EPROM to faciliate remote firmware update capability
- Optional no-fail boot, Fast Boot, and Secured-boot
- Optional batteryless operation.
- Optional Customer sign on message at boot up
- Advanced firmware setup utility for system parameters and I/O configuration
- Power saving mode with "green PC"

BUS

- 16-bit Pc/104 interface for optional sound, CompactFlash, Battery-Backed SRAM, additional serials ports, and additional network interface
- 32-bit PCI bus PC/104-Plus bus.
- Supports 33 MHz PCI bus clock

OPTIONAL ON-BOARD I/O FEATURES:

- Video Interface
- On-board Flat Panel & CRT display interface using C&T 69000 with optional C&T B69030
- Support for LCD monochrome, S/S and D/D STN, TFT, EL and gas plasma Flat Panel displays to 1280x1024 resolution.
- Supports 3.3V or 5V Flat Panel display.
- Supports up to 36-bit LCD on both TTL and LVDS interface.
- Capable of driving high resolution LCD at distances up to 20'
- Supports ZV port
- 2 MB of SDRAM display memory on C&T B69000
- 4 MB of SDRAM display memory on C&T B69030

Table 1

Table 1 continued

NETWORK FEATURES
- Intel 82558 Device
- 32-bit PCI local BUS interface
- Supports 10/100Base-T/TX
- Supports PCI BUS Master
- Supports Remote Boot-ROM for diskless system
- Supports IEEE 802.3 standard
- Supports Ethernet standard
- Configuration information stored in EEPROM for jumperless configuration
- Device Drivers for DOS/Windows, Windows NT, Windows95, SCO UNIX, UNIX, Novell, OS/2 and more...

DIMENSIONS
- 5.75" X 8" EBX form factor

ENVIRONMENTAL Operation
- Temp: 0° C to 65° C @ no airflow (with CPU fan sink only)
- -40° C to +80° C available upon request
- Humidity: 5% to 90% non-condensing

STORAGE
- Temp: -40°C to 95°C
- Humidity: 5% to 95% non-condensing.

Note: Please refer to TME's web-site for more information at http://www.tme-inc.com.

The TME motherboards with Intel Pentium 266 MHz MMX and AMD K6-2/3D 550 MHz were selected. They were the faster processors by Intel and AMD which came on PC/104 motherboards at the time. Intel Pentium III processors were not available on the PC/104. For now, they only come on the standard personal computer motherboards. The selected motherboard also can with Dual Ultra DMA/33 EIDE and floppy interface, four serial ports, one parallel port, and two USB ports.

The major advantage of the TME PC/104 motherboard that we selected is the 16Mbyte fully bootable single-chip flash disk. This on board solution is called *DiskOnChip 2000* made by M-Systems. It has high performance read/write for data reliability. As a result, this alleviates the need for the 1.44M floppy drive, which was necessary on the previous TestBed system to run the operating system. The previous system was started by a Microsoft Windows 95 boot-disk. The updated system uses the full version of Dos 6.0.

DiskOnChip 2000

Figure 5

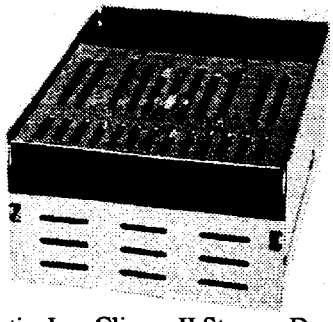
The *DiskOnChip 2000*, shown above in figure 5, is a unique data storage solution. It offers cost effective data storage beyond that of traditional hard disks. Because the *DiskOnChip 2000* is integrated into PC/104 motherboard, it allows more space in for additional storage devices.

It is a perfect solution for running the application program used for retrieving data from Single Event Effects on DRAM and SRAM storage devices. The old Test-Bed uses the Iomega Zip Drive to run TestBed software program, and result data. The Disk on Chip, however, is more cost effective in reducing the need for a 1.44M floppy Drive and omega Zip Drive. It can boot-up the system, run the TestBed program, and store result data.

Storage Solution(s)

DRAM Storage-Device

The reason the PC/104 motherboard with a SCSI interface was chosen is because of the DRAM Storage device. This device is the primary Device Under Test (DIT) for the new TestBed system. The DRAM storage device holds the high capacity storage need to test orders of magnitude more memory. After doing a comprehensive search of a DRAM storage device, it was decided to use the Curtis, Inc. Clipper(II) storage device. This device can hold up to 8.6GB of memory. This capacity of memory is significantly larger than the 8Mbytes tested on the previous Test-Bed system.



Curtis, Inc. Clipper II Storage Device

Figure 6

The Clipper II, shown above, in figure 6, is a "plug and play" device. Thus, it is easy to install, and appears on the system like other standard hard drives. It is available with Ultra2 SCSI interface, which makes the Clipper II a flexible device for the TME PC/104 motherboard. Table 2 lists the data sheet for the Clipper II storage device.

Specifications Description
- Desktop/Rackmount Solid State Disk
- Interface: Ultra2SCSI or FibreChannel

Models and Capacities
Ultra2 SCSI Interface Models
- CLIP2-DSK-1GB.....1GB
- CLIP2-DSK-2GB.....2.1GB
- CLIP2-DSK-3GB.....3.2GB
- CLIP2-DSK-4GB.....4.3GB
- CLIP2-DSK-8GB.....8.6GB

Physical Specifications
Desktop Models Ultra2SCSI/FibreChannel
- Height.....6.7"/ 12.4"
- Width.....7.5" / 9.5"
- Depth.....12" / 12.3"
- Weight.....20 / 25 lbs

Reliability
- MTBF.....>1,000,000 Hours
- Integrated ECC Memories.....72bit (64Data/8ECC) modified Hamming Code meets/surpasses server memory requirements

Environmental Characteristics
- Operating Temperature.....0 to 50°C
- Non-Condensing Humidity....10 to 90%
- Altitude.....10000 ft.

High Performance
- Access Time.....60mS
- I/O (transactions/sec).....>10000
- Interface Transfer Rate (U2SCSI).....80MB/sec
- Data Transfer Rate (sustained).....>68MB/sec

Power Requirements
- 115/230V AC 65W

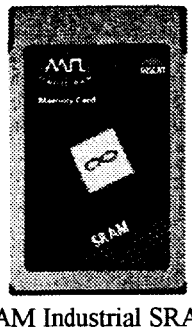
Data Retention and Power Management
- External AC/DC Backup Power Supply
- Integrated Lead Acid Battery and Charger: minimum 2 hours data retention in battery backup mode
- Optional internal mechanical disk backup available

Table 2

SRAM Storage Cards

The use of SRAM card is an alternative way of recording Single Event Effects. Unlike the DRAM storage device, the SRAM cards do not need to be connect to tests system during test flight. The SRAM cards act as the secondary (DUT). Data files are stored on the devices before the test flight. The device data files are not be evaluated until the flight test is completed.

After doing a comprehensive search of SRAM storage cards, it was decided to use the MagicRAM Industrial 8Meg SRAM Memory cards, shown in figure 7. They are packaged in a PCMCIA Type II housing with x8/x16 PCMCIA Standard Interface. The cards are based on advanced CMOS technology, providing very low power and reliable data retention characteristics. The MagicRAM Industrial SRAM cards contain a rechargeable lithium battery and recharge circuitry, eliminating the need for replaceable batteries. They have an extended battery backup time of 2.5 months. The recharge feature eliminates the danger of battery failure and data loss during critical times, as well as risk of damage to the host and module components when batteries are removed or inserted.



MagicRAM Industrial SRAM cards

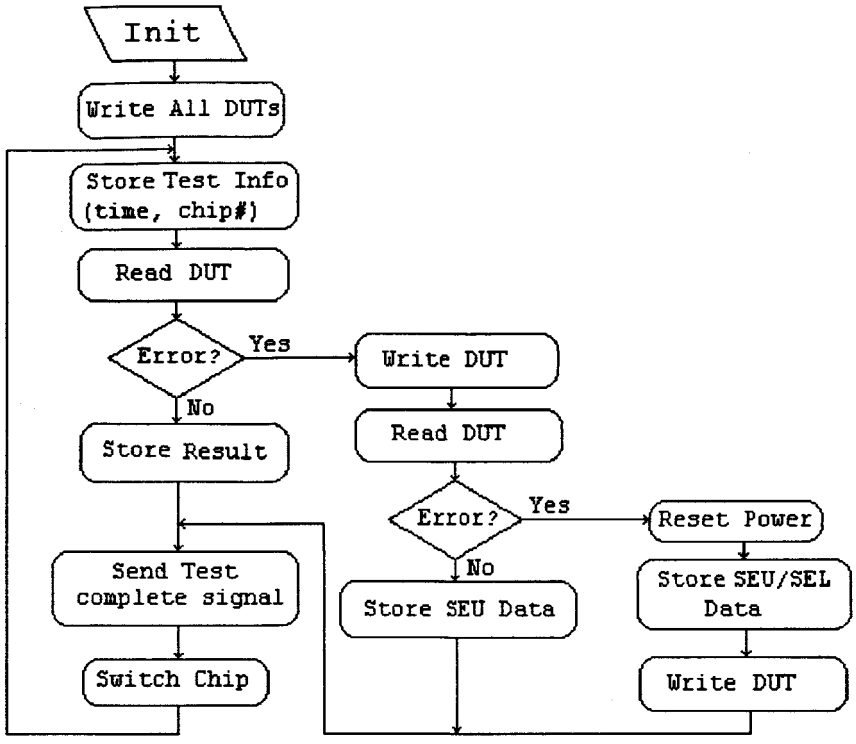
Figure 7

The MagicRAM Industrial SRAM card battery is encased in an ultra-sonically welded housing, thereby offering greater resistance to shock and vibration. They can operate in standard (0°C - +70°C) and extended temperature (-40°C - +85°C).

The SRAM cards will be stacked on top of one another in the test tube. Therefore 20 cards will provide 160Meg of additional memory to SEE evaluation process. After being flown at high altitudes, the pre-flight stored image/pattern will be compared to the original stored on a computer at CARR.

Software Program

In order to make the update Test-Bed computer work efficiently with the DRAM and SRAM memory devices, a software program was written. The updated test program design was similar to the previous test-bed program shown below in Figure 8.



ER-2 Memory Test Flow

Figure 8

Figure 7 shows the flow chart of the test program, which was developed using the C programming language. In this program, time is continuously recorded to the output file. The data pattern is written to all of the Device Under Test, in this case, 8 4Mbit Chips. Then the test program checks each chip for errors. When an error is detected, the data pattern is rewritten to the DUT and checked again to identify any radiation effects (Single Event Upset/Single Event Latchup) to the DUT, or even the testing device itself. If there is an error in the testing device, the power is reset.

In writing the program, a few things warranted special consideration. The updated Test-Bed system contained integrated circuits which were vulnerable to Single Event Effects. As a result, a WatchDog-Timer was required. This unit receives a signal from the CPU module at certain intervals indicating that the test

program is functioning correctly. When the CPU module fails to send the signal, this indicates that a Single Event Effect occurred in the TestBed system. This detection causes the TestBed system computer to restart. Each time the test program is cycled, it stores the time and begins processing. The program does not end until the power is turned off or manually interrupted.

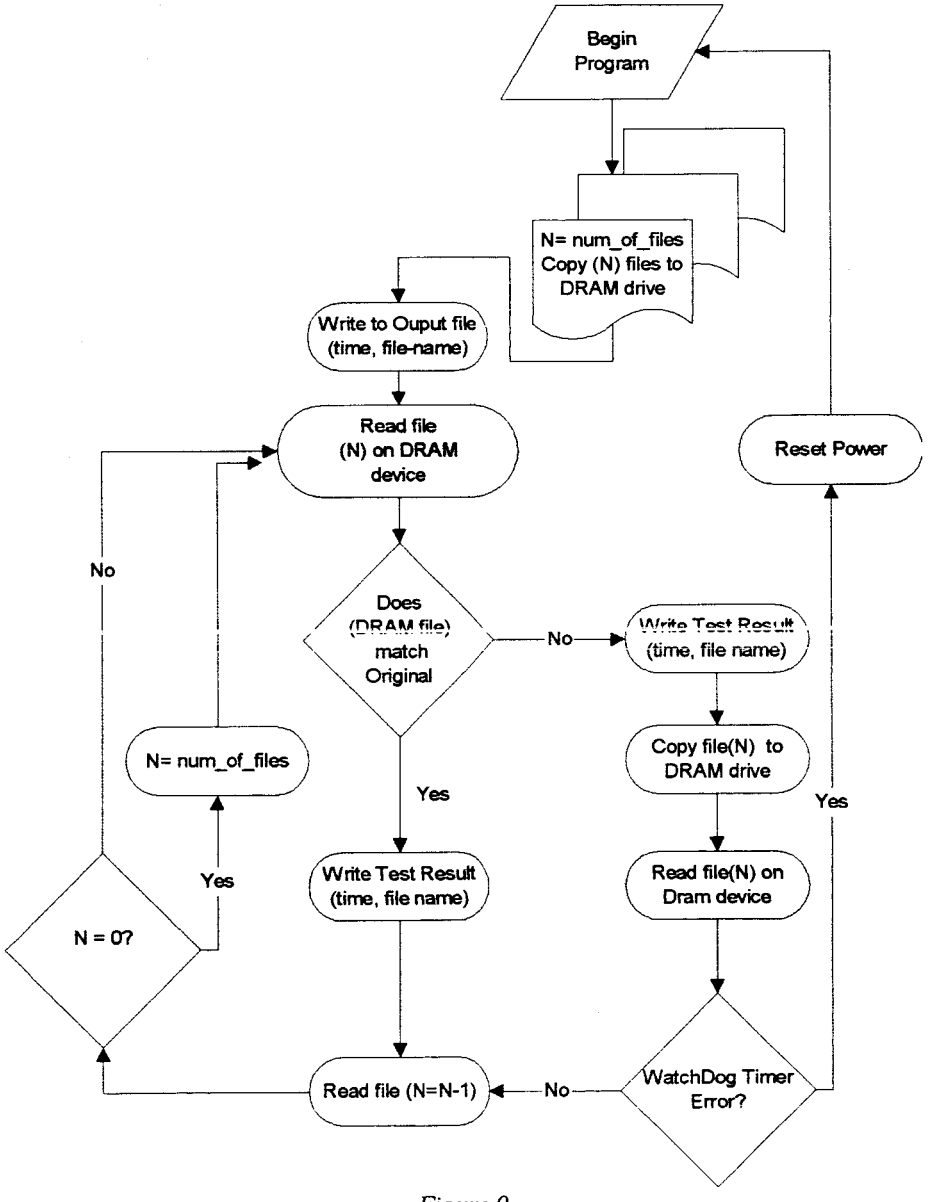


Figure 9

Figure 9 illustrates updated test program. Throughout the program, the time continually recorded to the output file. Multiple data files are copied from the Disk-on-Chip to the DRAM storage device. These files are repeatedly compared to the original, just as the each chip was tested for errors in the previous Test-Bed program. In the new system, when an error is detected the data is rewritten to the file and checked again to verify if a Single Event Effect has occured, or if there is an error in the testing device. If an error is identified by the WatchDog Timer, the testing device power resets. This process continues to repeat throughout the test flight.

Figure 10 shows the flow chart of the updated test program for the SRAM storage chips. In this program, data files are read into the storage device before the flight test begins. However, unlike the two programs mentioned previously, data files are not read until the end of the test flight. Therefore, there is no need for theses devices to be connected throughout the test flight. Data can then be compared to its original files stored in the research center.

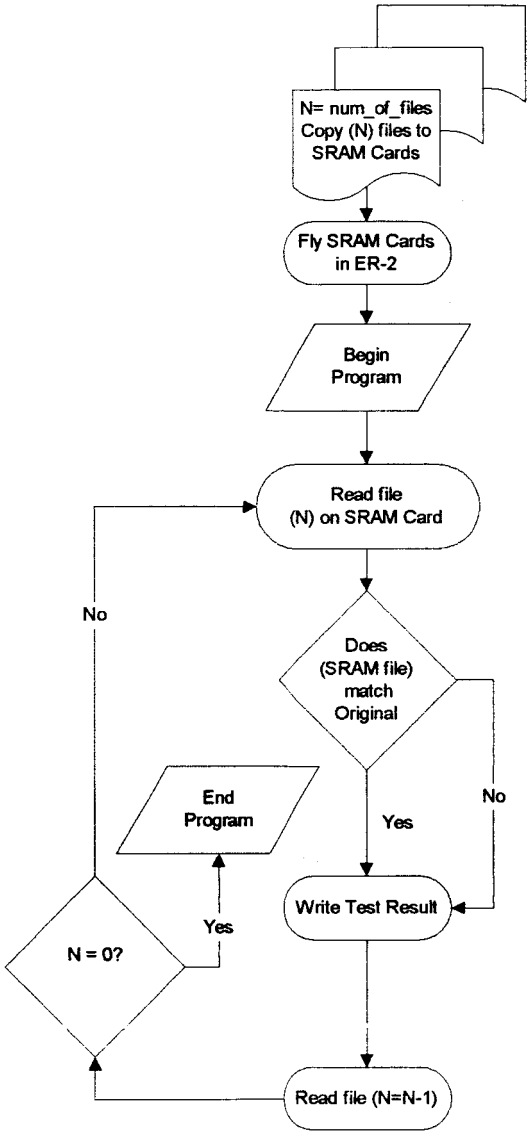

N= num_of_files
Copy (N) files to
SRAM Cards
Fly SRAM Cards
in ER-2
Begin
Program
Read file
(N) on SRAM Card
Does
(SRAM file)
match
Original
No
Yes
No
End
Program
Write Test Result
Yes
N = 0?
Read file (N=N-1)

Figure 10

Conclusion

This projected was designed to accomplish two objectives. First, to update the current TestBed system, and second, to test orders of magnitude more memory. These objectives were accomplished by setting the following goals:

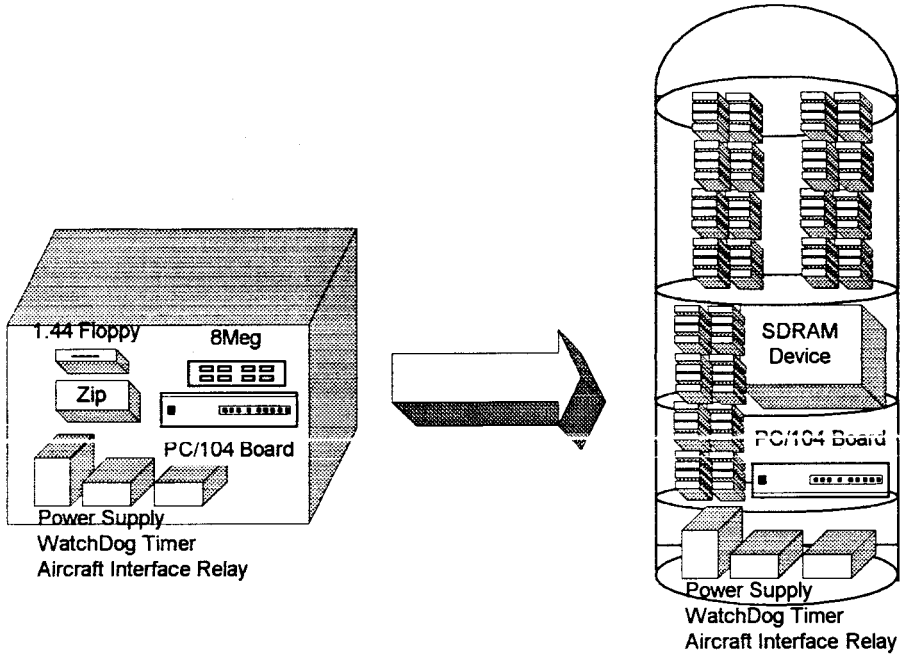
- Conduct a market search for Pentium III motherboards and develop a selection process.
- Conduct a market search for Random Access Memory (RAM) Modules – SRAM & DRAM.
- Develop a design for the upgrade to the ETB.
- Evaluate the ETB software system.
- Recommend upgrades to the ETB software.
- Develop the design for the software upgrade.
- Integrate the Pentium III and upgraded software.
- Document the upgraded hardware and software.
- Conduct post-operational tests on the Pentium III system.

Most of the goals were met. Unable to find a Pentium III processor, a substitution was made with the fastest processor available on a PC/104 motherboard. This processor was the AMD K6-2/3D 400 MHz. The motherboard, was created by Toronto Microelectronics Inc,(TME). The flask disk chip on the TME motherboard, allowed the upgrade of the current system significantly. The DiskOnChip storage device reduced the need for a 1.44M floppy drive, and a 100M Iomega Zip Drive. As a result, this yielded more space for Devices Under Test.

In conclusion, there was success in locating SRAM and DRAM devices. However, both devices are still on order. A final design and integration of the Electronic Test Bed software upgrade will not be complete until the storage devices are received. The current software has been evaluated, and upgrades have been recommended. This

information will be helpful in continuing the Electronic TestBed project. Figure 11 illustrates the updated TestBed System once all components have been complete integrated.

After all equipment is received the, a post-operational test can be conducted on the system at the Texas A&M University Cyclotron Institute and the EBT can then be run on the ER/2. All work to date has been documented and placed in the Center for Applied Radiation Research Library.



Updated TestBed System with Integrated Components

Figure 11

Acknowledgements

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Dr. Kelvin Kirby	Center for Applied Radiation Center Research
Kurt Kloesel	Dryden Flight Research Center

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http:\\www.m-sys.com
http:\\www.tme-inc.com