The Development of Design Tools for Fault Tolerant Quantum Dot Cellular Automata Based Logic

Curtis D. Armstrong and William M. Humphreys

Abstract—**We are developing software to explore the fault tolerance of quantum dot cellular automata gate architectures in the presence of manufacturing variations and device defects. The Topology Optimization Methodology using Applied Statistics (TOMAS) framework extends the capabilities of the A Quantum Interconnected Network Array Simulator (AQUINAS) by adding front-end and back-end software and creating an environment that integrates all of these components. The front-end tools establish all simulation parameters, configure the simulation system, automate the Monte Carlo generation of simulation files, and execute the simulation of these files. The back-end tools perform automated data parsing, statistical analysis and report generation.**

***Index Terms*—Cellular automata, Design automation, Fault tolerance, Monte Carlo methods, Quantum Dots.**

I. Introduction

Quantum dot cellular automata (QCA) represent an alternative paradigm to transistor-based logic [1], [2]. The operation of QCA logic gates has been verified using large lithographically defined devices [3], [4]. Due to their large size, these devices had to be operated at cryogenic temperatures in order for the quantum mechanical effects to be observed. To achieve room temperature operation, the size of the quantum dots, and therefore the QCA cell, has to be reduced significantly. The proper operation of the simple QCA gates is strongly dependent on the relative alignment of the QCA cells [5]. At nanometer scales, it is extremely difficult to achieve the required manufacturing tolerances. In order for QCA-based logic to be viable, QCA gate architectures that are tolerant of manufacturing variations and device defects must be developed.

The block majority gate (BMG) [6] utilizes the collective behavior of a 2D array to provide the functionality of a majority gate in spite of manufacturing variations and device defects (Fig. 1). However, this technique imposes an area penalty. Throughout this paper we use the optimization of the BMG architecture as the basis for our examples and descriptions.

Assessing the fault tolerance of QCA gates requires systematic statistical analyses. The current version of the A Quantum Interconnected Network Array Simulator (AQUINAS), developed by Lent *et al* [7], does not include tools to support these evaluations. The Topology Optimization Methodology using Applied Statistics (TOMAS) framework extends the capabilities of AQUINAS to enable these investigations.

II. Defect Modeling

A. Array Defect Types

The topology of an ideal QCA array is analogous to a two-dimensional crystal lattice. The unit cell of this lattice is a rectangle with a QCA cell at its center. The same defects that affect the properties of the crystal lattice [8], [9] also affect the performance of the QCA array (Fig. 2). A QCA cell missing from the array is equivalent to a lattice vacancy. A QCA cell shifted from its ideal location is analogous to an interstitial defect. A QCA cell stuck in a single polarization is comparable to a dopant in a crystal lattice. In a crystal, a dislocation can be thought of as an extra lattice plane inserted into the crystal that does not extend throughout the crystal. With a little imagination, a QCA cell that is rotated relative to the other cells in the array is akin to a dislocation in a crystal lattice.

B. Defect Modeling

Array defect types are modeled as either population densities or physical deviations from the ideal array. Population densities describe the distributions of vacancies, dopants, and dislocations in a sample of QCA cells. Physical deviations from ideal array values describe the positions of QCA cells in the x-y plane, the polarization of dopants, and the angle of rotation of dislocations relative to the row axis.

The physical processes that create these defects are inherently statistical. Therefore, all defects are modeled as independent random variables specified by a user-selected probability density function, mean, and variance. Consequently, statistical techniques are required to analyze the effects of these array variations on QCA gate performance.

Manuscript received August 4, 2003. This work was supported by the NASA Langley Research Center Creativity and Innovation research program.

The authors are with the National Aeronautics and Space Administration Langley Research Center, Hampton, VA 23681 USA (phone: 757-864-3701; fax: 757-864-8550; e-mail: curtis.d.armstrong@ nasa.gov). .

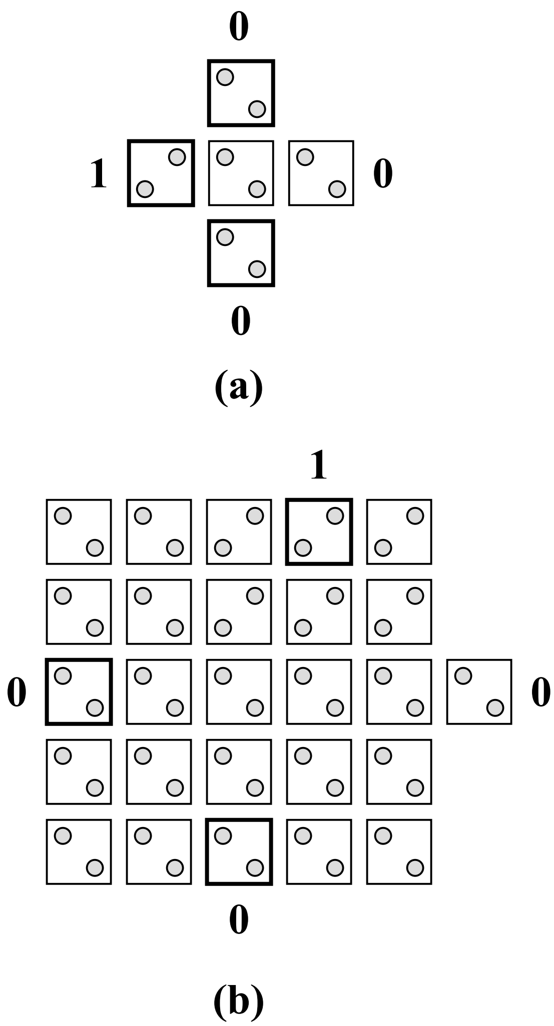

Figure 1 QCA majority gate (a) ideal (b) block

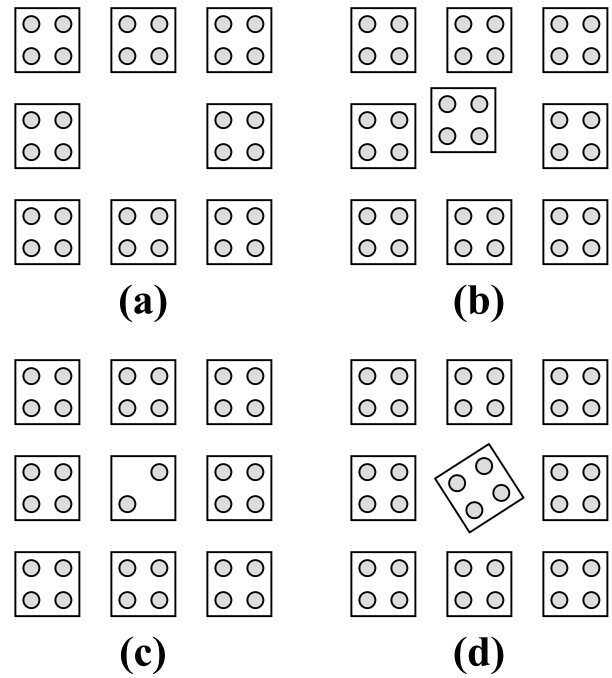

Figure 2 QCA array defects (a) vacancy, (b) interstitial, (c) dopant, and (d) dislocation

III. TOMAS AQUINAS

Statistical evaluation of the robustness of a gate topology requires a large number of simulations with well-controlled properties. AQUINAS provides no support for the configuration and generation of multiple simulation input files. TOMAS extends the capabilities of AQUINAS by creating a framework that allows the integration of external configuration, control, and analysis tools with AQUINAS (Fig. 3).

A. Graphical User Interface

The TOMAS AQUINAS graphical user interface (GUI) provides a common interface to all of the tools integrated into the framework. This GUI supersedes the interfaces to all of the other tools incorporated into TOMAS AQUINAS. This GUI provides an integrated environment to describe the array topology, configure the simulations, initiate and monitor the simulations, analyze the data, and document the results. The GUI captures all user inputs and passes them to the appropriate function.

B. Sim Generator

Sim Generator (SG) is an AQUINAS input file generation system. Via the GUI, SG acquires all of the simulation configuration information required by AQUINAS. In addition, SG acquires all of the information required to model array imperfections and all inputs required by the Monte Carlo generator. All of the signals required by the array are defined using SG. Based on user inputs, an interactive graphical diagram of the array is generated. This diagram is used to specify array input(s) and output, and assign signals to the cells. SG uses Monte Carlo techniques to apply the defects to an ideal array and generates a set of simulation input files.

C. Condor

Condor® is a workload management system for computationally intensive jobs [10]. Condor provides a job-queuing mechanism, a scheduler, a priority scheme, resource monitoring, and resource management. Condor can be used to manage a group of dedicated computational nodes, such as a Beowulf cluster, or to build a grid computing environment.

Condor provides an extremely flexible workload management system that is easily configured for the user's computational system. Via the GUI, users submit jobs to Condor. Condor places them in a queue, assigns the jobs to computational nodes based upon a priority resource management policy, monitors their progress, and informs the user upon completion.

D. AQUINAS

® Condor is a registered trademark of the University of Wisconsin

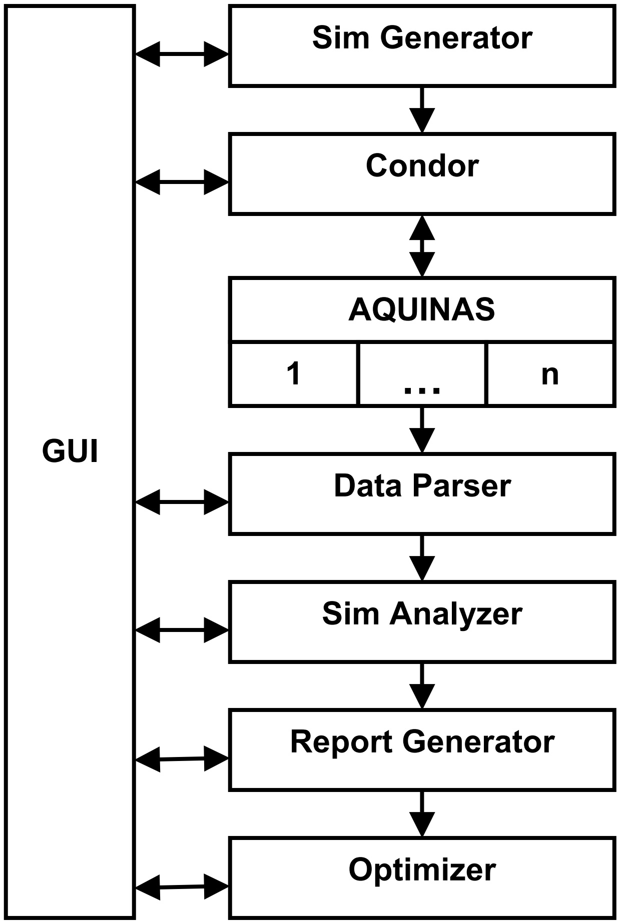

Figure 3 TOMAS AQUINAS components

AQUINAS is a QCA array simulator that forms the core of the TOMAS AQUINAS system. AQUINAS uses QCA cell geometry, cell location, input signals and clock signals to calculate the time evolution of the quantum mechanical state of an arbitrary QCA array. A command line interface to AQUINAS is utilized to enable batch processing. Each simulation input file is submitted to AQUINAS.

E. Data Parser

The output of each AQUINAS simulation is a text file that contains simulation settings, a circuit description, and a time history of the evolution of the polarization of all QCA cells in the array. To simplify the analysis of data from a large population of simulations, Data Parser (DP) creates a composite data file. DP opens each simulation output file, extracts the final polarization of the output cell, and appends this data to the composite data file. Subsequent analysis tools only have to access this composite data file instead of multiple AQUINAS output files.

F. Sim Analyzer

The user specifies all inputs to the block majority gate, therefore, the correct output is known *a priori*. If the output is within a user-specified threshold of the target value the BMG passes the test, otherwise it fails. Therefore, the Monte Carlo simulations are Bernoulli trials and the population parameters are described by a binomial distribution [11]. The mean, variance, and 95% confidence levels for the population characterize the tolerance of this specific gate topology to the applied defects. Sim Analyzer (SA) performs these calculations and writes the results to a file.

G. Report Generator

The MATLAB® Report Generator (RG) [12] is used to document all aspects of the experiment. Reusable templates are created to capture and organize all of the simulation configuration parameters, Condor parameters and log files, analysis options and results. The templates are dynamic; content can be adjusted based on any of the workspace parameters, such as analysis results. The files can be saved in HTML, SGML, XML and Word formats.

IV. Optimization

A. Array Topology Optimization

Gate topology can be optimized for a given fabrication process by determining the minimum array configuration(s) that achieves the required fault tolerance. Each set of Monte Carlo simulations yields one datum that describes the probability that this gate configuration will yield a correct result when fabricated using this process. Modifications to the gate configuration by varying the number of rows and/or columns, cell size, and cell spacing and repeating the Monte Carlo simulations with the same defect distribution, mean, and variance will yield additional data points. Analysis of the curve generated by this data can be used to optimize the gate topology for the fabrication process.

B. Fabrication Process Optimization

Similar techniques can be utilized to optimize fabrication processes by keeping the gate topology constant and varying the manufacturing variation and device defect models. Each set of Monte Carlo simulations yields one datum that describes the probability that this gate configuration will yield a correct result when fabricated using these process parameters. Analysis of the family of curves generated by this data can be used to determine the sensitivity of the array to process parameters. The parameters with the highest sensitivity offer the greatest gains in array fault tolerance.

V. Future Work

The National Science Foundation Materials Research Science and Engineering Center intends to apply the TOMAS AQUINAS system to identify QCA directed-self-assembly process optimization parameters. There are many opportunities to enhance the capabilities of TOMAS AQUINAS to facilitate this effort. Our major goals include the

® MATLAB is a registered trademark of The Mathworks, Inc.

application of more sophisticated statistical techniques, and incorporating the ability to model internal QCA cell defects.

A. *DOE and Response Surface Methods*

Basic Monte Carlo techniques are simple to apply, however, more efficient optimization procedures exist. Statistical design of experiment (DOE) techniques can significantly reduce the number of simulations required to determine the result within a user-specified confidence level [13]. Additionally, DOE techniques can uncover correlations between variables that cannot be determined from a one-factor-at-a-time approach. When used in conjunction with DOE, response surface methods (RSM) provide powerful empirical model building tools that can be utilized in multi-variable optimization [14], [15]. This combination of techniques can be applied to efficiently determine optimum array topologies and fabrication process parameters.

B. *QCA Cell Defect Modeling*

Though the analogy has limitations due to the limited number of elements that constitute a QCA cell, for the purposes of these analyses, the topology of an ideal QCA cell is also comparable to a two-dimensional crystal lattice. The unit cell of this lattice is a rectangle with a quantum dot (QD) at its center. A QD missing from the cell is equivalent to a lattice vacancy. A QD stuck in a single quantum state is comparable to a dopant in a crystal lattice. Additionally, non-uniform QD sizes and asymmetrical arrangements of the quantum dots within the cell can be viewed as types of lattice distortions. The current version of AQUINAS cannot simulate these defects.

VI. Conclusion

In order for QCA-based logic to be viable, QCA gate architectures that are tolerant of manufacturing variations and device defects must be developed. Design tools that support the analysis and optimization of QCA arrays and fabrication processes are required. We have added these capabilities to AQUINAS by developing the TOMAS framework that enables the integration of advanced configuration, control, and analysis tools with AQUINAS.

Acknowledgment

We sincerely appreciate the access to AQUINAS source code provided by Dr. Craig Lent of the University of Notre Dame. We would also like to thank Dr. Amir Fijany for information on block QCA gate architectures, and Dr. Richard DeLoach for support during the development of the statistical techniques.

References

[1] P. D. Tougaw and C. S. Lent, “Logical devices implemented using quantum cellular automata,” *Journal of Applied Physics*, vol. 75, pp. 1818–1825, 1994.

[2] W. Porod *et al*., “Quantum-dot cellular automata: computing with coupled quantum dots,” *Int. J. of Electronics*, vol. 86, pp. 549-590, 1999.

[3] I. Amlani et al., “Digital logic gate using quantum dot cellular automata,” *Science*, vol. 284, pp.289-291, 1999.

[4] G. L. Snider *et al.*, “Quantum-dot cellular automata: Introduction and experimental overview,” in *Proc. IEEE-Nano 2001*, 2001, pp. 465-470.

[5] F. Rojas, E. Cota, and S. E. Ulloa, “Quantum dynamics, dissipation, and asymmetry effects in quantum dot arrays,” *Phys. Rev. B*, vol. 66, pp. 235305, 2002.

[6] A. Fijany and B. N. Toomarian, “New design for quantum dots cellular automata to obtain fault tolerant logic gates,” *Journal of Nanoparticle Research*, vol. 3, pp. 27-37, Feb. 2001.

[7] C. S. Lent *et al.*, “AQUINAS-A quantum interconnected network array simulator,” in *Proc. Fifth International Workshop on Computational Electronics*, 1997.

[8] R. B. Phillips, “*Crystals, defects, and microstructures: modeling across scales*,” New York, NY: University Press, 2001.

[9] J. Weertman and J. R. Weertman, “*Elementary dislocation theory*,” New York, NY: Oxford University Press, 1992.

[10] Available: http://www.cs.wisc.edu/condor/.

[11] R. V. Hogg and J. Ledolter, *Applied Statistics for Engineers and Physical Scientists*. New York, NY: Macmillan Publishing Co., 1987.

[12] Available: http://www.mathworks.com/products/ML_reportgenerator/ .

[13] D. C. Montgomery, *Design and Analysis of Experiments*, New York, NY: John Wiley & Sons, 1997.

[14] R. H. Meyers and D. C. Montgomery, *Response Surface Methodology Process and Product Optimization Using Designed Experiments*, New York, NY: John Wiley & Sons, 1995.

[15] G. E. P. Box and N. R. Draper, *Empirical Model-Building and Response Surface Methods*, New York, NY: John Wiley & Sons, 1987.