

# Enhancements to a Superconducting Quantum Interference Device (SQUID) multiplexer readout and control system

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## ABSTRACT

Far-infrared detector arrays such as the 16x32 superconducting bolometer array for the SAFIRE instrument (flying on the SOFIA airborne observatory) require systems of readout and control electronics to provide translation between a user-driven, digital PC and the cold, analog world of the cryogenic detector. In 2001, the National Institute of Standards and Technology (NIST) developed their Mark III electronics for purposes of control and readout of their 1x32 SQUID Multiplexer chips. We at NASA's Goddard Space Flight Center acquired a Mark III system and subsequently designed upgrades to suit our and our collaborators' purposes. We developed an arbitrary, programmable multiplexing system that allows the user to cycle through rows in a SQUID array in an infinite number of combinations. We provided 'hooks' in the Mark III system to allow readout of signals from outside the Mark III system, such as telescope status information. Finally, we augmented the heart of the system with a new feedback algorithm implementation, flexible diagnostic tools, and informative telemetry.

Keywords: bolometer array, transition edge sensor, superconducting multiplexer, SQUID multiplexer, cryogenics

## 1. INTRODUCTION

### 1.1 Transition Edge Sensors

Transition-Edge Sensors (TESs) are highly sensitive, cryogenic detectors. An image viewed by a telescope is projected onto a TES, and the change in heat present on the detector represents the image's energy. TES sensitivity is inversely proportional to temperature, so they must be thermally isolated<sup>1</sup>. In the context of this project, TES detectors are housed in a cryogenic chamber, or dewar.

TES detectors are new technology that may replace semiconductor bolometers in astronomical and materials applications<sup>1</sup>. Transition Edge Sensors offer many practical advantages over semiconductor bolometers. TES detectors are more sensitive than semiconductor bolometers operating at the same temperature. Another advantage is TES detectors can be run at higher speeds than semiconductor bolometers operating at the same temperature<sup>3</sup>. Both of these advantages are related to one of the greatest advantages of TES detectors; TES detector arrays are, potentially, easily multiplexed.

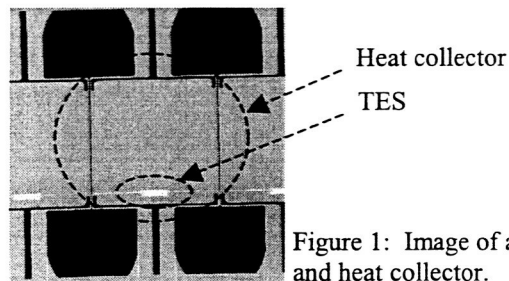


Figure 1: Image of a TES detector and heat collector.

Semiconductor bolometers are high impedance devices; a robust amplifier must be present in the dewar for signal readout. FET amplifiers at a temperature of 70K are a typical implementation of this requirement. A drawback to this approach is it necessitates the use of 1 FET per detector, meaning a limit on detector array size and increase in wire count. The upper limit on an array of semiconductor bolometers is typically 500 pixels. This translates to 500 FETs, and a dicey wiring situation.

TES detectors are low impedance devices; almost superconducting. A TES array is multiplexed using a clever implementation of Superconducting Quantum Interference Devices (SQUIDs). The SQUIDs used in this project were developed at the National Institute of Standards and Technology (NIST) in Boulder, CO. SQUIDs are cryogenic, low-noise, low-power, and low-impedance amplifiers. The readout of a large-scale, two-dimensional array of TES detectors is achieved utilizing a SQUID multiplexer, also developed at NIST. SQUID multiplexer technology reduces both wire count and power dissipation over a non-multiplexed configuration. SQUIDs are ideal amplifiers for TES detectors, but have one drawback. The  $V-\phi$  (voltage versus flux) response of a SQUID amplifier is nonlinear; linear operation is only achieved by applying a periodically-switched feedback signal to the SQUID multiplexer. A generalized  $V-\phi$  response of a typical SQUID is illustrated in Figure 1. The switched-feedback must be operated such that the response of the SQUID maintains linearity on the proper period of the response curve.

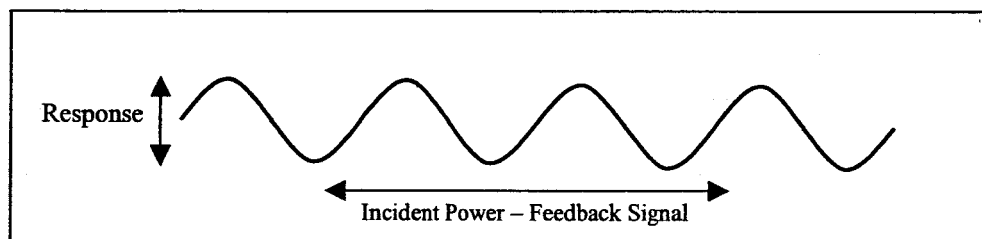


Figure 2: Generalized  $V-\phi$  response of a SQUID amplifier.

NIST manufactures SQUID multiplexer chips to handle  $1 \times 32$  TES arrays. Construction of multi-column arrays is achieved by wiring enable inputs for each corresponding row together. For example, in a  $16 \times 32$  array, the enable inputs for row 5 of each chip are tied together. Turning row 5 on in one chip turns on row 5 in every chip. Since one readout and switched-feedback signal exists per chip, multiplexing of a multi-column array is achieved by turning on an entire row of an array, then performing readout and feedback individually for each column. These operations must be done with room temperature electronics. NIST developed a system of room-temperature electronics called the Mark III that performs the readout and switched-feedback operations.

### 1.2 History of the NIST Mark III SQUID multiplexer readout and control system

In 1999, Dave Bergman, Bob Baker, and Rick Shafer (NASA GSFC) designed the Mark II; an electronics system built to readout and control  $1 \times 8$  SQUID multiplexer arrays. The system worked well, but for larger arrays, a more modular system was needed. NIST's John Martinis, Sae Woo Nam, and Carl Reintsema developed the original Mark III in 2000.

### 1.3 Reasons for enhancements of the Mark III

The Mark III is an excellent system for testing and operating  $1 \times 32$  SQUID multiplexer arrays in a laboratory setting. Use of the Mark III in an instrument setting necessitates additional functionality. The design of enhancements to the Mark III requires the addition of three new system components and a firmware overhaul of an existing design. The table below catalogs enhancement needs for instrument use, and the decisions for implementation.

Need	Reason	Method of Implementation
Self-Documenting Data Stream	Long-term and remote use requires	Upgraded DFB Card firmware
Access to high-time resolution (raw) data		Upgraded DFB Card firmware
Acquisition of signals from external systems (i.e. telescope timing signals)	Facilitates comparing disparate data streams	Addition of Interface Card
Programmable, arbitrary row-changing sequences	Allows remote operation, facilitates characterization techniques	Addition of Interface Card, Address Card and Cryogenic Address Driver
Ability to pass analog signals to first-stage SQUID bias lines	Facilitates multiplexing	Cryogenic Address Driver

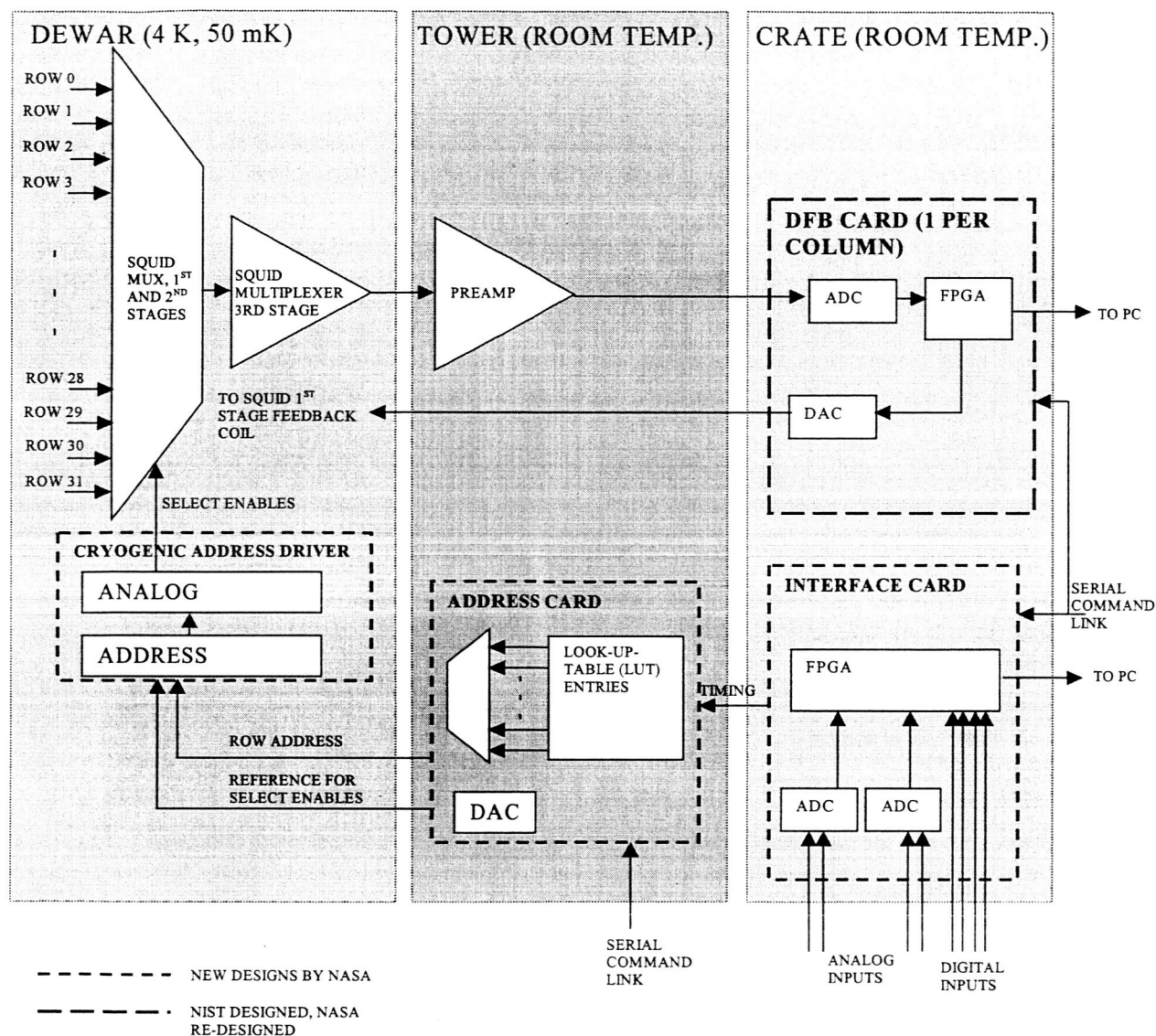


Figure 3: Generalized Mark III Block Diagram

#### 1.4 Customers and Collaborators

The upgrades to NIST's Mark III electronics will be deliverable to several NASA missions and university collaborations. These missions and collaborators will use the Mark III electronics and SQUID multiplexers to readout and control arrays of Transition Edge Sensors (TESs). The University of Pennsylvania's Simon Dicker is developing a 90GHz detector array that will be a facility instrument for the Green Bank Telescope (GBT). SAFIRE will be an instrument aboard the Stratospheric Observatory for Infrared Astrophysics (SOFIA), administered by the USRA. SAFIRE<sup>8</sup> is a Fabry-Perot spectrometer, and will deliver in FY06. Cornell University's South Pole Imaging Fabry-Perot Interferometer (SPIFI)<sup>1</sup> and 'Z' (red shift) Early Universe Spectrometer (ZEUS)<sup>3</sup> will also use TES arrays. SPIFI will be used at the Antarctic Sub millimeter Telescope / Remote Observatory (AST/RO)<sup>1</sup> and the James Clark Maxwell Telescope (JCMT) will utilize ZEUS<sup>1</sup>. Princeton's Atacama Cosmology Telescope in Chile will use TES arrays to perform very sensitive observations of the Sunyaev-Zel'dovich effect in galaxy clusters<sup>7</sup>. It is worthy to note the current customers for this effort are earth and sub-orbital missions, not space-flight missions.

## **2. DESIGN COMPONENTS**

### **2.1 Address Card and Driver**

The Address Card and Driver are designed to facilitate multiplexing large SQUID multiplexer arrays. The room temperature Address Card translates user commands and system timing for Ernie Buchanan's cryogenic Address Driver, which performs row selection on the SQUID multiplexer chips at 4K.

The primary function of the Address Card is to implement a user-programmable, row-switching algorithm. The algorithm allows the user to create an arbitrary sequence of changes in the index of a Look-Up-Table (LUT). The values in the LUT contain actual row addresses; these addresses are read from the table and passed to the Cryogenic Address Driver.

The Address Card also provides a user-adjustable voltage reference to the Cryogenic Address Driver. The selected row address and voltage reference serve to 'turn on' one row of a 1x32 SQUID multiplexer. The Address Driver performs this function by a novel implementation of CMOS chips operating at liquid He. The end result is the Address Card and Cryogenic Address Driver give the user the ability to arbitrarily cycle through the rows in a multi-column, SQUID-multiplexer array.

The abilities of the Address Card / Driver combination would be useless if their actions occurred asynchronous to the heart of the SQUID multiplexer control loop, the Digital Feedback (DFB) Card. Remember, the driving purpose of the Mark III electronics system is to maintain a linear response in the SQUID multiplexer. Each DFB card is assigned to a column of a SQUID multiplexer array. Since the Address Driver enables only one row at a time, the Mark III system is able to isolate one pixel of each column at a time for sampling and feedback. Proper functionality requires DFB card 'awareness' of the Address Card and Driver behavior.

### **2.2 Interface Card**

The Address Card is housed in the Tower; the DFB Card in the Crate. The Tower and Crate are on separate clock domains. The Interface Card solves the problem of synchronization between the Address Card and the DFB cards by passing a system frame synchronization signal, along with a divided-down system clock to the Address Card.

The Tower was originally designed as an analog, passive, and RF-tight means of passing signals back and forth between the Crate and the SQUID multiplexers. The Tower was designed such that all power returns are passed over the chassis of the Tower. Inserting a digitally-operated Address Card in the Tower means that every time an inbound clock pulses, ringing will appear on the ground plane of every other card in the Tower. This is important; the Preamp Card output is a crucial point in the SQUID control loop. Therefore, the clock for the Address Card had to be specially formatted to maximize the amount of 'quiet' time on the remaining Tower Cards during signal acquisition.

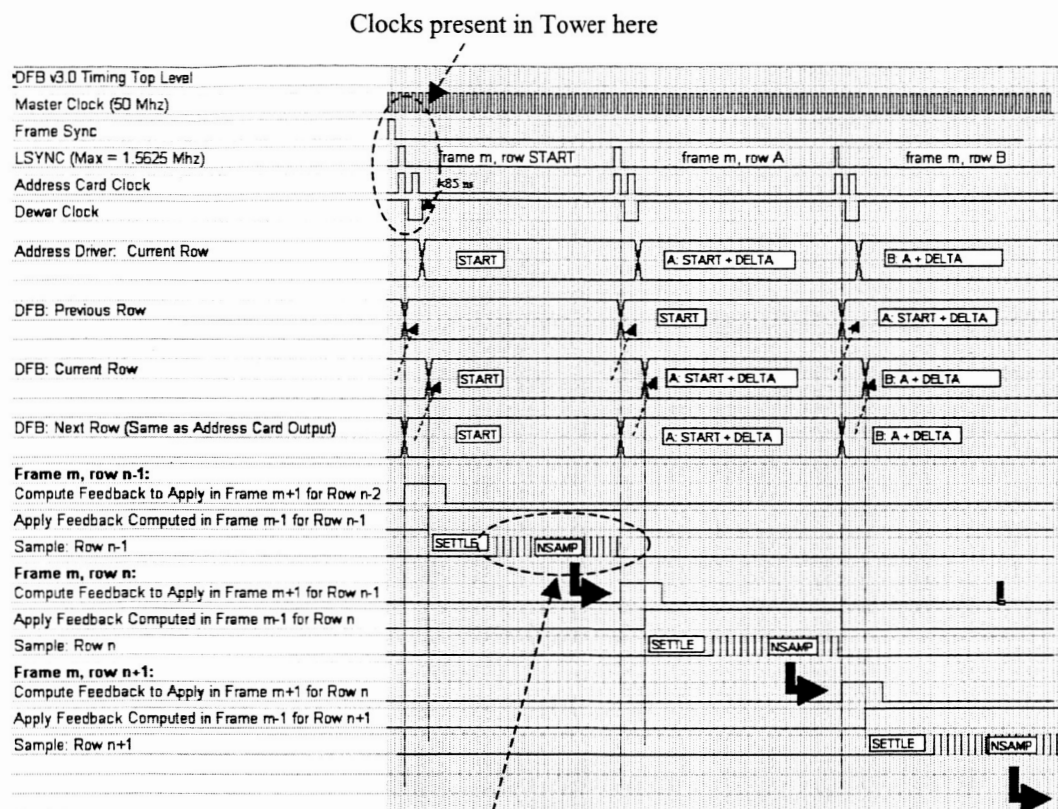


Figure 4: System Timing

DFB signal acquisition

Future revisions of the Interface Card will also include up to four analog and six digital inputs for acquisition of signals from external electronics systems. This allows the Mark III user to synchronize its data-stream with information from other systems in an installation. For example, by acquiring low-frequency timing pulses from a telescope, the Mark III user can synchronize the behavior of the SQUIDS with the location of the telescope in the sky.

### 2.3 Digital Feedback Card Firmware Upgrade

The intention of the Digital Feedback Card firmware upgrade is to provide the Mark III user the capability to readout and control SQUIDS in an instrument setting. The primary action taken to facilitate this goal is the inclusion of a bevy of telemetry and synchronization information into the data-stream. Headers document the Mark III data-stream at user-defined intervals. User-requested status dumps are available. Several modes of packing and streaming data are at the users disposal. Though the user is primarily interested in the data read out from the SQUIDS, instrument use requires periodic telemetry and status information to insure the system is behaving in a proper manner.

NIST's original firmware (v2.0) contained the means to generate DC and triangle waveform outputs for diagnostic and calibration purposes. The new DFB firmware adds a saw tooth waveform to the repertoire. The original firmware computed its feedback via a Proportional-Integrator (PI) loop; the new firmware utilizes a Proportional-Derivative (PD) calculation loop.

Feedback is applied to each row on the next instance of enabling that row. Feedback applied to the next instance of a row (denoted by the subscript 'm+1') is based on the most recent ('m') samples taken of that row and previous ('m-1') samples of that row. The feedback applied to each row is, in its most simplified form, expressed as

$$D_{m+1,n} = [(1+f_n)*(D_{m,n} + \alpha_n x_{m,n})] - [f_n*(D_{m-1,n} + \alpha_n x_{m-1,n})]. \quad (1)$$

The parameters are defined in the table below.

Table 2: Feedback Algorithm Parameters

Parameter	Description	Units	User-Programmable?	Notes
$h$	Feedback Threshold	ADC Counts	By LUT entry	If $ x_{m,n}  > h$ , then the product $\alpha_n x_{m,n}$ in eqn. (1) is set to 0.
$D_{m+1,n}$	DAC Value – Current Row, Next Frame	DAC Counts	N/A	
$D_{m,n}$	DAC Value – Current Row, Current Frame	DAC Counts	N/A	
$D_{m-1,n}$	DAC Value – Current Row, Previous Frame	DAC Counts	N/A	
$f_n$	Prediction Factor – Current Row	N/A	By LUT entry	$0 \leq f_n \leq 2$
$\alpha_n$	Proportional Gain – Current Row	(DAC Counts) / (ADC Counts)	By LUT entry	$0 \leq \alpha_n \leq 2/G$ , where $G$ is the (linear) system response of the SQUID to a change in the DAC value. Note $G$ can be positive or negative. $\alpha_n$ can be obtained during calibration.
$x_{m,n}$	Error Signal – Current Row, Current Frame	ADC Counts	N/A	Difference between ADC input and $t_n$ , accumulated and radix-adjusted over NSAMP samples.
$x_{m-1,n}$	Error Signal – Current Row, Previous Frame	ADC Counts	N/A	
$t_n$	Target – Current Row	ADC Counts	By LUT entry	
NSAMP	Number of Samples	N/A	Yes	$0 \leq \text{NSAMP} \leq (2^{20} - 1)$

The Error signal is the difference between each ADC sample and a user-programmable target value ( $t_n$ ), accumulated and radix-adjusted over NSAMP samples. Additionally, if  $|x_{m,n}| > h$ , then the product  $\alpha_n x_{m,n}$  in (1) is set to 0.

During a system event, some quantity of incident power arrives at the SQUID. The signal at the input to the ADC is representative of this incident power, in a 12-bit ADC word. Calculation of the proper SQUID feedback requires conversion of units to a 14-bit DAC word.

Figures 5, 6, and 7 show simulated responses of the DFB algorithm under a variety of conditions. Figure 5 illustrates behavior of the system to an impulse event with the predictor-corrector capability disabled ( $f_n = 0$ ) and  $\alpha_n = 0.5$ . In this condition, equation (1) reduces to

$$D_{m+1,n} = (D_{m,n} + \alpha_n x_{m,n}) \quad (2)$$

Figure 5 illustrates the beauty of the SQUID feedback system. The sum of the error signal and the feedback equal the incident power on the system. Telemetry of the DAC value and error signal tells the Mark III user power present on the SQUID at any given time. For example, at time = -1, the current DAC value, and error signal are zero, the incident power is zero. The calculated DAC value for time = 0.0 is therefore, zero. However, at time = 0.0, an impulse power is applied to the system. The error signal is now 1.0; since our current DAC value is 0.0, we know the incident power on the system is 1.0. As time increases, one can see the feedback 'catches up' to the impulsive event.

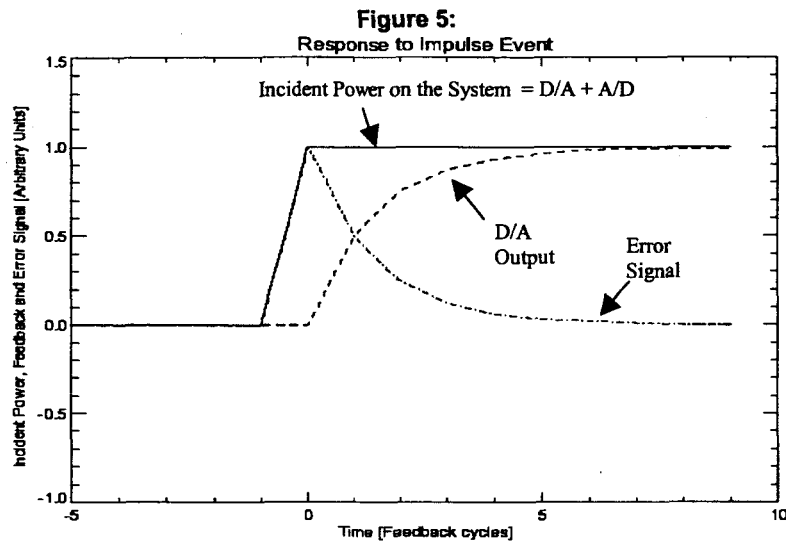
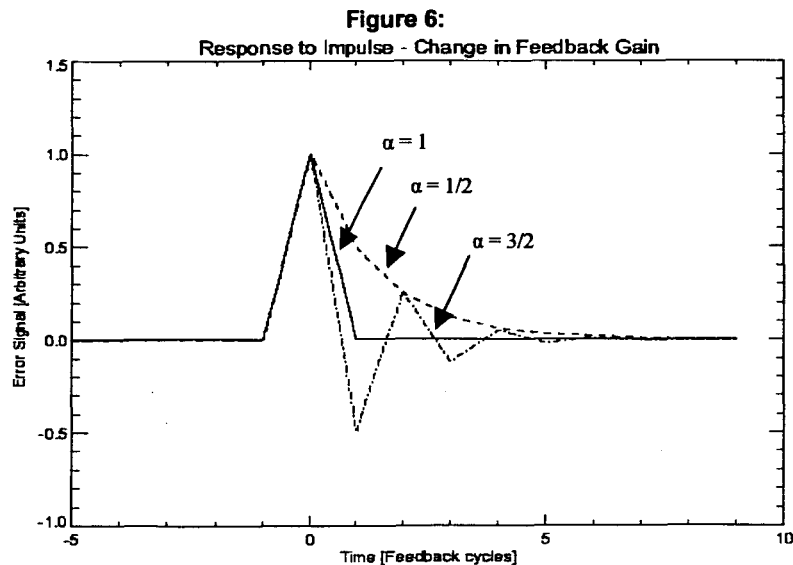


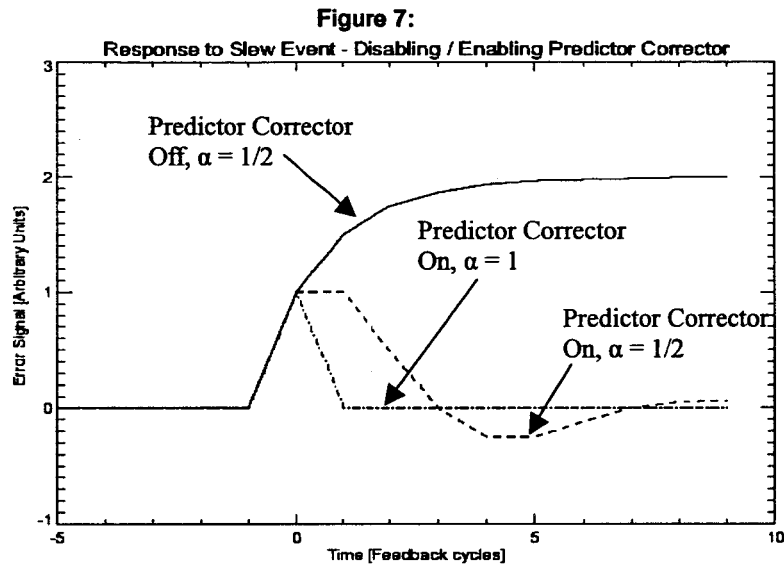
Figure 6 shows the behavior of equation (2) for different values of  $\alpha_n$  in terms of the error signal. In the case of  $\alpha_n = 0.5$ , we see the error signal asymptotically dies off, as in Figure 5. When  $\alpha_n = 1.5$ , the error signal rings and eventually settles out. The proportional gain is most accurate at  $\alpha_n = 1$ . In this case, significant error is present for only one cycle. This behavior is the result of accurate SQUID calibration; the algorithm is able to fully respond to an impulsive event in one feedback cycle.



The final figure shows error signal responses for a slew event on the system. The bold line shows the purely proportional gain scenario dictated by equation (2). The error for the system asymptotically reaches a value equal to the slew rate divided by  $\alpha_n$ . The other two cases utilize the predictor factor by setting  $f_n = 1$ ; equation (1) now becomes

$$D_{m+1,n} = [2(D_{m,n} + \alpha_n x_{m,n})] - [(D_{m-1,n} + \alpha_n x_{m-1,n})]. \quad (3)$$

Tuning the predictor factor on allows the algorithm to use the previous two sets of samples to respond quickly to a slew event. The behavior for inaccuracies in  $\alpha_n$  can be seen in Figure 7. When  $\alpha_n$  is 0.5, an oscillation is induced in the error signal before it settles out to 0.0. When the gain is picked accurately ( $\alpha_n = 1$ ), the feedback lags for one clock cycle and thereafter tracks the slew event present on the system.





A block diagram of the DFB card firmware is shown in Figure 8.

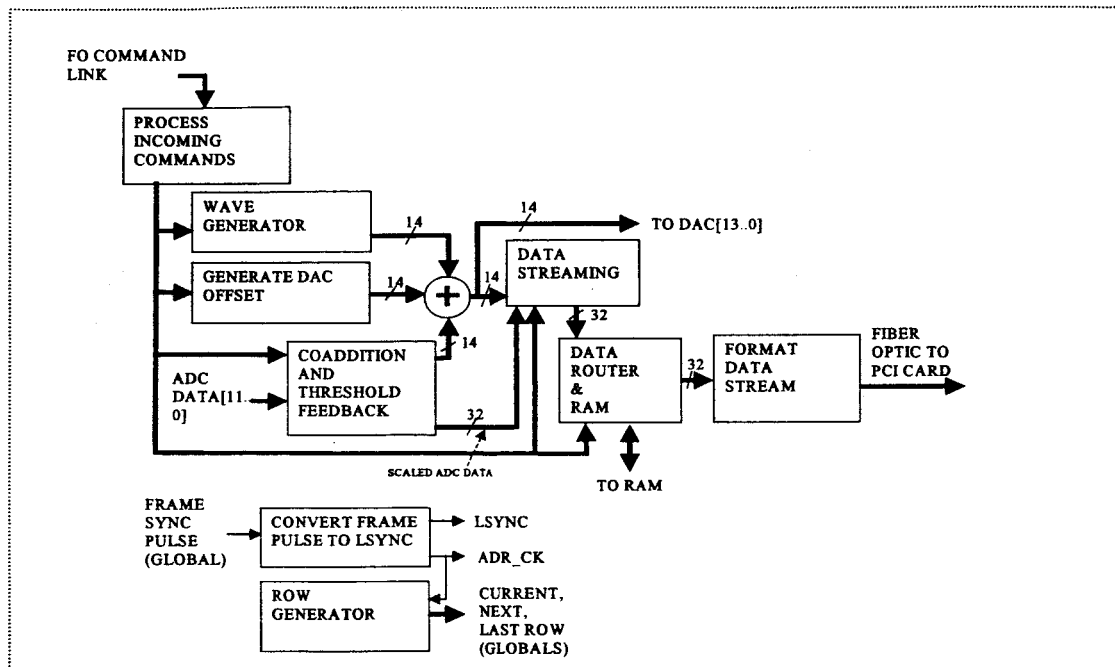


Figure 8: DFB v3.0G Block Diagram

## 2.4 Software Upgrades

The primary scope of this discussion is on electronics upgrades. However, the software changes taking place in conjunction with the electronics modifications deserve mention. The original NIST package provided a custom driver for its data acquisition card, and Python scripts for writing commands to, and reading data from, the electronics. The Mark III enhancements were planned so as to utilize the Instrument Remote Control (IRC) software suite instead of Python scripts. IRC is a platform-independent, extensible, and generic software package that allows scientists to operate instruments in remote locations over an intranet<sup>2</sup>. Utilization of NIST's data acquisition card with the IRC framework required additional software effort.

NIST's custom driver was originally installed on Debian Linux 3.0. Work has been carried out to port NIST's custom data-acquisition driver to Red Hat Linux<sup>3</sup>. IRC is RedHat-proven, but additional effort had to be made to allow the NIST driver to communicate to IRC's Java-based platform<sup>4</sup>. Mark III-specific component development for the IRC platform is forthcoming.

### 3. DESIGN STATUS

#### 3.1 Multiplexing (Address Card, Address Driver, Interface Card) Status

At the time of manuscript submission, the multiplexing portion of the enhancements has been fabricated and tested. Figures 9 and 10 show the output of the Address Driver under operation in liquid He. For proper data streaming, the Mark III row-switching rate is constrained to  $1.5625 \text{ MHz}^2$ ; this test was performed utilizing the Interface Card and Address Card operating at a row-switching rate of approximately 2 MHz. Figures 9-12 show the new Mark III components in the test environment.



Figure 9: Test dewar and dunk probe.

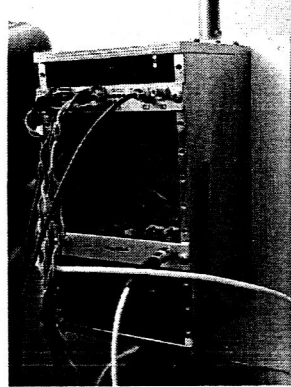


Figure 10: Test Tower; Address Card is on the bottom

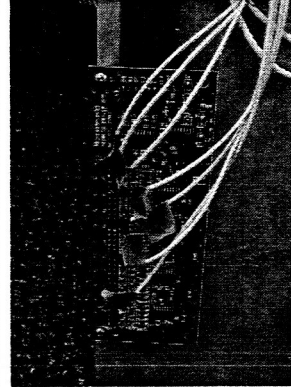


Figure 11: Cryogenic Address Driver

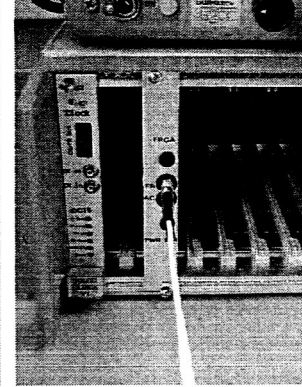


Figure 12: Test Crate; Interface Card at right

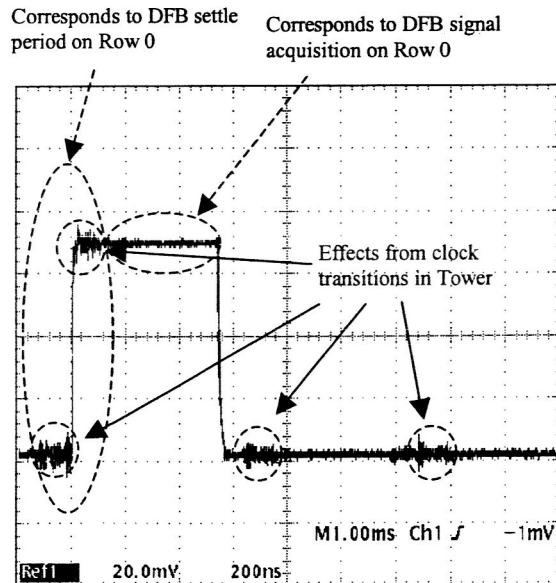


Figure 13: Address Driver Test in Liquid He – Enable Pulse for Row 0

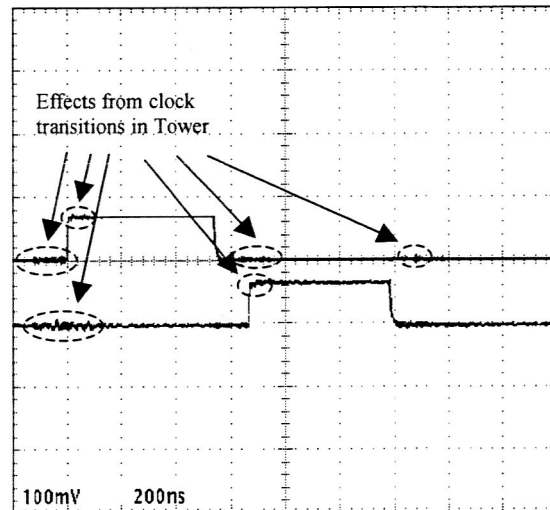


Figure 14: Address Driver Test in Liquid He – Transition Between Adjacent Rows.

Graphs 13 and 14 illustrate the effects of digital clocks on the Tower shared-return design. Refer to Figure 3 for the system timing. Without isolating the Interface Card outputs to the DFB settle region, noise effects from these outputs would affect DFB signal acquisition. Though noise present on the Address Driver output may degrade acquisition, the potential noise pickup on the preamp card (see Figure 4) was the driving force in design of the system timing.

### **3.2 DFB Firmware v3.0G Status**

The DFB firmware overhaul has finished the coding and simulation stage. A limited version of the new firmware is being tested to validate the functionality of the feedback algorithm and data streaming processes. Slight changes to the firmware are expected as new failure modes and operational needs are encountered.

### **3.3 Status of Other Enhancements**

The external input feature of the Interface Card has been fabricated and tested at the prototype level. A new revision the Interface Card that will include these features is in fabrication.

The software modifications necessary to run the Mark III with IRC are partially completed. Specifically, the NIST-custom driver is operating on the Princeton RedHat 7.3 installation. Code has been written that will allow the driver to continuously stream data to a Java interface. Upon successful testing of the DFB firmware, a command parameter specification will be submitted for Mark III-specific IRC parser development. Mark III Graphical User Interfaces (GUIs) await completion.

## **4. CONCLUSIONS**

NIST's development of the Mark III electronics system created a modular alternative to the Mark II system. The Mark III is optimal for small TES arrays utilized in a laboratory environment. NASA's contribution to the collaboration is modification of the Mark III system such that users of larger TES arrays may operate NIST's Mark III system in an instrument setting.

NIST, NASA, and university collaborators have all contributed to the maturation of a SQUID multiplexer readout and control system over the past five years. Enhancements to the system, in conjunction with the IRC software package, have the potential to allow scientists to remotely operate large Transition Edge Sensor arrays in ground-based and sub-orbital missions. Every party's contribution to the collaboration serves to create a system that will advance a technology that may significantly affect astronomical imaging.

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