Final Report for the Project Entitled

PSAW/MicroSWIS [Microminiature Surface Accoustic Wave (SAW) based Wireless Instrumentation System]

Contract No. NAS3-01118

Sponsored by: Glenn Research Center

Baseline

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September 2004

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REVISION AND HISTORY PAGE

Revision	Description	Publication Date
Baseline	Initial Release	Sep-04

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1. Scope

This Final Report for the PSAW / MicroSWIS Program is provided in compliance with contract number NAS3-01118. This report documents the overall progress of the program and presents project objectives, work carried out, and results obtained.

2. Program Goals and Objectives

Program Conceptual Design Package stated the following objectives:

To develop a sensor/transceiver network that can support networking operations within spacecraft with sufficient bandwidth so that (1) flight control data, (2) avionics data, (3) payload/experiment data, and (4) prognostic health monitoring sensory information can flow to appropriate locations at frequencies that contain the maximum amount of information content but require minimum interconnect and power: *a very high speed, low power, programmable modulation, spread-spectrum radio sensor/transceiver.*

The following performance goals were identified:

2.1 PERFORMANCE OBJECTIVES FOR PHASE 2 SYSTEM:

1) Reliable communications at distances of 25 meters.
2) Potential form factor of < 4 cubic inch.
3) Total sensor/transceiver unit weight < 6 ounces.
4) Total average power of 50 milliwatts (sub milliwatt in standby).
5) 1 megabit per second baseband data rate.

2.2 PERFORMANCE OBJECTIVES FOR PHASE 3 SYSTEM:

1) Reliable communications at distances of 100 meters.
2) Potential form factor of < 0.5 cubic inch.
3) Total sensor/transceiver unit weight < 3 ounces.
4) Total average power of 50 milliwatts (sub milliwatt in standby).
5) Fifty megabits per second baseband data rate.
6) Synchronization equal to wired networks with up to 100 nodes.
7) Able to support dynamic encoding schemes that can "see through" interference.
8) Support range determination technology for geographic position fixing.
9) Recognition and rejection of jamming and spoofing.

The system designs address all of these goals, but single devices are not able to meet all of the specifications due to the technical tradeoffs inherent in the design.

3. Phase 1

The main task in Phase I was to create the Conceptual Design Package. This involved research into properties of the SAW correlator itself, communications system design, and coding theory. The following sections describe the results of these activities.

3.1 SIMULATION OF SAW OUTPUT WAVEFORM

The following plots have been generated using a simulator programmed in MatLab. The simulator is designed to accept any codes for the input signal and the correlator. The correlator simulated in the plots is encoded with the 11-chip Barker sequence {1-1 1 1-1 1 1 1-1-1-1} with 8 finger pairs/chip. The input signal is the sine wave of the same frequency as the central (carrier) frequency of the correlator, modulated BPSK-fashion with some spreading code sequence. One code sequence carries one information symbol, and therefore the symbol time is defined as the time it takes the waveform to fill the correlator (an inverse of the symbol rate of the correlator). The time units on the x-axis equal one chip duration (an inverse of the chipping rate of the correlator).

The plots show the cross correlation of the input signal and the correlator with sampling rate of 16 samples per carrier cycle. The value of the waveform multiplied by the charge per finger factor will approximate the output charge level for the actual device. The shape of the envelope of the resulting wave is dictated by the correlation function of the two codes, the code carried by the correlator and the code carried by the signal.

Figure 1 shows the cross correlation of the correlator with a single sequence carrying the same ("proper") code. The signal envelope is governed by the properties of the aperiodic auto-correlation function of the code sequence, which has a main peak that reaches maximum equal to the code length and, for Barker codes, alternates between 0 and –1 for any non-zero offset.

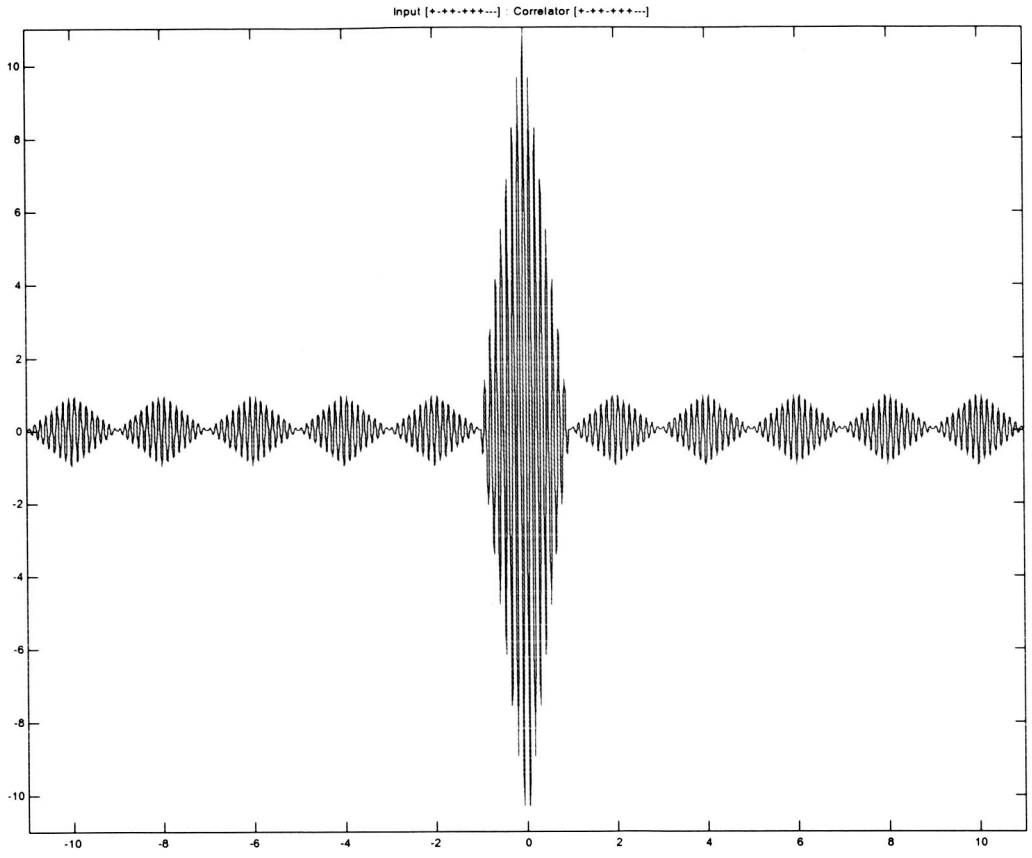

Figure 1 – Aperiodic auto correlation of Barker code

Figure 2 shows the part of the convolution function with the waveform containing a proper code immediately followed by another proper code. The section shown corresponds to the time when the correlator is almost filled with the proper code (at the beginning of the last chip) and is completely filled from then on. The envelope expresses the property of the periodic auto-correlation function of the proper code, which is constant at –1 outside the main peak in our case of the Barker code.

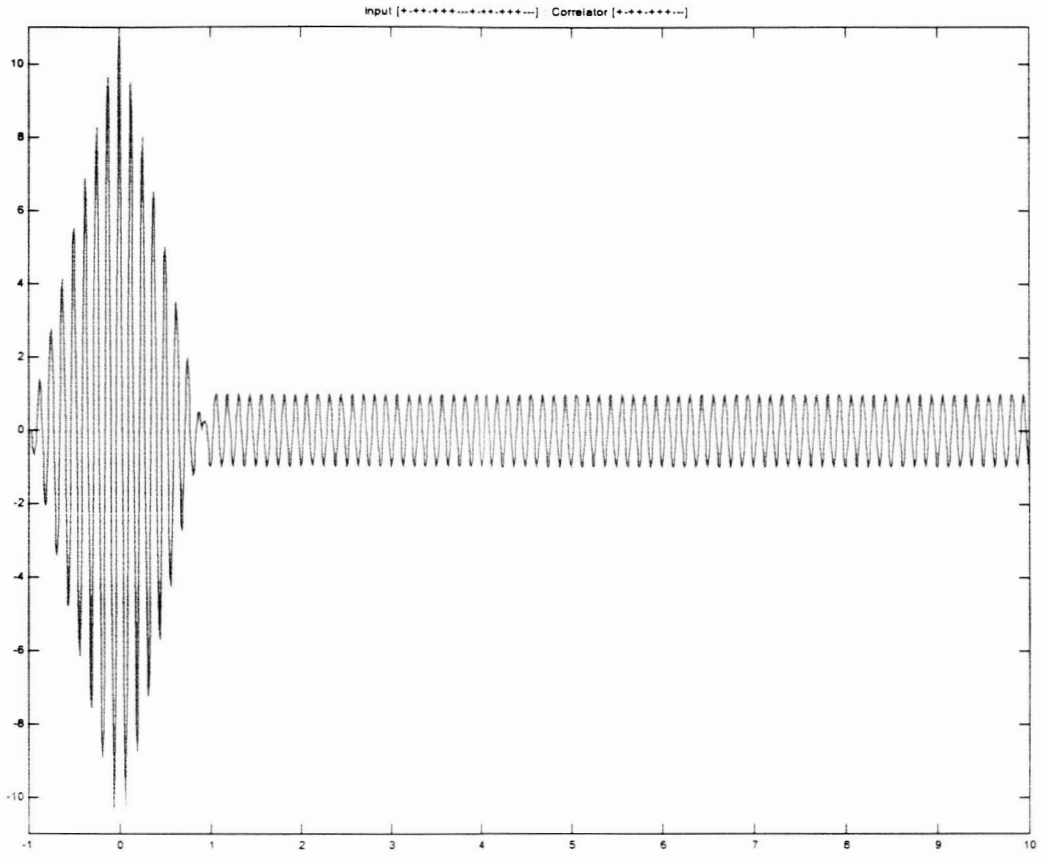

Figure 2 – Periodic auto correlation of Barker code

Figure 3 and Figure 4 show the interaction of the correlator with an unmodulated carrier signal that lasts one and two symbol periods. The envelope is governed, respectively, by the aperiodic and periodic cross-correlation function of the Barker code (fixed in a correlator) and the sequence that consists of all ones.

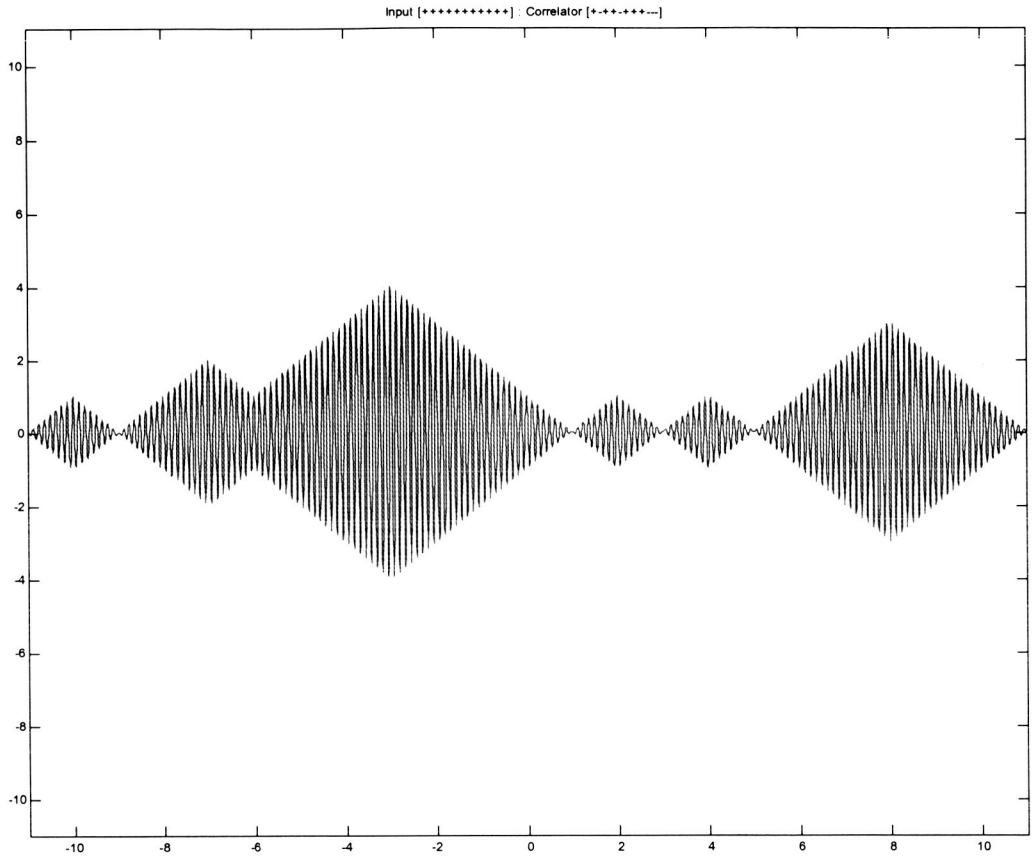

Figure 3 – Aperiodic cross correlation of un-modulated carrier and Barker Code

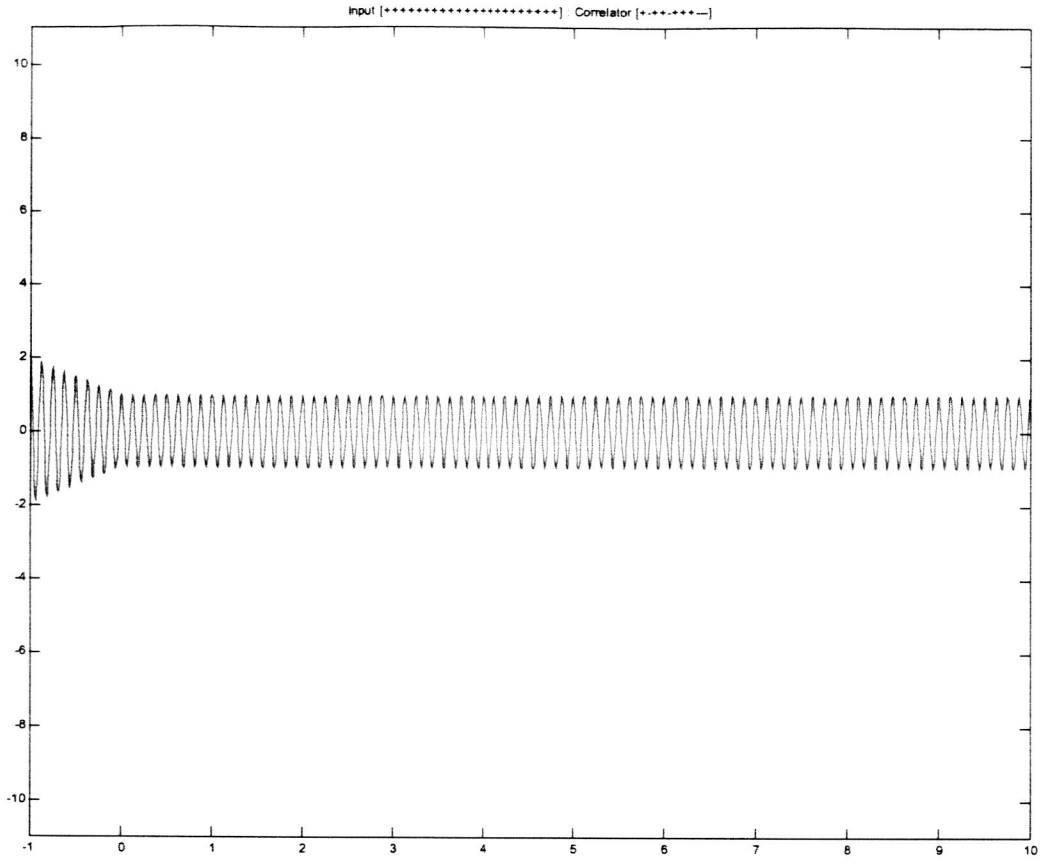

Figure 4 – Periodic cross correlation of un-modulated carrier and Barker code

Discussion of the detector circuit for the above output waveform is provided in section 3.2.1.1, Charge Amplifier/Discriminator.

3.2 COMMUNICATIONS SYSTEM DESIGN

3.2.1 Receiver Design

Shown in Figure 5 is the block diagram of an SS radio based on the proposed SAW correlators. Notice that RF down conversion is used in this receiver. The signal from the antenna is filtered and amplifier by an appropriate LNA and then routed to two SAW correlators. Two SAW correlators are shown, but in general one or more may be used. Here, for simplicity, it is assumed that one correlator is configured to detect a symbol representing a "1" and the other a "0". Then, data can be received by sending one of the two unique symbols representing a 1 or 0. The correlation outputs of the SAW correlators are detected by rectifying the RF pulse before using logarithmic signal detectors. The output of the log detectors will be at the low symbol rate and easily detected and reassembled by a low-speed signal processor (possibly a microcontroller or programmable logic).

SAW correlators offer a significant reduction of power consumption due to the above discussions, as well as due to very short "start-up" times. For the several year battery life target, it is expected that even the efficient receiver discussed here must be duty-cycled. Since the correlation process is performed in a "passive" device, the correlation results will be available within at worst two symbol periods. If one assumes a sample period of several milliseconds, chip rates of many

Mbps, and symbol sizes of 63 bits; duty cycles of over 1000 to 1 are easily achieved. Therefore, average receiver power consumption on the order of several microWatt is possible.

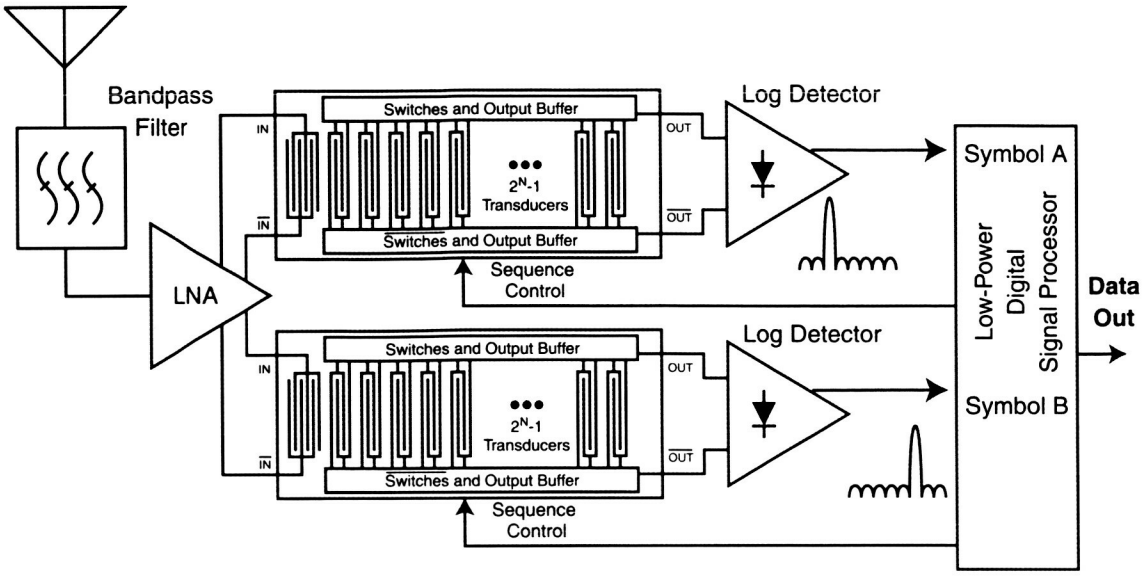

Figure 5 – Block diagram of an ultra-low-power DSSS receiver based on SAW correlators.

3.2.1.1 Detector Circuit

Correlation of the SAW filter and received signal is the amplitude of the detector circuit's input. The detector will output the envelope of its amplitude modulated input. A diode is the most commonly used component for amplitude demodulation. Figure 6 shows the basic operation of a detector diode.

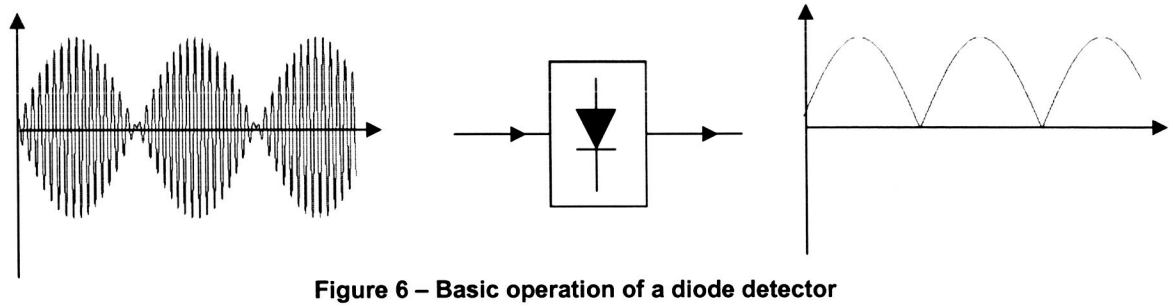

Figure 6 – Basic operation of a diode detector

Demodulation results from diodes being non-linear devices. Detection normally occurs in the square-law region, where the DC current is proportional to the square of the inputted wave's voltage. One equation for power states power equals voltage squared divided by resistance; thus, this current is also proportional to the power of the input signal. To obtain demodulation, the range of input power is limited: if too little power is applied it will be lost in the system's noise; and, if too much power is applied then the current will become a linear function of the input power (i.e., the square-law conditions will no longer apply).

Multiple options exist for implementing a diode detector. Two basic detector circuits are shown in Figure 7 below; impedance matching, filtering, and amplification on the input and output of both configurations occur in additional circuits.

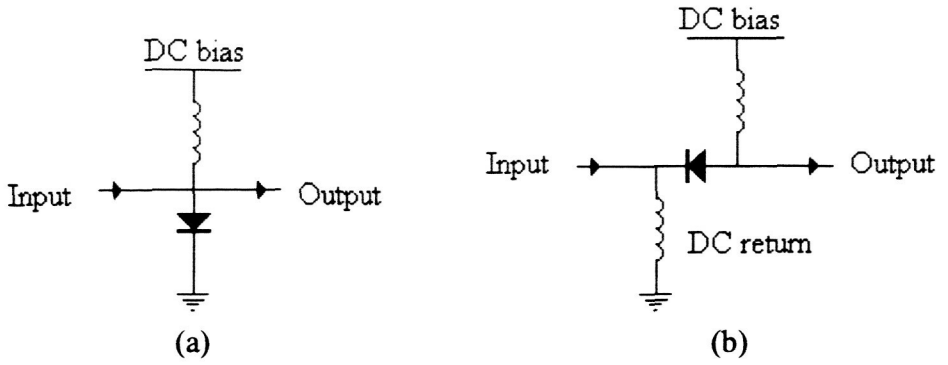

Figure 7 – Diode detector circuits: (a) in shunt; (b) in series.

3.2.2 Transmitter Design

A SAW correlator can be used to generate SS transmissions in much the same manner as it is used to receive transmissions. Input pulses will be used to excite the SAW device and create the complex waveform. The acoustic wave would then travel down the SAW device and out through the driver finger pairs. The output of the SAW is routed through a high-efficiency power amplifier to an antenna. Since transmit power consumption will be dominated by the transmitter RF output power, a power control of the output power amplifier is essential for long battery life. Protocol of the communication system should provide appropriate information on power reduction of the transmitter. This will save battery life as well as increase the aggregate CDMA network capacity (just like a cellular telephone network).

3.2.3 Antenna Design

The antenna design will be either a ¼ wave whip or patch type antenna, optimized for size and ease of use. Special designs may be necessary due to the possibly wide bandwidth utilized.

3.2.4 Impedance Matching Network

The impedance matching network will be integrated with the SAW correlator due to the small value of many of the passive components and to eliminate the variances of off-chip stray capacitance, etc. The matching network will provide a 50Ω nominal impedance for the driver end of the SAW correlator to simplify interface requirements for RF components. The correlator end of the SAW will be matched to a value yet to be determined.

3.2.5 Charge Amplifier/Discriminator

As shown in the simulation of the SAW correlator receive output, the signal generated by the reception of a valid symbol is assumed to be an "RF pulse" with a pulse width equal to one chip period and a frequency equal to twice the center frequency. Additionally, this signal is known to be a very high impedance charge-type signal that must be amplified with a charge-type amplifier.

It is assumed that this signal will be rectified and then detected with some sort of pulse discriminator or log detector. However, further investigation into the exact nature of the SAW receiver output is required prior to proceeding further with the design.

In addition to detecting the pulses that correspond to baseband data, it is desired to extract a Received Signal Strength Indicator (RSSI) signal for the purpose of determining the proper RF output power level and quality of the RF link. The height of the pulse relative to the background noise at a given time is assumed to provide this RSSI signal. The design of this circuit is complicated by the short pulse width of the received signal. Circuits designed for particle detectors and similar applications will be investigated, as well as the possibility to integrate the

received pulses over the period of a typical transmission in order to reduce the data conversion complexity.

3.2.6 Baseband Processor

The Baseband Processor (BBP) is some form of digital circuitry that performs all functions necessary to enable a general-purpose processor to interface with the SAW-based radio. The circuitry used for the BBP may also perform some operations typically performed by a Medium Access Controller (MAC). The BBP may be implemented as programmable logic, a digital signal processor, or a microcontroller.

Figure 8 and Figure 9 below show block diagrams for the receiver and transmitter portions of the BBP. In actuality, some of the common functions between the receiver and transmitter portions will be combined, but they are shown separately for clarity. Additional functionality provided by the BBP could include address recognition, error checking, etc.

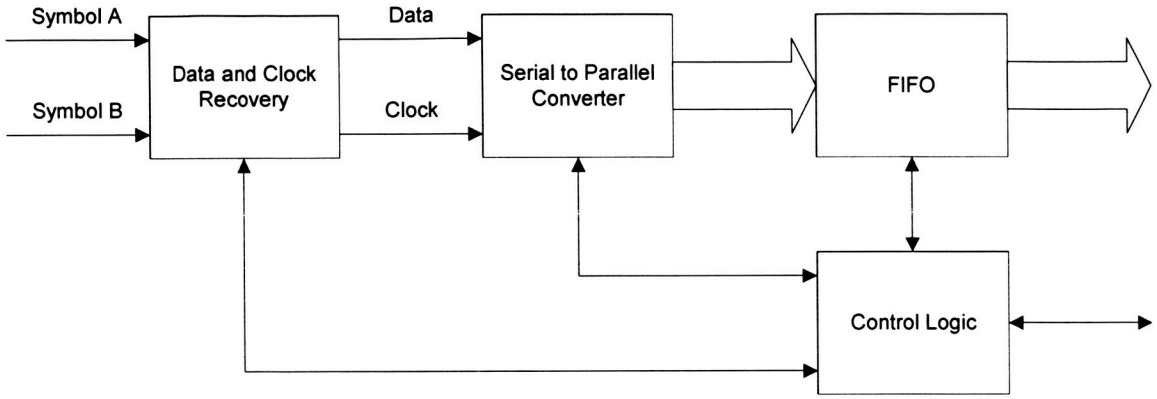

Figure 8 – Functional Block Diagram of Receiver Baseband Processor

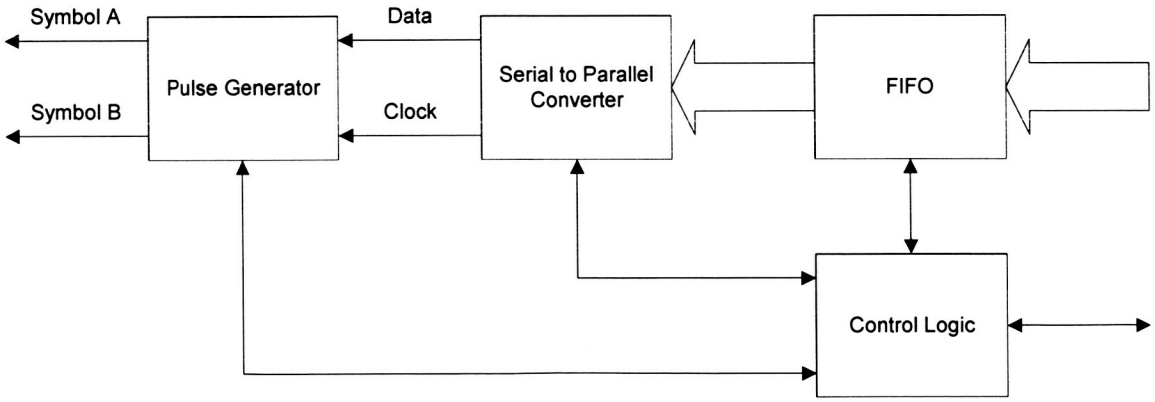

Figure 9 – Functional Block Diagram of Transmitter Baseband Processor

Initially the BBP will be designed in programmable logic such as FPGA. Designing in programmable logic will give the greatest flexibility during the prototype phase. Custom CMOS fabrication will be considered for the final implementation. CMOS should yield lower power consumption and be more robust in harsh environments.

3.2.7 RF Design Considerations

For each unique application of the SAW based radio system, a number of RF considerations must be made to optimize performance and convenience, while minimizing power consumption and size. In addition, FCC and NTIA regulations must be considered and adhered to.

3.2.7.1 Frequency Band

The Phase 2 system will target some frequency around 2.4 to 2.6 GHz, since this is the current limit imposed by the lithography processes employed. The center frequency will be set as high as possible in order to maximize data throughput. The exact center frequency will be determined with the assistance of JSC Frequency Authorization personnel.

3.2.7.2 Bandwidth

As will be described in section 3.3.1, the bandwidth of the system is controlled by the number of finger pairs per chip and the number of chips per bit. There are direct tradeoffs between these values and the occupied bandwidth that must be considered for each application.

Current FCC regulations for ISM band operation put minimum and maximum limitations on the width of the frequency band occupied. The basic SAW-based radio approach described here could be implemented to meet the FCC regulations, but severe penalties to system performance would be experienced. Because the length of the spreading code is proportional to processing gain, transmission range would be reduced.

The Programmable SAW designed in Phase 3 will most likely have "bandwidth flexibility", meaning that the frequency bandwidth of the system could be programmable by effectively changing the number of finger pairs per chip.

There has been work done by the FCC to classify "Ultra-Wideband" devices, and to provide for their approval. This process will continue to be monitored.

3.2.7.3 Output Power

Output power must be determined for all applications. Desired range, operational environment include metallic obstructions, and regulatory limits must be considered

3.3 CODING THEORY

3.3.1 Requirements

Preliminary analysis and simulation of the correlation functions suggest that we will not be able to distinguish the code sequence from its inverse (the code that differs by 180° phase) when the correlator codes are used in the bi-phase modulation scheme. Therefore, we should take the conservative approach and assume that we will need to use two separate unique codes, and thence two unique SAW devices, to transmit the binary 0 and 1. Thus the number of individual stations that the chosen code set supports is half the number of orthogonal sequences in the set.

Several families of pseudo-noise (PN), or pseudo-random noise, codes are used for DSSS communications. The choice of particular code family is dictated by the properties of the communication channel used.

The use of the SAW device as spreader-despreader presents some new requirements on the spreading codes while eliminating others usually met within spread spectrum systems. One everlasting and all-persevering requirement is that the spreading codes must possess high auto-correlation properties and low cross-code correlation for proper detection in the presence of noise, which may include other communication channels of the same system. Both of these requirements cannot be satisfied simultaneously, therefore the choice of code type will be a

compromise between the two requirements, provided the desired code family is defined for the required length.

The code length is determined as a local minimum in a multi-parameter space. The code length, equal to the theoretical maximum of the processing gain, together with the data rate define the chipping rate. The symbol rate can be expressed as:

$$F_{symbol} = \frac{F_c}{L_{cc}},$$

where F_c - the chipping rate, and L_{cc} is the chipping code sequence length.

For N_c finger-pairs per chip, the total length of the SAW device is

$N = L_{cc} \cdot N_c$ finger pairs.

The bandwidth of the spread spectrum is proportional to the chipping rate:

$$B = 2F_c = 2 * \frac{f_0}{N_c},$$

where f_0 is the center frequency of the SAW device. Combining these result we obtain another expression for the symbol rate:

$$F_{symbol} = \frac{f_0}{N} = \frac{f_0 \cdot \lambda}{N \cdot \lambda} = \frac{\text{SAW wave velocity}}{\text{Correlator physical length}}.$$

Thus, the limit on the physical length of the correlator unequivocally determines the data rate (or "symbol rate", to be precise) achievable with the device.

Fabrication techniques also impose limits on the code and SAW configuration. Most notable is the desired physical size limit of 2mm. Table 1 lists the minimum data rate and maximum number of finger pairs allowed by this constraint given the center frequency in the middle of the 2.4 GHz ISM band.

Piezo Material	Orientation	SAW Wave Velocity (m/s)	Acoustic Wave length (um)	Min data rate (MHz)	Finger pairs max
Piezo Material	Orientation	SAW Wave Velocity m/s	Wavelength (um)	Min data rate (MHz)	Max finger-pairs
LiNbO3	ROTY-X	4000	1.633	2.000	1225.0
LiNbO3	Y – Z	3488	1.424	1.744	1404.8
Quartz	Y – X	3159	1.289	1.580	1551.1
Quartz	ST – X	3158	1.289	1.579	1551.6
Bi12GeO20	(100)(011)	1681	0.686	0.841	2914.9
Bi12GeO20	(111)(110)	1708	0.697	0.854	2868.9
LiTaO3	Y – Z	3230	1.318	1.615	1517.0
ZnO	Non crystalline	3150	1.286	1.575	1555.6
ZnO	Crys on sapp	5200	2.122	2.600	942.3
LiNbO3	Thin film on diamond/Si	12000	4.898	6.000	408.3
GaAs	Z-cut +22.5deg	2763	1.128	1.382	1773.4
GaAs	<001>(110)	2868	1.171	1.434	1708.5
Frequency(Hz)	2.45E+09				
Max length(mm)	2.00E-03				

Table 1 – Limitation on the number of finger-pairs for various piezoelectric devices .

The number of finger pairs per chip determines the bandwidth of produced spectrum. Initial estimates are that the SAW correlator requires at least 4 finger-pairs per chip to properly "identify" the wave. However, the bandwidth of such a device is 600MHZ at 2.4GHz center frequency. Clearly, the ranges of this parameter and the physical length of the correlator effectually restrict the code sequence length. Thence the choice of both code length and chipping rate is a trade-off between these parameters.

For the design of the fixed SAW correlator radio, we will implement only error-detecting algorithms. We will not consider error-correcting codes, data encryption or compression algorithms. No data manipulation other than signal spreading will be done for the following reasons:

1. Proper choice of coding sequence will provide very good data recovery probability.
2. Spread spectrum concept in itself provides a certain degree of data scrambling since one cannot reconstruct the original data symbol without knowing the coding sequence. However, the use of a well-known sequence makes this method a weak protection from deliberate eavesdropping.

3.3.2 DSSS code families

The codes that have been traditionally employed for spread spectrum CDMA systems are maximal length, or *m*-sequences, and several variants of Gold and Kasami sequences. The IEEE 802.11 and 802.11b Wireless LAN standards use Barker codes and Complementary (Golay) Codes. Hadamard-Walsh codes are used in some of the cellular CDMA downlink (base station to mobile) channels. (Gold codes are also used in GPS phase detection, and the Barker codes had been used for timing and synchronization.)

The PN sequences are classified by the specific properties they manifest. Table 2 lists the "classic" PN code families used in DSSS systems, with lengths of $2^n - 1$, where $n = 4,14$. The *m*-sequences are unexcelled for their performance, but they provide only up to 60 orthogonal codes

for $n = 10$. Gold codes are not exactly orthogonal, however, the so-called Orthogonal Gold codes might prove sufficient. The Kasami codes and their properties will also be explored.

Code family	Code length								
	15	31	63	127	255	511	1023	2047	4095
m-sequence	2	6	6	18	16	48	60	60	60
Gold codes	nd	33	65	129	nd	130	130	130	nd
Small Kasami	4	nd	8	nd	16	nd	32	nd	64
Large Kasami	15	nd	65	nd	256	nd	130	nd	64

Nd=not defined

Table 2 – Some PN codes traditionally used in spread spectrum CDMA systems (taken from http://www.ee.oulu.fi/~kk/optim_codes_info.html, Dr. Kari Kakkainen).

Barker and Hadamard-Walsh codes provide the number of orthogonal codes equal to the length of the code. The Walsh codes are not deemed suitable since they are repetitive by nature and will produce numerous partial correlation spikes. Partial correlations of the shorter codes could hinder the resolution of the actual correlation peak even in the absence of other signals, and make it impossible when combined with other signals.

The Barker codes have particular auto-correlation properties that make them highly suitable for SAWs. However, it appears the Barker codes are known as one sequence for a given length, with the length up to 13 bits. The so-called extended Barker codes can be 16 bits long. This limits their applicability as a data spreading sequence. Yet, the Barker codes could be very useful for synchronization, identification and other similar purposes that require unambiguous correlation of single code.

Partial results of the preliminary analysis of the correlation functions for the the Gold, Kasami and *m*-sequences at lengths 15, 31, 63, and 127 are presented in Table 3. The numbers show the lower and upper bounds (as a fraction of the main auto-correlation peak) of the aperiodic auto-correlation function (AACF), periodic auto-correlation function (ACF), and the periodic Cross-Correlation Function (CCF) for each code family. (n/d = not defined).

Code family	Code length = 15				Code length = 31			
	#Codes	AACF	ACF	CCF	#Codes	AACF	ACF	CCF
M-sequences	2	-0.2,0.13	-0.07,-0.07	-0.33,0.5	6	-0.13,0.1	-0.03,0.03	-0.29,0.36
Gold	n/d				33	-0.29,0.26	-0.29,0.23	-0.29,0.23
Short Kasami	4	-0.27,0.2	-0.33,0.2	-0.33,0.2	n/d			
Large Kasami	15	-0.5,0.3	-0.6,0.5	-0.6,0.5	n/d			
Code family	Code length = 63				Code length = 127			
	#Codes	AACF	ACF	CCF	#Codes	AACF	ACF	CCF
M-sequences	6	-0.10,0.08	-0.02,-0.02	-0.27,0.37	18	-0.08,0.07	-0.01,-0.01	-0.32,0.18
Gold	65	-0.29,0.24	-0.27,0.24	-0.27,0.24	129	-0.16,0.15	-0.13,0.12	-0.13,0.12
Short Kasami	8	-0.17,0.16	-0.14,0.11	-0.14,0.11	n/d			
Large Kasami	65	-0.25,0.22	-0.27,0.24	-0.27,0.24	n/d			

Table 3 – Correlation properties of selected code families.

4. Phase 2

4.1 FSAW SYSTEM DESCRIPTION

The object of this design was to demonstrate the ability to receive and demodulate wireless data signals using SAW devices. The FSAW data acquisition system consists of a single transmitter and receiver. Bi-directional communication was not achieved by this system since it was not necessary to accomplish the main objective and would have required increased system complexity.

The system was capable of transmitting a packet containing data samples acquired from a variable resistance device. These packets were communicated at rates of no less than once per second and included information to detect errors in the received data e.g. CRC or checksum codes. The data was transmitted using direct sequence spread spectrum (DSSS) encoding with predetermined spreading codes. This wideband data signal modulated an RF carrier using binary phase shift keying (BPSK). The modulated signal was transmitted to the receiver which demodulated the signal using a SAW correlator. The system controller for the receiver processed the received data for user inspection on the output device.

The center frequency of the RF signal used in this system is a function of the SAW device itself. The SAW correlators used were built for a 31 chip code length and a center frequency of 2.433 GHz. The correlators are constructed with 30 finger pairs per chip which provides a maximum data rate of 2.616 Mbit/s as shown in Equation 1.

$$\frac{2.433\times10^{9}\ cycles}{s}\times\frac{1\ finger\ pair}{cycle}\times\frac{1\ chip}{30\ finger\ pairs}\times\frac{1\ bit}{31\ chips}=\frac{2.616\times10^{6}\ bits}{s}$$

Equation 1 – Data Rate

4.2 DESIGN PHILOSOPHY

The design approach taken in developing this system was to divide the functions performed by the system into several functional modules. These modules could then be assigned as individual tasks to be developed by the appropriate personnel. The requirements placed on each module are defined by a functional requirements document. Using this approach the modules could be developed separately and alternative methods for implementing individual functions could be investigated.

At a defined point in the development schedule integration of the modules occurred. Prior to integration a system interface diagram that clearly depicts the interconnections between modules was created with input from the module designers. The end result of the module integration was the initial prototype system. This system was laid out in a way that provides sufficient access to individual modules for performance testing and measurement of system parameters.

The initial prototype system was used for design verification and testing to create a performance baseline for subsequent hardware revisions to be compared with. Once this performance baseline had been established the entire design or subsets of the design are ready to be fabricated into the next phase of the hardware development cycle.

4.3 FSAW RECEIVER

Figure 10 is the system interface diagram for the FSAW Receiver. All the modules defined in the FSAW system requirements document are shown in this diagram as well as interconnects between modules.

The horizontal bar across the top is the power distribution module that provides the power supply voltages for all modules in the system as well as power control functionality to allow the system controller to apply or remove power from selected modules to conserve energy in certain operating modes.

From left to right the diagram shows the system controller, baseband processor, power detectors, bit discriminators, detector amplifiers, SAW correlators, RF splitter and low noise amplifiers.

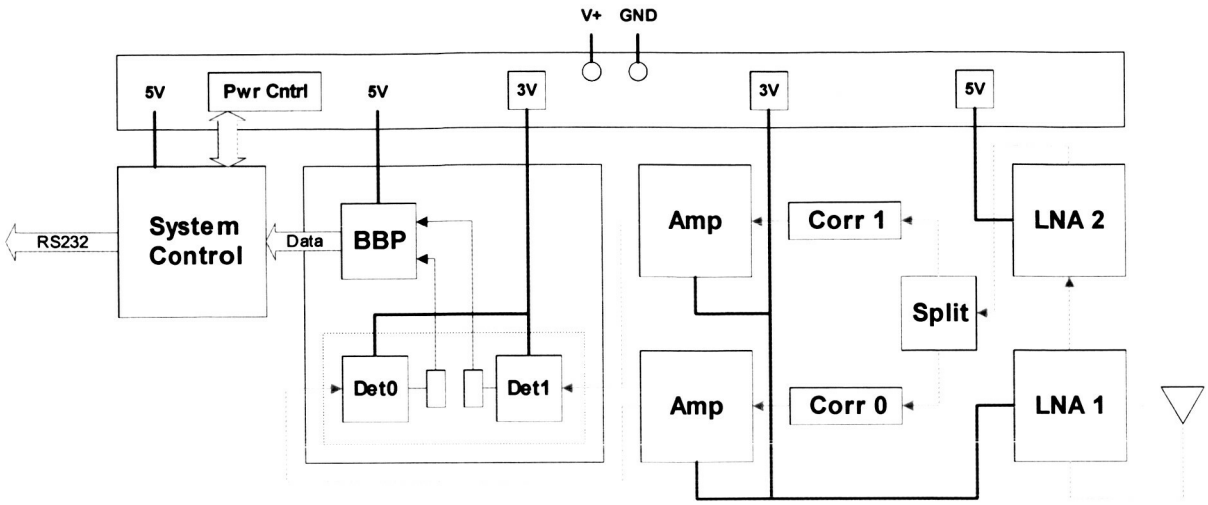

Figure 10 – FSAW Receiver

A description of the major components selected for each module of the receiver is contained in the following sections as well as individual test results for each module. The rational for the selection of components as well as alternative solutions that were evaluated are included where applicable.

4.3.1 Low noise amplifier (LNA)

The LNA selected is a very wideband device to accommodate the signal it receives. It also requires sufficient gain to offset the loss due to splitting the signal as well as the large insertion loss of the correlator.

4.3.2 Splitter

The splitter selected is a wideband passive RF splitter that is capable of accommodating the amplified received signal.

4.3.3 Saw Correlators

The SAW correlators were fabricated and packaged by program partner Sandia National Laboratories. The packaged correlators were mounted to a test fixture. Figure 11 below is a picture of a complete test fixture. The PN codes chosen for the correlators were the result of a "brute-force" algorithm designed to find pairs of codes that could be used together in the system.

4.3.3.1 Test Fixture

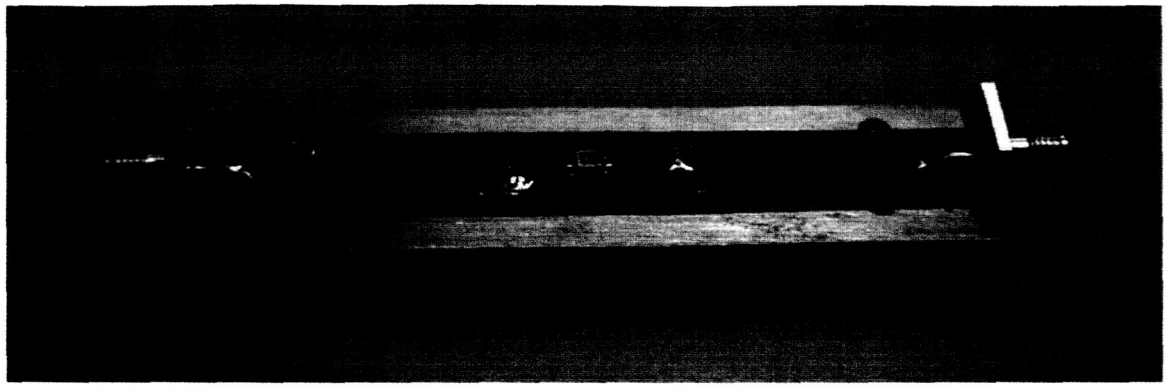

Figure 11 – SAW Correlator test fixture.

The test fixture is composed of SMA connectors, a PCB, and a brass block. The SMA connectors are a panel mount version that are mounted to the brass block screws and electrically connected to the PCB using either solder or conductive epoxy. The PCB was designed as a co-planar wave guide. A 50 ohm transmission line is used from the SMA connector to the SAW package. The length of the transmission line was designed to be half the wavelength of the desired center frequency. The substrate was chosen for its high dielectric constant which makes it very useful in impedance control circuits. No plating was used in the fabrication of the PCB to minimize the effects of uneven plating. Table 4 below shows the specifications for the PCB. The PCB is mounted to the brass block using conductive epoxy and screws.

Parameter	Specification
Thickness	0.031 in.
Material	Rogers RT/Duroid 5880
Copper Weight	1 oz.

Table 4 – SAW correlator test fixture PCB specifications

4.3.3.2 Code Search Algorithm

Early simulations revealed that that the correlators responded to the antipode[1] of a code almost identically to the original code. This meant that a single correlator could not be used if a positive indication of both a 1 and a 0 were required. However, two codes with good cross correlation properties could be used. The search began by selecting a set of codes from all possible 31 bit codes that met minimum criteria for both periodic and aperiodic auto correlation. Once the criteria were determined that produced a manageable set of codes, every possible pair of codes from that set was tested and the best performing pair was chosen. One of the codes in the chosen pair was an M-sequence and the other code did not belong to any known family. The performance of the codes is shown in Figure 12 through Figure 14. In these figures, the top signal is correlation of code A and the bottom signal is the correlation of code B. In Figure 12 the input is code A repeated back to back. In Figure 13 the input is code B repeated back to back. In Figure 14 the input is code A immediately followed by code B repeated back to back.

[1] The antipode of a code is the negative version of the code. For example [1 -1 1 -1 -1] is the antipode of [-1 1 -1 1 1].

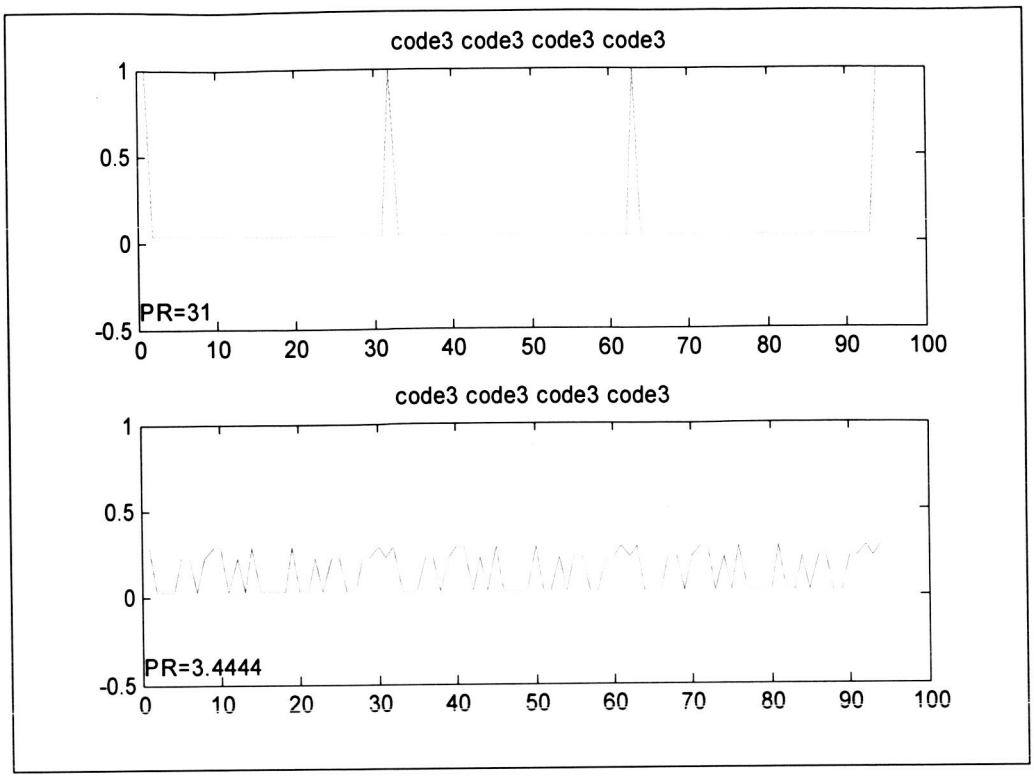

Figure 12 – Simulated correlation envelope from code A input.

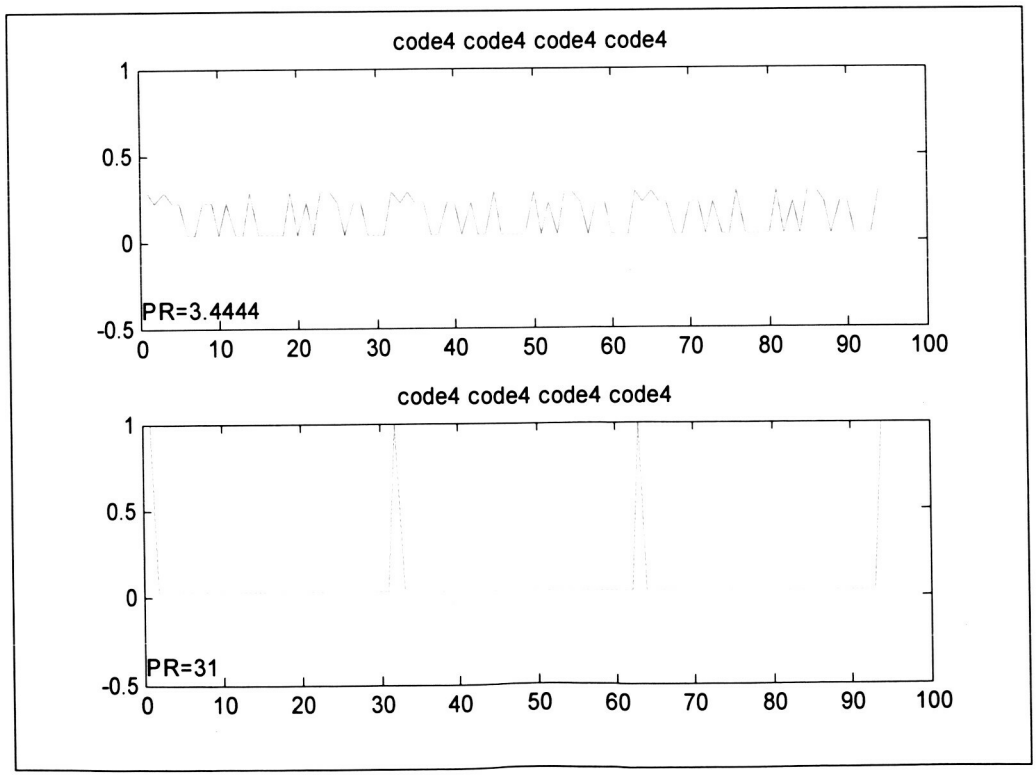

Figure 13 – Simulated correlation envelope from code B input.

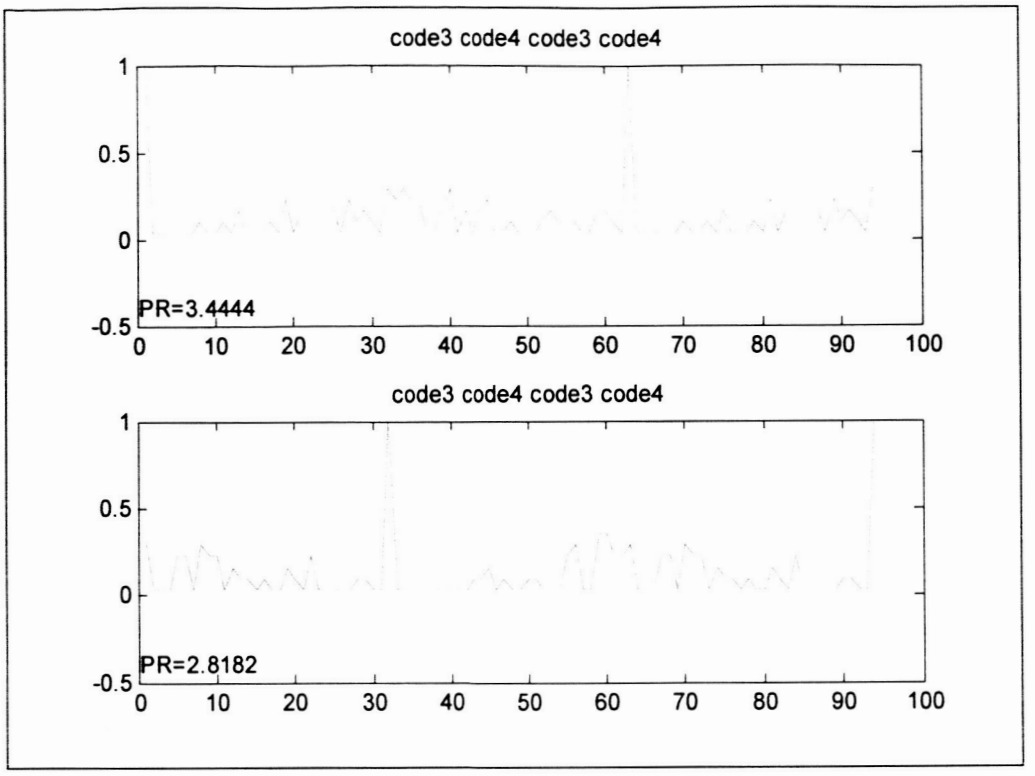

Figure 14 – Simulated correlation envelope from code AB input.

4.3.4 Detectors

The detector modules consist of two types of components as shown in Figure 15 (inside dotted line). The RF envelope detector converts the correlator output to a baseband signal that the bit decision circuit can use to make decisions as to whether or not a bit was received.

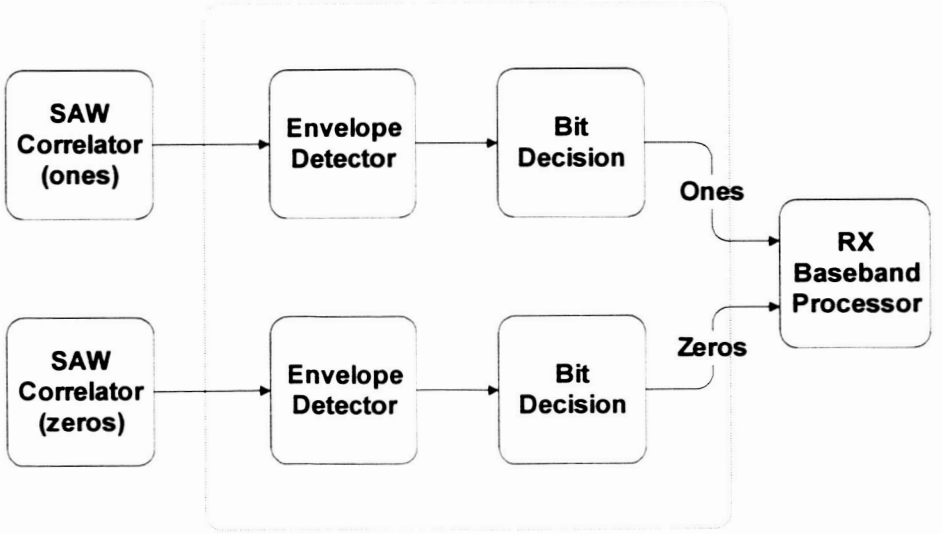

Figure 15 – FSAW Detector

4.3.5 RX Baseband Processor

The function of the receiver baseband processor is to interleave the two pulse streams received from the bit discriminators into a single serial bit stream that can be sent to the system controller. By performing this task outside of the system controller it frees up processing power and allows for the use of a lower power system controller in power sensitive applications. In order to benefit from such power savings the baseband processor must be low power itself. For this reason, the baseband processor has been implemented in a low power Xilinx CoolRunner-II CPLD with the corresponding coding done in VHDL.

The heart of the receiver baseband processor is a finite state machine that continuously monitors the inputs for incoming pulse streams. When pulses are detected it interleaves the two pulse streams into a standard SPI stream that is then sent to the system controller. In this design, the SPI slave select signal can also be thought of as a carrier sense signal that goes inactive after a programmed timeout is exceeded with no further reception of data.

While most high power processors can handle the ~2.6 Mbps data rate of this system, a number of very low power system controller options cannot processes such a data stream in a continuous fashion. One possible solution is to introduce a buffer into the baseband processor that can be written to at ~2.6 Mbps, but read from by the system controller at a slower rate. The only caveat to this solution is that the buffer must be able to hold an entire packet of data, which would need to be relatively small to fit into the available CPLD space. This is the solution employed by the current prototype baseband processor.

4.3.6 RX System Controller

The function of the receiver system controller is to decode and display incoming packets from the baseband processor. This includes removing any header information and confirming that the CRC is valid. Valid data is then displayed in a PC terminal window via a standard RS-232 link. Because this is intended as a low power design, the Texas Instruments MSP430 micro-controller has been chosen to demonstrate the functions of the system controller. While it is one of the lowest power micro-controllers available today, it should be noted that higher power processors could be used in its place for higher performance applications.

As mentioned above, a number of low power system controller options cannot handle the ~2.6 Mbps data rate of this system. After initial testing, it has been determined that the MSP430 micro-controller requires the use of a buffer in order to handle this data rate. For this reason, a small buffer has been placed in the baseband processor for this prototype.

4.3.7 RX Power Distribution Module

The RX power distribution module uses a single DC power supply input generates all the voltages necessary for the receiver components. Some supply voltages may also be enabled or disabled by the system controller as necessary to conserve power.

4.3.8 RX Integration Test Results

The FSAW receiver was assembled in a breadboard manner to ease testability and shorten development times. A photo of the assembly is shown in Figure 16

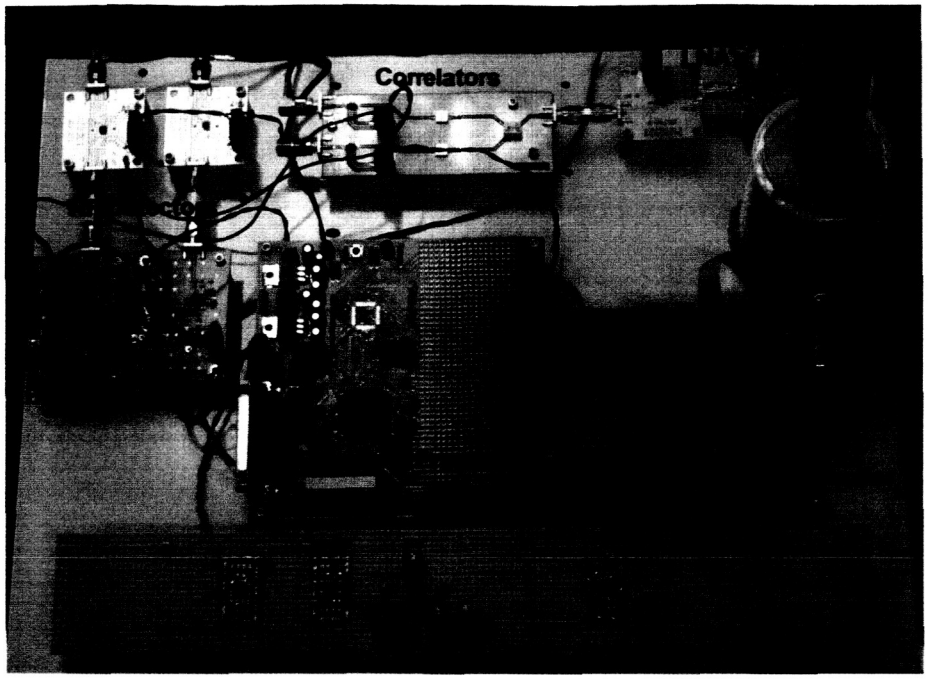

Figure 16 – 2.4GHz FSAW Receiver Assembly

An integration test plan was written and executed for the FSAW system. This test plan was designed to measure signal levels, time domain waveforms, and frequency spectrums at all measurable points in the transmit and receive signal paths at several operating ranges. Receiver sensitivity and dynamic range were the two most important quantities measured in this test. Figure 17 demonstrates receiver performance by displaying the packet error rate vs. signal power measured at the receiver input port. This chart shows that the receiver performs well at signal levels as low as -54 dBm and has a dynamic range of nearly 50 dB.

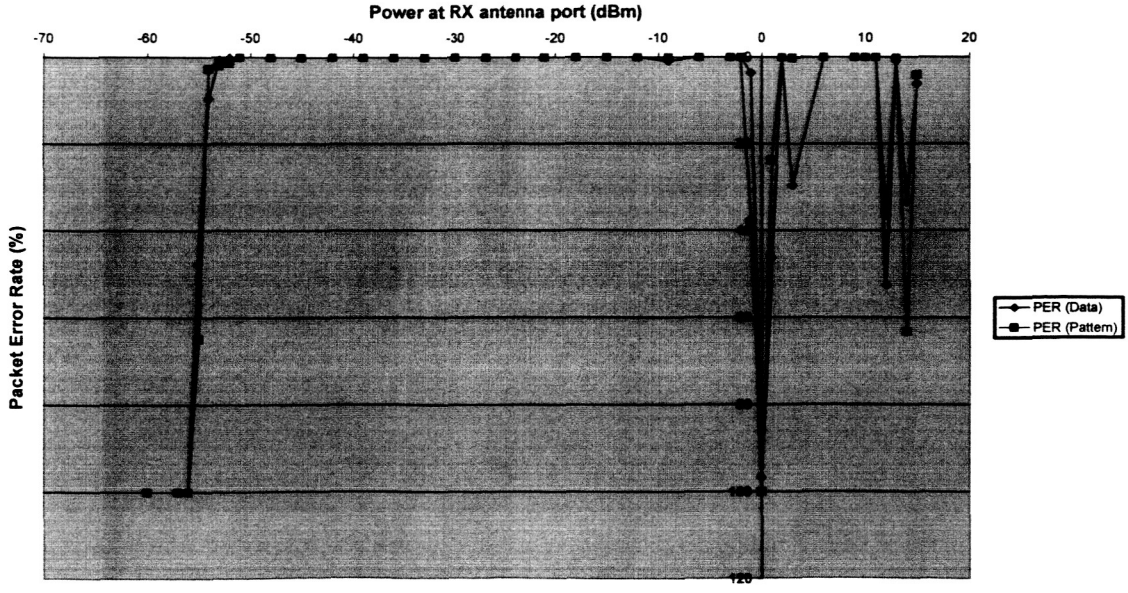

Figure 17 – 2.4GHz FSAW Receiver Performance

4.4 FSAW TRANSMITTER

Figure 18 is the system interface diagram for the FSAW Transmitter. All the modules defined in the FSAW system requirements document are shown in this diagram as well as interconnects between modules.

The horizontal bar across the top is the power distribution module which provides the power supply voltages for all modules in the system as well as power control functionality to allow the system controller to apply or remove power from selected modules to conserve energy in certain operating modes.

From left to right the diagram shows the system controller, RF Synthesizer, baseband processor, BPSK modulator, and TX power amplifier.

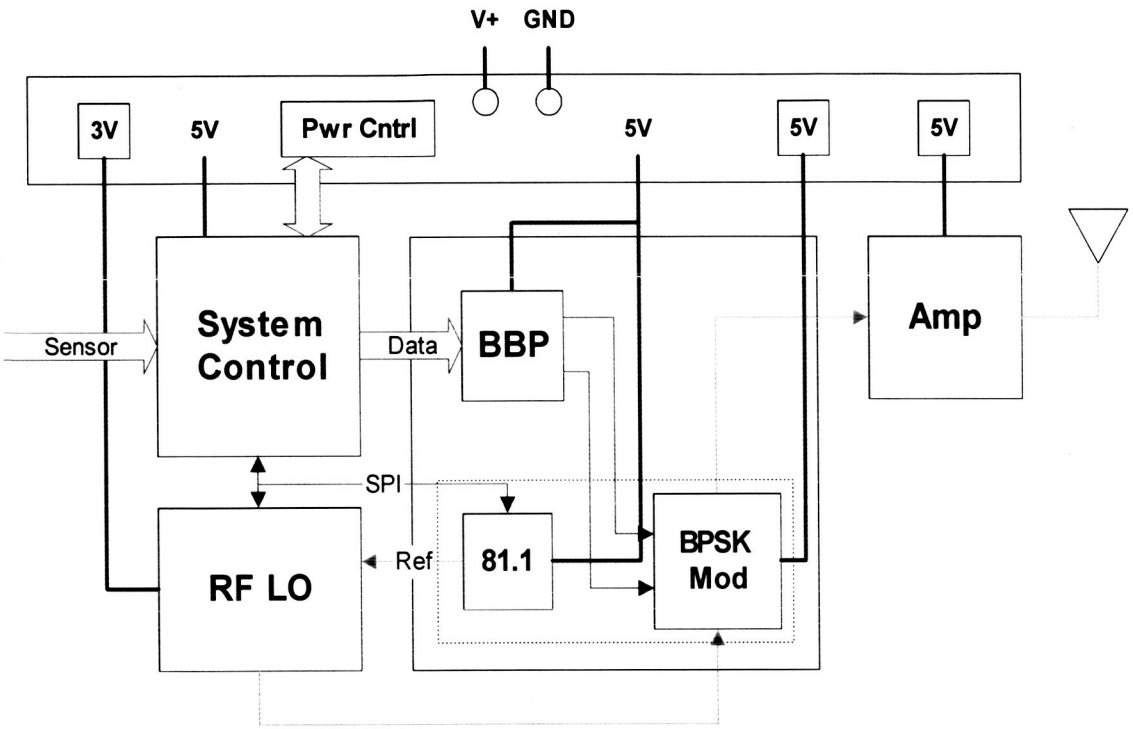

Figure 18 – FSAW Transmitter

A description of the major components selected for each module of the transmitter is contained in the following sections as well as individual test results for each module. The rationale for the selection of components as well as alternative solutions that were evaluated is included where applicable.

4.4.1 Sensor

The sensor module for the FSAW transmitter is capable of acquiring data samples from a transducer and transferring them over the sensor interface to the TX System Controller.

4.4.2 TX System Controller

The function of the transmitter system controller is to perform periodic data acquisitions, packetize the data, and send it to the transmitter baseband processor. In addition, for this prototype unit, it must provide testing functions such as the ability to transmit raw data or test

packets and the ability to measure RF power. As with the receiver system controller, user interaction is through a PC terminal window via a standard RS-232 link. The same design considerations were used in choosing the Texas Instrument MSP430 micro-controller as the transmitter system controller as in the receiver system controller.

Upon power up, the system controller applies power to the remainder of the switched devices in the transmitter chain as well as programs the RF synthesizer. Once the power up sequence is complete, the transmitter system controller uses its on-chip 12-bit A/D converter to sample data at a user specified interval. For this prototype, the maximum sampling interval shall be no slower than once per second, but may be as fast as 32 times per second. Once the data is sampled, it is assembled into a packet with appropriate header information and a standard 16-bit CRC and sent to the baseband processor. As with the receiver system controller, the transmitter system controller requires the use of a buffer in the baseband processor.

For testing purposes, this prototype system controller includes provisions to transmit several types of test packets as deemed necessary by the engineering team. It may also include provisions to put the transmitter chain into a continuous transmission mode to facilitate the measurement of RF power.

4.4.3 Synthesizer

The synthesizer module is required to provide the 2.433 GHz carrier frequency that the BPSK modulator uses as well as the 81.1 MHz clock (Equation 2) that the TX baseband processor uses to clock out data at the spread spectrum chipping rate.

$$\frac{31\,chips}{1\,bit} \times \frac{2.616 \times 10^6\,bits}{s} = \frac{81.1 \times 10^6\,chips}{s}$$

Equation 2 – Chipping Rate

The synthesizer module is programmed by the TX System Controller via a serial programming interface and provides a lock detect output that indicates when its outputs are stabilized and locked to the programmed frequency.

4.4.4 TX Baseband Processor

The function of the transmitter baseband processor is to convert the incoming data stream from the system controller into the chipping stream required by the BPSK modulator. Based upon the same power and processing considerations as in the receiver baseband processor, the transmitter baseband processor is implemented in a low power Xilinx CoolRunner-II CPLD.

The transmitter baseband processor receives a chipping clock of ~81.1 MHz from the RF synthesizer, which is then divided down to generate the data clock of ~2.6 Mbps required by the system controller. In this design, the transmitter baseband processor acts as an SPI host with the transmitter system controller acting as an SPI slave. For each data bit provided by the system controller, the baseband processor outputs 31 chips representing either a binary 0 or binary 1 to the BPSK modulator.

As explained in the receiver baseband processor portion of this document, many low power system controller options are unable to support a continuous ~2.6 Mbps data rate. As a result, the transmitter baseband processor makes use of a small buffer to address this limitation.

4.4.5 BPSK Modulator

The BPSK Modulator modulates the RF carrier with the spread spectrum signal from the TX baseband processor. The interface between the baseband processor and the modulator requires some signal conditioning circuitry. The modulator baseband inputs are differential signals with an

internally generated bias voltage and the baseband processor outputs are 3.3V digital signals. Figure shows an example interface using a STQ-3016 QPSK modulator in BPSK mode applying the same signal to both I and Q inputs.

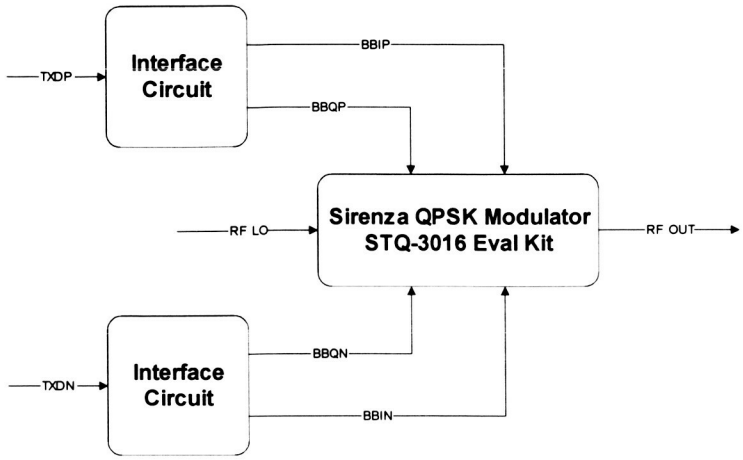

Figure 19 – BPSK Modulator Interface

4.4.6 TX Power Amplifier

The TX power amplifier is a wideband RF amplifier. This amplifier has a linear gain that boosts the modulated signal to the desired power level for transmission.

4.4.7 TX Power Distribution Module

The TX power distribution module uses a single DC power supply input which generates all the voltages necessary for the transmitter components. Some supply voltages may also be enabled or disabled by the system controller as necessary to conserve power.

4.4.8 TX Integration Test Results

The FSAW transmitter was assembled in a breadboard manner to ease testability and shorten development times. A photo of the assembly is shown in Figure 20.

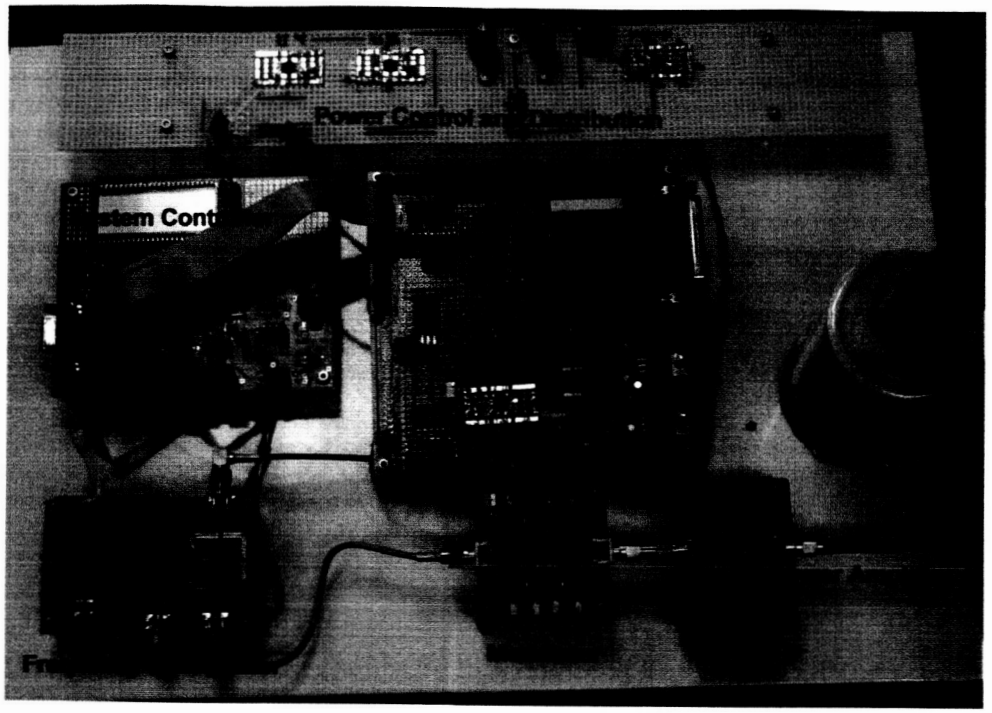

Figure 20 – 2.4GHz FSAW Transmitter Assembly

4.5 ALTERNATIVE TRANSMITTER DESIGN

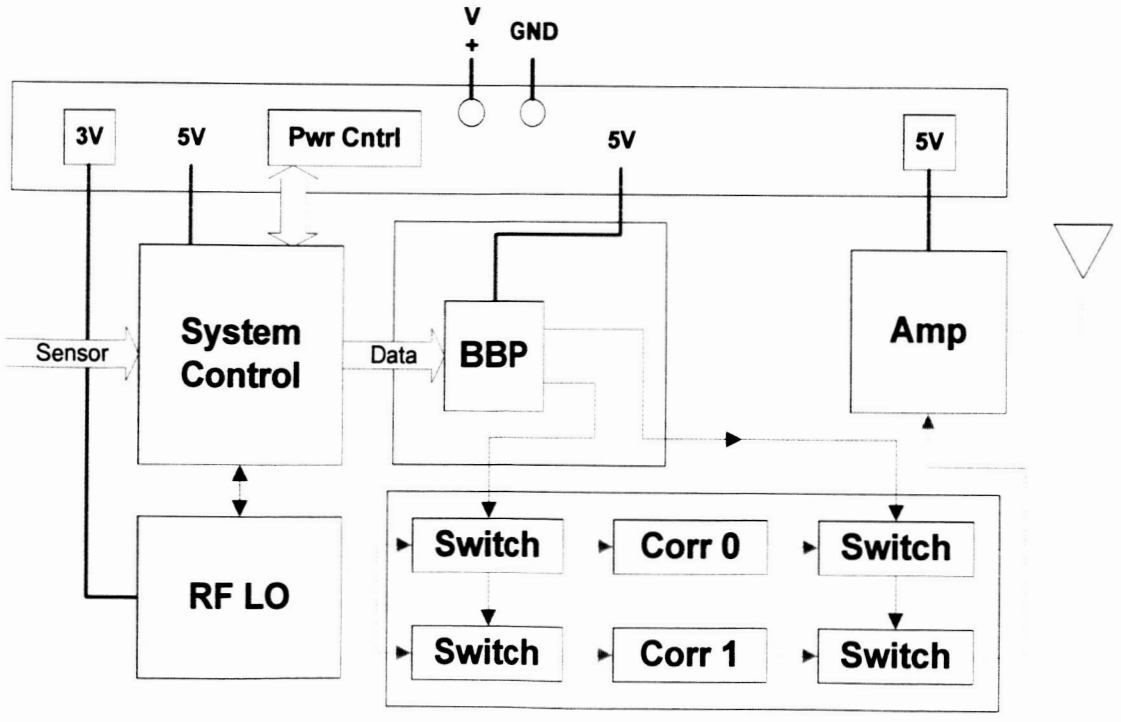

Figure 21 – SAW based transmitter.

A design similar to that shown in Figure 21 was initially considered. It is based on using a SAW correlator to produce the modulated RF waveform by exciting the correlator with several cycles of the proper center frequency. These correlators would be fabricated (or programmed for the programmable SAW) with the reverse of the codes used in the receiver. The RF local oscillator would be set for the proper center frequency. The baseband processor would either turn on the switch preceding the "0" correlator to transmit a "0" or turn on the switch preceding the "1" correlator to transmit a "1". The initial purpose of the switches on the output of the correlator was to avoid the inherent 3dB loss of using a combiner. The switch was later necessitated by the amount of "feed-through"[2] of the excitation signal that occurs. Table 5 below shows the results of testing a fixed SAW correlator using an RF pulse generator.

It is important to note that a correlator used as in this fashion does not have a continuous signal as its input. Consequently, some of the Insertion Loss listed is due to this fact. The information is presented to illustrate the large difference between the desired signal ~-44dB and the undesired signal ~-20dB.

Input(V)	FeedThru(mV)	Isolation (dB)	Signal (mV)	Insertion Loss (dB)
1.0	94	-20.5	6.5	-43.7
1.1	107	-20.2	7	-43.9
1.2	118	-20.1	7.5	-44.1
1.3	135	-19.7	8	-44.2
1.4	146	-19.6	8.5	-44.3
1.5	157	-19.6	9	-44.4
1.6	170	-19.5	9	-45.0
1.7	187	-19.2	9.5	-45.1
1.8	201	-19.0	10	-45.1
1.9	210	-19.1	11	-44.7

Table 5 – Feedthrough test results

This design was the desired approach. However, it was set aside until the amount of feedthrough could be reduced. The feedthrough would have to be reduced to the point of not needing a switch on the output to "gate-out" the feedthrough to make this design viable. Using a switch in this manner would prevent sending the same bit twice without a gap between them.

4.6 ALTERNATE COMMUNICATIONS SYSTEM DESIGNS

Before deciding on a particular overall communications system design, several designs were considered. The benefits and challenges of each design were analyzed and one design was chosen for the initial effort. The following sections discuss the concepts of the 3 major designs that were considered. In each section, a discussion of the benefits, challenges, and concerns are presented. The final section discusses the choice of the initial communications system. Discussions about the performance of the communication system assume ideal transmitters and receivers. Discussions about the design of components of the system will be limited to what would be required regardless of the actual design of the component.

4.6.1 Code On/Off Keying

The concept of this communications system is to choose a single code that is used to transmit one of the two symbols. The other symbol is inferred by the absence of detection of the chosen code.

[2] Feedthrough is defined as the portion of the input signal that appears directly at the output without propagating through the device.

4.6.1.1 Benefits

This concept has the initial benefits of being a simpler RF section, at the expense of a more complicated digital section. Another initial benefit is lower power because the component count would be lower. We determined that these initial benefits would go away or become negligible as the SAW and RF technology involved becomes more advanced. Meaning that as we approached the ideal ultra low-power radio, this method would require more power than the other methods and be more complicated.

4.6.1.2 Challenges and Concerns

The digital section is more complicated because the receiver needs to lock to the data rate to know when to latch the second symbol. When analyzing the processing gain from this approach, the aperiodic properties of the spreading code will dominate. The 31 bit codes that were chosen, if used in this method, would have processing gains of 15.8dB and 17.8dB. For reference, the processing gain of the same code used in a continuous transmit method would have a processing gain 29.8 dB.

4.6.2 Code Diversity Keying

The concept of this communications system is to choose two orthogonal codes each of which, respectively, are used to transmit the two symbols.

4.6.2.1 Benefits

This method yields its best performance when the two codes chosen are antipodes, and is more commonly known as antipodal signaling. However, since a SAW based receiver is inherently a non-coherent receiver, discrimination between the antipodes is not possible. To implement this method, two codes would have to be chosen that can be discriminated from each other (see Section 4.3.3.2). The main benefit of this method is that the receiver has a positive indication of the reception of both symbols. The processing gains from the two chosen codes used in this method are 10.7dB and 9.0dB. However, there is information content in the comparison of the two signals which would increase the processing gain. The actual amount of increase in processing gain is dependent on the method(s) used to compare the two signals. Initial estimates range from 15.0dB to 16.7dB

4.6.2.2 Challenges and Concerns

Because there are two nearly identical signal paths, more components will be required for the implementation. The design of a circuit to extract information content from the comparison of the two signals will be difficult.

4.6.3 Differential Code Diversity Keying

The concept of this communications scheme is to differentially encode the data before using the method described in section 4.6.2. In other words, one symbol is defined as the same phase between two consecutive correlations and the other symbol is defined as the opposite phase between two consecutive correlations. As in that method, the best performance of this method occurs when the codes chosen are antipodes. The key reason why a SAW can be used in this method is that the detection of the symbols is a comparison of the phase between two consecutive correlations.

4.6.3.1 Benefits

There are several methods to implement the receiver for this system, many of which use a single correlator. Although this method uses two signals, there is a single detector (a mixer) which gives positive pulses for one symbol and negative pulses for the other symbol.

4.6.3.2 Challenges and Concerns

This receiver requires the use of a mixer which will be difficult to find in low power versions. The Differential Delay Correlator version of the receiver will pose difficulties in the design and fabrication of the correlator element. A very closely controlled RF circuit design will be necessary to maintain the proper phase relationship of the two signals presented to the mixer.

5. Phase 3

The primary development goal of phase 3 was the progression from a fixed SAW correlator-based system to a system with a programmable SAW correlator-based architecture. The following sections describe the results of this development effort.

5.1 910 MHZ RF PSAW SYSTEM

The Phase 3 PSAW was designed to operate at a range of frequencies centered within the instrumentation, scientific, and medical (ISM) band at 900MHz.

5.1.1 System Description

The system transmits data using direct sequence spread spectrum (DSSS) encoding with predetermined spreading codes. This wideband data signal modulates an RF carrier using binary phase shift keying (BPSK). The modulated signal is transmitted to the receiver which demodulates the signal directly with a SAW correlator. The system controller for the receiver displays the received data for user inspection on the output interface.

The center frequency of the RF signal used in this system is a function of the physical construction of the PSAW device itself. The correlators were designed for a 31 chip code length and a center frequency of 910 MHz. The correlators were constructed with 13 finger pairs per chip which provides a maximum data rate of 2.258 Mbit/s as shown in Equation 3.

$$\frac{910\times10^{6}\ cycles}{s}\times\frac{1\ finger\ pair}{cycle}\times\frac{1\,chip}{13\ finger\ pairs}\times\frac{1\,bit}{31\,chips}=\frac{2.258\times10^{6}\ bits}{s}$$

Equation 3 – 910 MHz RF PSAW Data Rate

Figure 22 is a high level block diagram of the PSAW transceiver. The components inside the dotted line represent functions that are implemented on a single printed circuit board. These functions include the system controller, baseband processor, sensor interface, power control and distribution, RF frequency synthesis and interfaces for all the connected RF components. All components not implemented on the baseband/system controller board were implemented in the form of evaluation modules or prototype circuits for the individual parts.

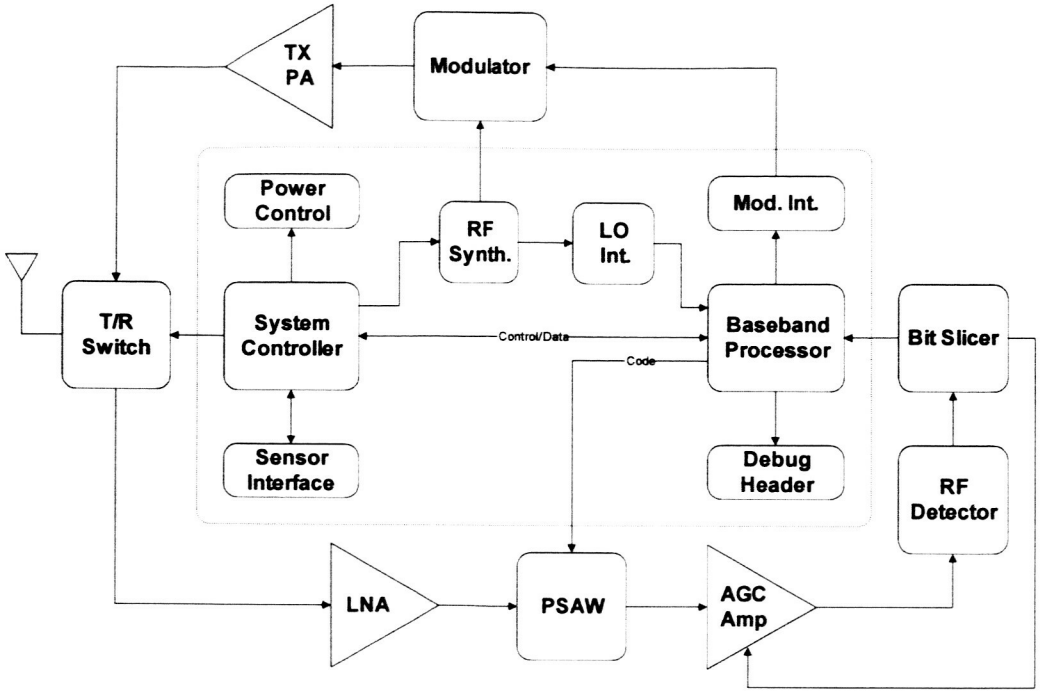

Figure 22 – 910 MHz RF PSAW Transceiver Block Diagram

The transceiver has 5 modes of operation. Transitions between operating modes are managed by the system controller and initiated through the user interface. A description of transceiver functionality for each mode is described as follows.

1. **Idle** - System controller and user interface are active. Remaining circuits are powered down or disabled.
2. **TX** - System controller, user interface, and transmit components are active. Remaining circuits are powered down or disabled.
3. **TX + Sampling** - System controller, user interface, transmit components, and sensor interface are active. Remaining circuits are powered down or disabled.
4. **RX** - System controller, user interface, and receive components are active. Remaining circuits are powered down or disabled.
5. **RX + Sampling** - System controller, user interface, receive components, and sensor interface are active. Remaining circuits are powered down or disabled.

5.1.2 Sensor Interface

The sensor interface for the PSAW transceiver is the analog-to-digital converter (ADC) integrated with the system controller. For demonstration purposes a potentiometer is placed on the system controller board to allow the voltage seen at the ADC input to be adjusted manually. If an external sensor is to be integrated with the system that sensor must provide its own signal conditioning and filtering as none is provided by the transceiver itself.

Property	Minimum	Nominal	Maximum
Sample Rate (samples/s)			250
Sample Width (bits)		12	

Table 6 – Data Acquisition Parameters

5.1.3 *RF Link Analysis*

A link analysis was performed to determine the gains required in the RF signal path. The transmitter is designed to radiate at a certain signal level and the receiver must be capable of receiving signals within a certain range of power levels. The lowest power level that the receiver can accept is defined as the receiver sensitivity and the difference between the highest and lowest power levels defines the receiver's dynamic range. Together these three parameters define the distances within which two transceivers can function reliably. Table 7 shows the target RF performance requirements for the PSAW transceivers.

Property	Minimum	Nominal	Maximum
Transmit Power (dBm)		14	
Receiver Sensitivity (dBm)		-65	
Receiver Dynamic Range (dB)	50		

Table 7 – RF Performance Requirements

Table 8 is an example link analysis for two transceivers spaced 50 meters apart. It is assumed that the AGC amplifier is designed to maintain a constant power input to the RF envelope detector of -25 dBm. As shown in the table the 50 meter separation corresponds to a media gain (loss) of -65.60 dB. If the distance were to increase to 100 meters the media gain would decrease to -71.62 dB. To maintain the same detector input the AGC amp would need to adjust its gain by 6.02 dB. The AGC amplifier can adjust its gain up or down within its dynamic range to compensate for different input power levels at the receiver. Thus the dynamic range for the PSAW receiver is a combination of the AGC amplifier dynamic range and the dynamic range of the bit slicer once the AGC has reached its limits.

The receiver sensitivity is measured at the RX LNA input. In the 50 meter example of Table 8 the LNA input is -57.6 dBm. To meet the requirement of -65 dBm sensitivity the AGC amplifier must be capable of an adjustment of an additional 7.4 dB or a total gain of 40.1 dB. This implies that to reach the desired -65 dB sensitivity the receiver must have a total gain (LNA + AGC) of 75.1 dB. Care was taken to ensure that no amplifiers used in the receive path will saturate over the desired range of received signals or the receiver performance would be degraded.

System Component	Gain		Test Point	Value
			Modulator Output (dBm)	0.00
TX PA (dB)	14		TX PA Output (dBm)	14.00
TX Antenna (dBi)	-3		TX Antenna output (dBm)	11.00
Media (dB)	-65.60		RX Antenna Input (dBm)	-54.60
RX Antenna (dBi)	-3		RX LNA Input (dBm)	-57.60
RX LNA (dB)	35		Correlator Input (dBm)	-22.60
Correlator (dB)	-35		AGC Input (dBm)	-57.60
AGC amp (dB)	32.7		Detector Input (dBm)	-24.90
Detector sensitivity (V/mW)	0.8		Detector output (Vpp)	0.003
Bit slicer amp (V/V)	50		Bit slicer amp output (Vpp)	0.129
AGC control amp (V/V)	5		AGC control (Vpp)	0.647

Table 8 – 910 MHz RF PSAW Link Analysis at 50 meters

5.1.4 *Antenna Interface*

Transmit and receive modes use a common antenna. This is accomplished by using an RF multiplexer to switch the antenna between transmit and receive paths. The paths are switched by the system controller when transitioning between operational modes.

5.1.5 *Receiver*

The diagram in Figure 23 shows the PSAW transceiver components that are active when the device is receiving data. The operating individual receiver components are detailed in the following sections. Input, output, power and performance parameters are documented where necessary.

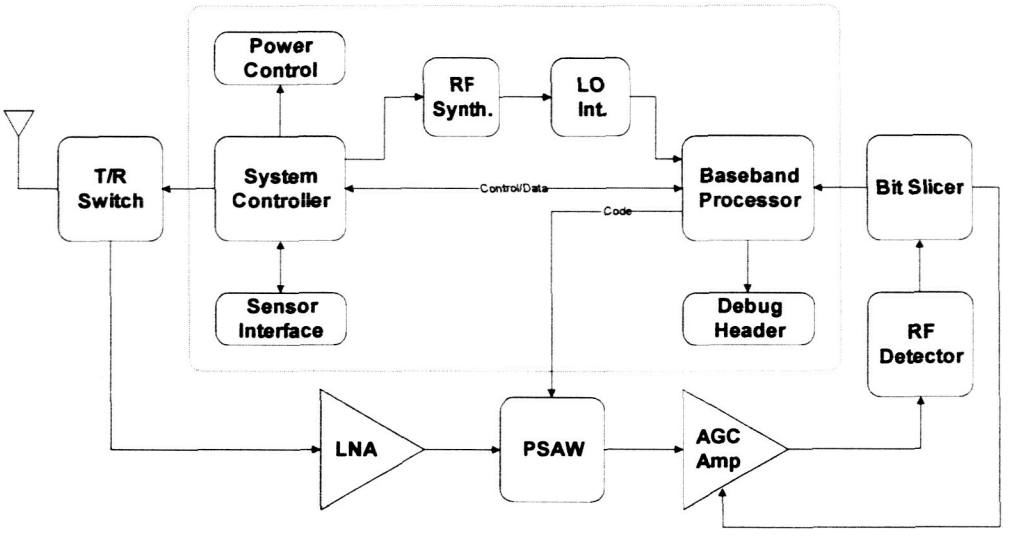

Figure 23 – 910 MHz RF PSAW Receive Mode

5.1.5.1 *Low noise amplifier (LNA)*

The LNA selected must be a very wideband device to accommodate the signal it receives. It also requires sufficient gain to offset the loss due to the large insertion loss of the correlator. The LNA selected for the 910 MHz RF PSAW system was a two stage amplifier design with over 35 dB of gain.

Property	Minimum	Nominal	Maximum
Input Impedance		50 ohm	
Output Impedance		50 ohm	
Operating Frequency (MHz)	800-1000		
Noise Figure (dB)			2.5
Gain (dB)		35	
Input 1 dB compression	-15 dBm		

Table 9 – Performance Requirements for LNA

5.1.5.2 *PSAW Correlator*

The PSAW correlators used were built for a 31 chip code length and a center frequency of 910 MHz. The correlators are constructed with 13 finger pairs per chip which provides a maximum data rate of 2.258 Mbit/s as shown in Equation 3. The correlators can be programmed digitally with any code sequence of 31 bits in length. The programming sequence is set by the system

controller via output lines from the baseband processor. Figure 24 is a photo of a 910 MHz correlator mounted on a circuit card that was designed and fabricated for this system.

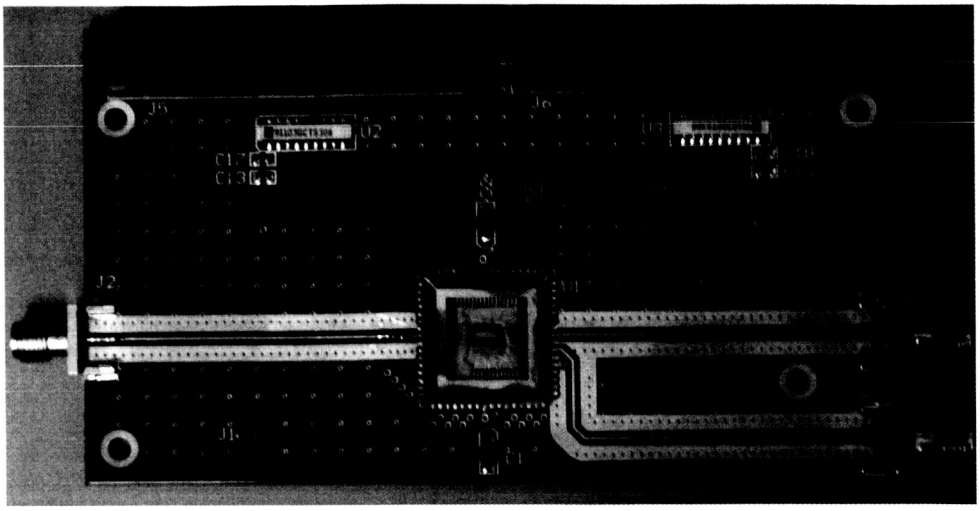

Figure 24 – 910 MHz RF Correlator PCB Assembly

5.1.5.3 AGC Amplifier

The AGC amplifier is used to maintain the input level of the RF detector at a near constant value. The control signal is an output of the bit slicer circuit that is properly conditioned to provide an adequately damped AGC output signal. The output of the AGC amp must settle to its steady state value within the 75% of the preamble sequence that is inserted at the beginning of each data packet. If the preamble length is 31 bits the response time of the AGC control loop must be no greater than 10.296 microseconds for any input power signal within its dynamic range.

$$\frac{s}{2.258\times10^{6}\,bits}\times\frac{31\,bits}{preamble}\times.75=10.296\mu s$$

Equation 4 – AGC response time example

Multiple gain stages may be required to meet the requirements of Table 10. These stages may include combinations of both fixed and variable gain amplifiers. The control voltage for the AGC amplifier should adjust the gain of the amplifier throughout its entire range which may include negative (dB) gain values if the amplifier is made up of more than one stage.

Property	Minimum	Nominal	Maximum
Input Impedance		50 ohm	
Output Impedance		50 ohm	
Operating Frequency (MHz)	800-1000		
Noise Figure (dB)			4.0
Gain (dB)	0		40
Input 1 dB compression	-5 dBm		
Control Voltage (V)	0		

Table 10 – Performance Requirements for AGC Amplifier

5.1.5.4 RF Detector

The output of the correlator consists of bursts of RF energy at the SAW devices resonant frequency that peak when a correlation occurs. The RF detector component in the receiver acts as a squaring rectifier when its diode is operated in the "square law" region. The detector also has limited output bandwidth based on its capacitance which makes it a good envelope detector for the correlator output.

Detectors of this type generally do not have a very large dynamic range. At the upper end of the range the diode starts to deviate from its square law region and noise sets the sensitivity limit at the lower end.

Property	Minimum	Nominal	Maximum
Input Impedance		50 ohm	
Operating Frequency (MHz)	800-1000		
Sensitivity (mV/mW)	700		
TSS (dBm)			-40

Table 11 – Performance Requirements for RF Detector

5.1.5.5 Bit Slicer

The bit slicer used by the PSAW receiver functions identically to the one designed for the previous Phase 2 FSAW system. The bit slicer module performs as shown in Figure 25 (inside dotted line).

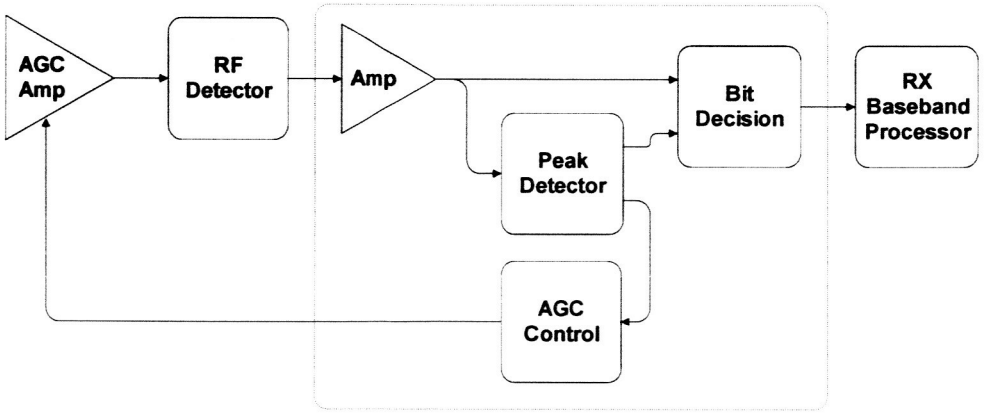

Figure 25 – Bit Slicer

The RF detector output has a nominal output level of around 2mV. The amplifier has a gain of 50 increasing this signal to a nominal 100mV. The peak detector tracks the peak amplitude of the incoming signal and uses the peak to create a threshold that the bit decision circuit compares with the original signal to determine if a bit was received. The peak detector output is also conditioned for use as the AGC amplifier control voltage. The bit slicer outputs a single digital pulse when a bit is detected.

5.1.5.6 RX Baseband Processor

The receive band has two data interfaces. The data receiver monitors digital inputs from the detector circuits. When a pulse is detected on these pins, the process of looking for a packet begins. When a start flag is found, the data is stored until a timeout between pulses occurs (signaling the end of a packet). The data is decoded using the 10B/8B standard line code. The READ_READY line is lowered signaling to the system controller that data can be read. It also

programs the PSAW device by holding the values given by the System Controller in the PSAW_REG.

Name		Description
Data Receive		
Inputs		
	RX_RAD0	Receive bit 0. Active high pulse indicating reception of a binary 0.
	RX_RAD1	Receive bit 1. Active high pulse indicating reception of a binary 1.
Controller interface		
Inputs		
	RESET	Baseband reset.
	READ_ENABLE	Active low signal used to put data on the bus.
Outputs		
	READ_READY	Active low when new data is ready to be read out.
	DATA(7:0)	Data bus for bytes to be read out.
PSAW interface		
Outputs		
	PSAW_REG(30:0)	PSAW register. Buffer that holds the program value for the PSAW device.
Controller interface		
Inputs		
	ADDRESS(1:0)	Address for each quarter of the PSAW register.
	PSAW_WRITE	Active low strobe for storing PSAW programming data to the proper address.
	DATA(7:0)	Shared data bus with receiver for receiving the PSAW register value.
General		
Inputs		
	CLK	Baseband clock (F_{chip} from synthesizer).

Table 12 – RX Baseband Processor I/O Signals

5.1.5.7 RX System Controller

The PSAW system controller accepts packetized data from the radio baseband processor, performs error detection, and displays the data for user inspection at the user interface. The output device is an RS-232 terminal to which text messages are written. The System Controller also sends the selected chipping code to the baseband processor for programming the PSAW device.

Name		Description
Power control		
Outputs		
	AMP_POWER	Power control for amplifiers.
	PSAW_POWER	Power control for PSAW
	DET_POWER	Power control for detector.
	T/R_POWER	Power control for T/R switch
	BB_POWER	Power control for baseband processor
	SENS_POWER	Power control for sensor
Baseband interface		
Inputs		
	READ_READY	Active low when new data is ready to be read out of baseband processor.
Outputs		
	RESET	Baseband Processor reset.
	READ_ENABLE	Active low signal used to put data on the bus.
	DATA(7:0)	Data bus for bytes to be read out.
PSAW interface		
Outputs		
	PSAW_ADD(1:0)	Address for each quarter of the PSAW register.
	PSAW_WRITE	Active low strobe for storing PSAW programming data to the proper address.
Output Device		
RS-232		RS-232 communication lines.
General		
	CLK	Controller clock (32.768KHz, internally converted to 8MHz).

Table 13 – RX System controller I/O Signals

5.1.5.8 RX Power Control/Distribution

This module accepts a single DC power supply input and provides all the voltages necessary for the receiver components. Some supply voltages may also be enabled and disabled by the system controller to conserve power. Care is taken when applying power to the receive components to avoid damaging or overstressing sensitive parts. The following sequence is followed when applying and removing power to the receiver.

Power up:

1. Enable power to baseband processor
2. Assert baseband RESET
3. Enable power to bit slicer
4. Enable power to PSAW
5. Enable power to RX amplifiers
6. Enable power to synthesizer
7. Verify synthesizer lock
8. Enable power to T/R switch
9. Assert RX mode on T/R switch
10. De-Assert baseband RESET

Power Down

1. Assert baseband RESET
2. Disable power to synthesizer
3. Disable power to RX amplifiers
4. Disable power to PSAW
5. Disable power to bit slicer
6. Disable power to T/R switch
7. Disable power to baseband processor

5.1.6 Transmitter

The diagram in Figure 26 shows the PSAW transceiver components that are active when the device is transmitting data. Operation of the transmitter components are detailed in the following sections. Input, output, power and performance parameters are documented where necessary.

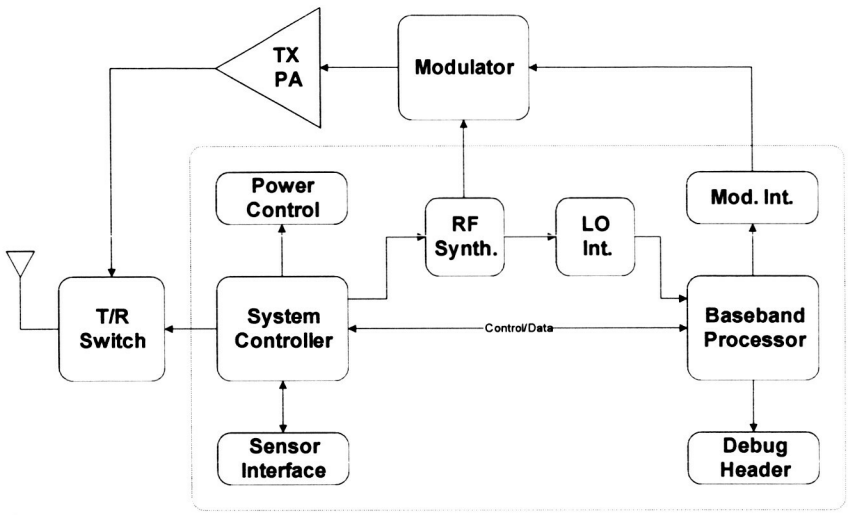

Figure 26 – 910 MHz Transmit Mode

5.1.6.1 TX System Controller

The TX system controller obtains sampled data from the sensor module and formats it into data packets with the appropriate encoding for the system protocol. These data packets are then transferred to the baseband processor over the transmit data interface.

Prior to initiating a data transmission the system controller must enable and initialize the components in the transmit path. This process occurs in the following sequence to ensure proper data transmission.

1. Enable power to T/R switch
2. Assert TX mode on T/R switch
3. Enable power to TX power amplifier
4. Enable power to Modulator
5. Enable power to baseband processor
6. Assert baseband RESET
7. Enable power to synthesizer
8. Verify synthesizer lock
9. Release baseband RESET
10. Transmit Data

Transmission begins when TX_STROBE goes low and ends when the transmit buffer is empty. The buffer can be loaded during transmission (as long as it is not full), allowing transmissions larger than the internal buffer size of the baseband processor. When data transmission is complete the controller shall disable the transmit components in the following manner.

1. De-assert TX mode on T/R switch
2. Assert baseband RESET
3. Disable power to synthesizer
4. Disable power to baseband processor
5. Disable power to Modulator
6. Disable power to TX power amplifier
7. Disable power to T/R switch

Name		Description
Power control		
Outputs		
	TX_POWER	Power control for transmit amplifiers.
	MOD_POWER	Power control for modulator.
	SYNTH_POWER	Power control for synthesizer
	T/R_POWER	Power control for T/R switch
	BB_POWER	Power control for baseband processor
	SENS_POWER	Power control for sensor
Synthesizer interface		
Inputs		
	SYNTH_LK_DET	Synthesizers lock detection. Active when locked on frequency.
Outputs		
	SYNTH_CLK	Transmit clock.
	SYNTH_MOSI	Transmit data. Valid on edge of SYNTH_CLK.
	SYNTH_SS	Slave select. Active when programming.
Baseband interface		
Inputs		
	BUFFER_FULL	Active low when baseband buffer is not full (ready for new data).
	TX_READY	Active low when data in buffer and transmit has not yet begun.
	TRANSMITTING	Active while transmitting is in progress.
	DATA(7:0)	Data bus to send data to transmit.
Outputs		
	RESET	Baseband processor reset.
	WRITE_STROBE	Active low strobe to write data into baseband buffer.
	TX_STROBE	Active low strobe to begin transmission.
	TEST_MODE	Active low signal for continuous transmission.
Output Device		
RS-232		RS-232 communication lines.
General		
	CLK	Controller clock (32.2KHz, internally converted to 8MHz).

Table 14 – TX System Controller I/O Signals

5.1.6.2 Synthesizer

The synthesizer module is required to provide the 910 MHz carrier frequency that the BPSK modulator uses as well as the 70 MHz clock (Equation 7) that the TX baseband processor uses to clock out data at the spread spectrum chipping rate.

$$\frac{910\times10^{6}\,cycles}{s}\times\frac{chip}{13\,cycles}=\frac{70\times10^{6}\,chips}{s}$$

Equation 5 – 910 MHz RF PSAW Chipping Rate

The synthesizer module is programmed by the TX System Controller via a serial programming interface and provides a lock detect output that indicates when its outputs are stabilized and locked to the programmed frequency.

Name		Description
Synthesized Outputs		
	F_{chip}	70 MHz chipping clock (3.3V CMOS)
	$F_{carrier}$	910 MHz carrier frequency (-6 dBm nominal)
Synthesizer Program		
Inputs		
	SYNTH_MOSI	Transmit Data. Valid on edge of SYNTH_CLK.
	SYNTH_CLK	Transmit Clock.
	SYNTH_SS	Chip Enable. Active when programming.
General		
Inputs		
	SYN_EN	Power control pin for transmit chain
Outputs		
	SYTH_LK_DET	Lock Detect. Active when locked on frequency.

Table 15 – Synthesizer I/O Signals

Synthesizer / Baseband Clock Interface

An interface circuit converts the low voltage AC coupled chipping frequency signal from the synthesizer to the CMOS compatible clock input required by the baseband processor. A simple comparator circuit accomplishes this by adding a bias voltage to the synthesizer signal and then comparing the biased version to the bias voltage itself. The output of this circuit is a square wave signal that swings nearly rail to rail (0 to Vcc) and is used as a baseband clock input.

5.1.6.3 TX Baseband Processor

At the request of the TX System Controller, the TX baseband Processor applies the proper spreading codes to the baseband data from the controller after encoding it with the 8B/10B line coding standard. These encoded bits or chips are then clocked out of the Baseband Processor to the BPSK modulator at the chipping rate clock provided by the synthesizer module.

Name		Description
Data Transmit		
Outputs		
	TX_RAD0	Transmit chip non-inverting.
	TX_RAD1	Transmit chip inverting.
Controller interface		
Inputs		
	RESET	Baseband reset.
	WRITE_STROBE	Active low strobe to write data into baseband buffer.
	TX_STROBE	Active low strobe to begin transmission.
	TEST_MODE	Active low signal for continuous transmission.
	DATA(7:0)	Data bus to receive data to transmit.
Outputs		
	TRANSMITTING	Active while transmitting is in progress.
	BUFFER_FULL	Active low when baseband buffer is not full (ready for new data).
	TX_READY	Active low when data in buffer is ready to transmit.
General		
Inputs		
	CLK	Baseband clock (F_{chip} from synthesizer).

Table 16 – TX Baseband Processor I/O Signals

Figure 10 is a simulated timing diagram of baseband processor signals at the beginning of a packet transmission.

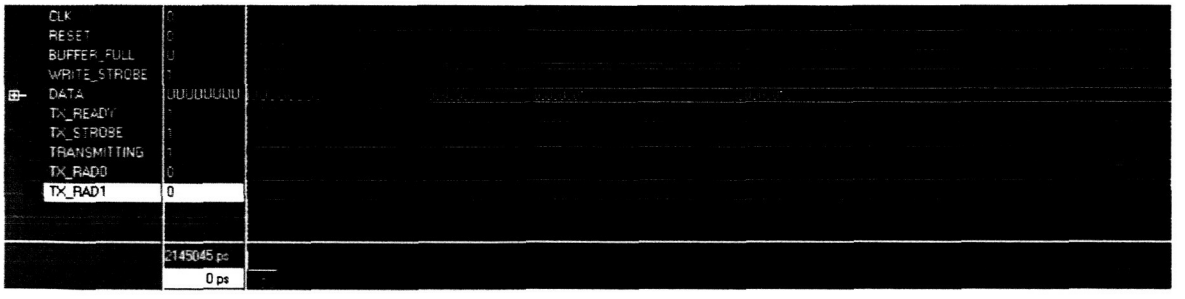

Figure 27 – TX Timing Diagram

5.1.6.4 BPSK Modulator

The BPSK Modulator modulates the RF carrier with the spread spectrum signal from the TX baseband processor. Its performance parameters are shown in Table 17.

Property	Minimum	Nominal	Maximum
Output Impedance		50 ohm	
Baseband Input Frequency (MHz)	DC	70	
Carrier Frequency (MHz)		910	
RF Output Power (dBm)		-12	

Table 17 – Performance Requirements for BPSK Modulator

5.1.6.5 TX Power Amplifier

The power amplifier used is a very wideband amplifier to accommodate the signal it will be transmitting.

Property	Minimum	Nominal	Maximum
Input Impedance		50 ohm	
Output Impedance		50 ohm	
Operating Frequency (MHz)	800-1000		
Gain (dB)	14		
Input 1 dB compression (dBm)	0		

Table 18 – Performance Parameters for TX PA

5.1.6.6 TX Power Control/Distribution

This module converts the DC power supply input to provide all the voltages necessary for the Transmitter components. Some supply voltages are also be enabled and disabled by the system controller to conserve power.

5.1.7 System Performance

The system design was completed to incorporate both receiver and transmitter on the same controller (transceiver) with minimal additional components. A controller board was designed and fabricated that integrates the system controller, baseband processor, RF synthesizer, power control circuitry and interfaces to other components. IVC assembled and tested two of these boards for use in 910 MHZ PSAW transceivers. One of the assembled units is shown in Figure 28.

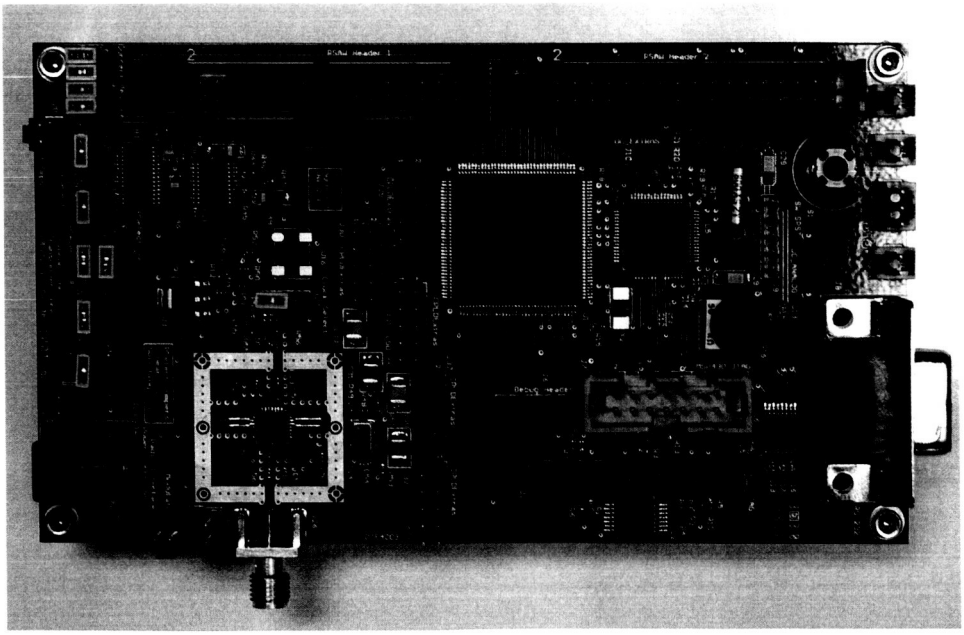

Figure 28 – System Controller PCB

5.1.7.1 910 MHz PSAW Device Simulation

A simulation method was developed to predict the performance of the 910 MHz PSAW devices. This model accounts for the effects of a driver IDT and losses due to attenuation within the correlator device itself. Model Parameters were adjusted so that the simulation results matched

actual device test data as closely as possible. The device test data was provided by Sandia using a 910 MHz device that they were able to mount and test successfully. Both the simulation results and the actual device test data indicate that the selected 31 bit m-sequence codes exhibit poor performance in these PSAW devices.

5.1.7.2 910 MHz PSAW Device Testing

IVC received two 910 MHz PSAW devices from Sandia. The first of these devices was mounted to the test board designed to accommodate the PSAW and tested. Results of those tests are presented below:

910 MHz PSAW #1

Testing of IVC's 900MHz PSAW board occurred before the correlator was mounted. All voltages measured as expected for all combinations of VCC = 3.3V & 5V and code = all 0s & all 1s. While compensating for pull-up resistors on the 'chip' pins, the test board consumed less than 1mA. During these tests, RF ports were connected to 50Ω terminations.

The 900MHz PSAW was attached to IVC's test board via electrically conductive epoxy. Again using 50Ω terminations on the RF ports, tests were performed. The bias voltage measured around 1.13V with a 5V source and around 1.04V with a 3.3V source. The system drew around 150mA at 3.3V and 0.5A at 5V. At these current levels, the correlator and test board experienced excessive heating. IVC stopped testing at this point and returned the device to Sandia for analysis. Testing at Sandia confirmed 5 times more current draw than a device Sandia had been testing. However, the devices functioned similarly. It was also noted that the device used by Sandia had a larger current draw than expected.

910 MHZ PSAW #2

IVC suspected that the wire bonding was incorrect and returned the device to Sandia. After removal of the lid it was confirmed that the wire bonding was incorrect. Repair of the device was attempted (with minimal chance of success) but was not successful.

Since IVC had not received a functional 910 MHz PSAW device to use in the system that was developed, a project review was scheduled to discuss the state of the program.

5.1.7.3 PSAW Project Review

A project review was held at IVC on October 30, 2003 with representatives from NASA, Sandia and IVC attending. Topics covered by IVC included:

- FSAW system test results;
- PSAW system design;
- PSAW component test results;
- PSAW simulation results; and
- Opportunities for future design improvements.

The Sandia presentation included PSAW device test results and detailed some of the technical challenges faced in 900 MHZ PSAW fabrication. A representative from NASA presented the results of the thermal testing conducted at JSC.

After discussing the results presented at this review a new course of action for the next step of PSAW development was proposed and mutually agreed upon. It was presumed that many of the performance shortcomings of the PSAW devices were caused by packaging difficulties that Sandia had encountered in fabricating devices at high frequency. To alleviate this requirement IVC proposed that a lower frequency PSAW could be used with the addition of RF Up/Down

conversion stages in the transmitter/receiver to maintain the 900 MHz RF frequency. This design approach became the focus of ongoing development.

5.2 183 MHZ IF PSAW SYSTEM

An operating frequency of 183 MHZ was chosen by Sandia to construct the IF (Intermediate Frequency) SAW devices. The transceiver system design was modified to include an RF to IF down conversion stage in the receiver. Additionally the change of the PSAW center frequency required a redesign of many components of the receive signal path. The following sections describe the unique components of the 183 MHz IF PSAW system in detail.

5.2.1 RX Topology Selection

A design effort was conducted to determine the optimum receiver topology for a 183 MHz IF PSAW device. The four receiver topologies considered are presented below. For each of these options part searches and performance comparisons were conducted. The criteria considered in selecting one of these options were performance, component availability, component count, power consumption, and miniaturization potential.

5.2.1.1 Option 1

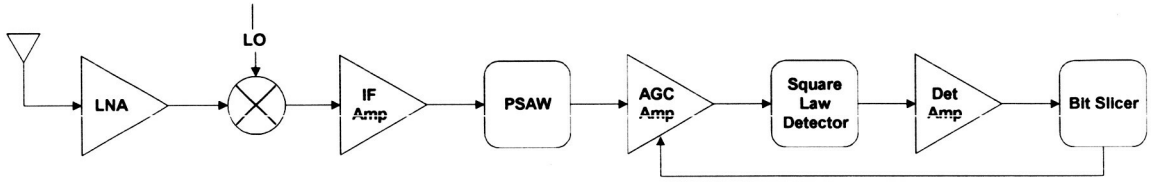

Figure 29 – Post SAW AGC with Square Law Detector

Pros	Cons
Similar to FSAW receiver system	High component count
	High power consumption
	AGC difficult to control

This option is the most similar to the 910 MHz RF PSAW receiver that was previously developed. A parts search for components to implement this design proved difficult as commercially available parts in the required frequency bands had significantly higher power consumption than those used in the FSAW design.

5.2.1.2 Option 2

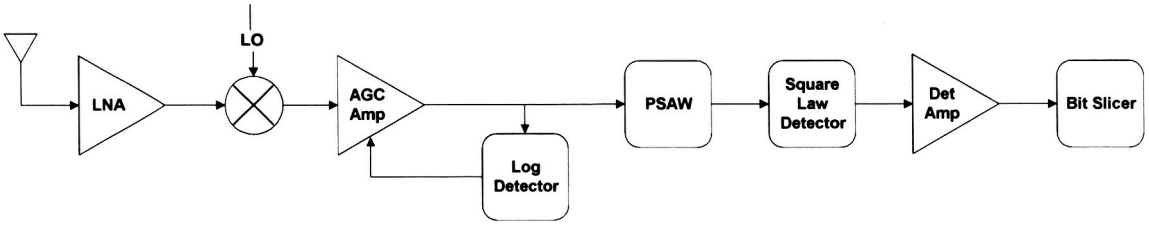

Figure 30 – Pre SAW AGC with Square Law Detector

Pros	Cons
Good dynamic range	High component count
Constant signal level into PSAW and detector	High power consumption
	Power tap required for AGC

Option 2 could prove to have better performance than option 1 due to the fact that the AGC control loop would have a faster response time and possibly improved dynamic range. However,

it would have the highest component count of all the design options considered and likely the highest power consumption as well.

5.2.1.3 Option 3

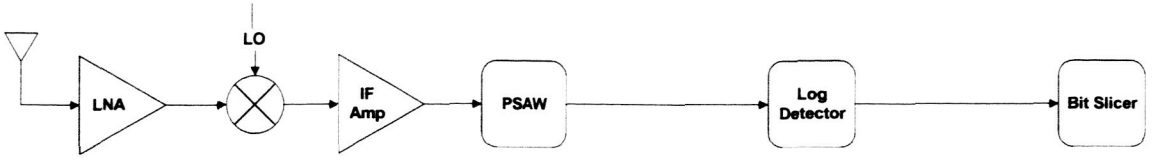

Figure 31 – No AGC with Log Detector

Pros	Cons
Low component count	Log detector distorts POP ratio
No detector amp required	
No AGC required	
Good dynamic range	

This design has many positive features but the POP (Peak to Off-Peak) ratio distortion caused by the log detector is unacceptable. The log detector provides an output voltage that varies linearly with logarithmic changes in input amplitude. Since the PSAW device output signal is amplitude modulated the resultant output of the log detector would have a POP ratio that is decreased by a log factor.

5.2.1.4 Option 4

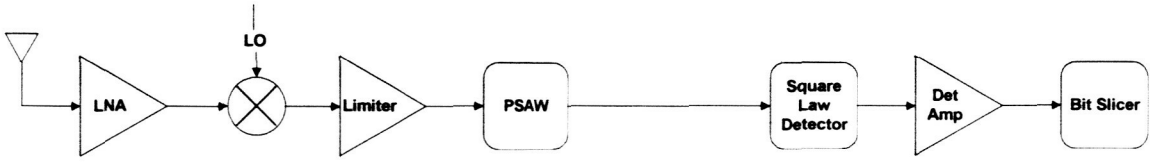

Figure 32 – Pre SAW Limiter with Square Law Detector

Pros	Cons
Good dynamic range	High power consumption
No AGC required	
Constant signal level into PSAW and detector	

Option 4 provides a low part count as well as a good dynamic range with no AGC required. These attributes are achieved by using a limiter amplifier on the phase modulated signal to provide a fixed signal level to the PSAW device and the detector. This limiter function does come at the cost of power consumption. The commercially available limiting amplifiers found were required more power than was desired but do have exceptional performance specifications.

5.2.1.5 Selection

The decision was made to pursue option 4 as the 183 MHz IF PSAW receiver's design. This option is the best design in terms of complexity versus performance. No feedback control is necessary to achieve the desired dynamic range and the overall component count is low. Future implementations of this design could greatly reduce its power consumption by combining many of the receiver functions onto custom integrated circuits specifically designed for the application.

5.2.2 *System Description*

The system transmits data using direct sequence spread spectrum (DSSS) encoding with predetermined spreading codes. This wideband data signal modulates an RF carrier using binary phase shift keying (BPSK). The modulated signal is transmitted to the receiver which down-converts the RF signal to an intermediate frequency (IF) at which the signal is demodulated using a SAW correlator. The system controller for the receiver displays the received data for user inspection on the output interface.

This transceiver is designed to operate in the 902-928 MHz ISM band at an RF center frequency of 915 MHz. Down conversion from RF to the IF frequency that the SAW correlator operates at is achieved with a mixer. The center frequency of the IF signal used in this system is a function of physical construction the PSAW device itself. The PSAW correlators that were used were built for a 31 chip code length and a center frequency of 183 MHz. The correlators are constructed with 17 finger pairs per chip which provides a maximum data rate of 347.25 kbit/s as shown in Equation 6.

$$\frac{183\times10^{6}\,cycles}{s}\times\frac{1\,finger\,pair}{cycle}\times\frac{1\,chip}{17\,finger\,pairs}\times\frac{1\,bit}{31\,chips}=\frac{347.25\,kbits}{s}$$

Equation 6 – 183 MHz IF PSAW Data Rate

Figure 33 is a high level block diagram of the 183 MHz IF PSAW transceiver. The components inside the dotted line represent functions that are implemented on a single printed circuit board. These functions include the system controller, baseband processor, sensor interface, power control and distribution, RF frequency synthesis and interfaces for all the connected RF components. All components not implemented on the baseband/system controller board were implemented in the form of evaluation modules or prototype circuits for the individual parts.

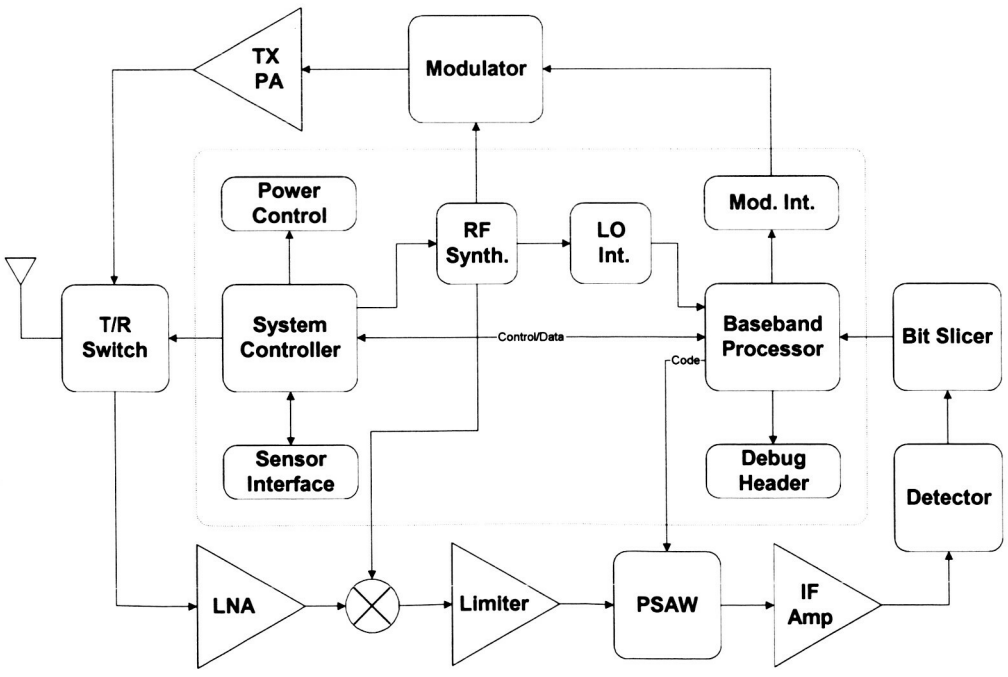

Figure 33 – 183 MHz IF PSAW Transceiver Block Diagram

5.2.3 *Sensor Interface*

Same as 910 MHz RF PSAW transceiver design.

5.2.4 *RF Link Analysis*

A link analysis was performed to determine the gains required in the RF signal path. The transmitter is designed to radiate at a certain signal level and the receiver must be capable of receiving signals within a certain range of power levels. The lowest power level that the receiver can accept is defined as the receiver sensitivity and the difference between the highest and lowest power levels defines the receivers' dynamic range. Together these three parameters define the distances within which two transceivers can function reliably. Table 19 shows the target RF performance requirements for the 183 MHz PSAW transceivers.

Property	Minimum	Nominal	Maximum
Transmit Power (dBm)		14	
Receiver Sensitivity (dBm)		-65	
Receiver Dynamic Range (dB)	50		

Table 19 – RF Performance Requirements

Table 20 is an example link analysis for two transceivers spaced 50 meters apart. It is assumed that the receiver is designed to maintain a constant power input to the RF envelope detector of −20 dBm. As shown in the table the 50 meter separation corresponds to a media gain (loss) of −65.65 dB. If the distance were to increase to 100 meters the media gain would decrease to −71.67 dB. Thus the dynamic range for the PSAW receiver is a direct function of the limiter amplifier's dynamic range.

The receiver sensitivity is measured at the RX LNA input. In the 50 meter example of Table 20 the LNA input is -57.65 dBm. To meet the requirement of -65 dBm sensitivity the limiter amplifier must be capable of accepting signal levels of an additional 7.35 dB less power. Care must be taken to ensure that no amplifiers used in the receive path will saturate over the desired range of received signals or the receiver performance will degrade.

System Component	Gain		Test Point	Value
			Modulator Output (dBm)	0.00
TX PA (dB)	14		TX PA Output (dBm)	14.00
TX Antenna (dBi)	-3		TX Antenna output (dBm)	11.00
Media (dB)	-65.65		RX Antenna Input (dBm)	-54.65
RX Antenna (dBi)	-3		RX LNA Input (dBm)	-57.65
LNA (dB)	19.5		Down Converter Input (dBm)	-38.15
RF Down Converter (dB)	0		Limiter Input (dBm)	-38.15
Limiter (dB)	100		Correlator Input (dBm)	-20.00
Correlator (dB)	-20		Correlator Output (dBm)	-40.00
IF amp (dB)	20		Detector Input (dBm)	-20.00
Detector sensitivity (V/mW)	0.1		Detector output (Vpp)	0.0010
Bit slicer amp (V/V)	50		Bit Slicer Input (Vpp)	0.0500

Table 20 – Link Analysis at 50 meters

5.2.5 *Antenna Interface*

Same as 910 MHz RF PSAW transceiver design.

5.2.6 *Receiver*

The diagram in Figure 34 shows the transceiver components that are active when the device is receiving data. The operating requirements for the receiver components are detailed in the following sections. Input, output, power and performance requirements are documented where necessary.

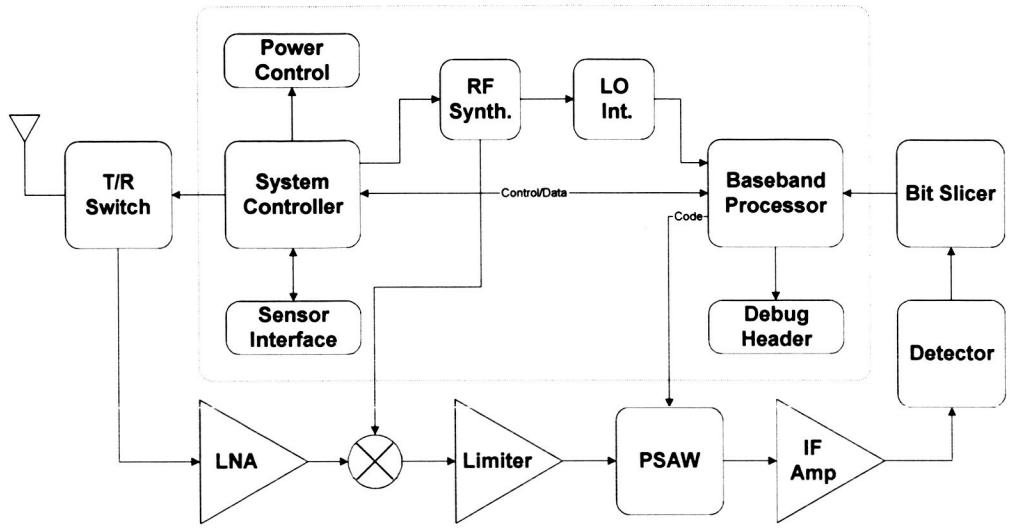

Figure 34 – 183 MHz IF PSAW Receive Mode

5.2.7 *Low noise amplifier (LNA)*

The LNA selected must be a very wideband device to accommodate the signal it receives. It also requires sufficient gain to offset the loss due to the large insertion loss of the correlator. The LNA selected for the 183 MHz IF PSAW system has over 15 dB of gain.

Property	Minimum	Nominal	Maximum
Input Impedance		50 ohm	
Output Impedance		50 ohm	
RF Frequency (MHz)	800-1000		
Noise Figure (dB)			2.5
Gain (dB)		15	
Input 1 dB compression	-15 dBm		

Table 21 – Performance Requirements for LNA

5.2.7.1 *RF Down Converter*

The RF down converter shifts the RF signal centered at 915MHz to an intermediate frequency (IF) centered at 183MHz. This is accomplished with a multiplier (mixer) component and appropriate filtering and gain to suppress the image signal from the mixer and any other mixer harmonics that are generated.

Property	Minimum	Nominal	Maximum
Input Impedance		50 ohm	
Output Impedance		50 ohm	
RF Frequency (MHz)		915	
IF Frequency (MHz)		183	
Gain (dB)		0	
Input 1 dB compression	0 dBm		

Table 22 – Performance Requirements for Down Converter

5.2.7.2 Limiter

The limiter amplifier is a high gain device that limits the amplitude of its output to a certain signal level regardless of input signal level. This type of non-linear operation is acceptable for a phase modulated signal because only the signal amplitude is distorted. The phase of the carrier is unaffected.

Property	Minimum	Nominal	Maximum
Input Impedance		50 ohm	
Output Impedance		50 ohm	
Output power (dBm)	-20		
Input sensitivity (dBm)	-65		

Table 23 – Performance Requirements for Limiter

5.2.7.3 PSAW Correlator

The PSAW correlators that will be used were built for a 31 chip code length and a center frequency of 183 MHz. The correlators are constructed with 17 finger pairs per chip which provides a maximum data rate of 347.25 kbit/s as shown in Equation 6. The correlators can be programmed digitally with any code sequence of 31 bits in length. The programming sequence is set by the system controller via output lines from the baseband processor. Figure 35 is a photo of a 183 MHz IF correlator mounted on a circuit card that was designed and fabricated for this system.

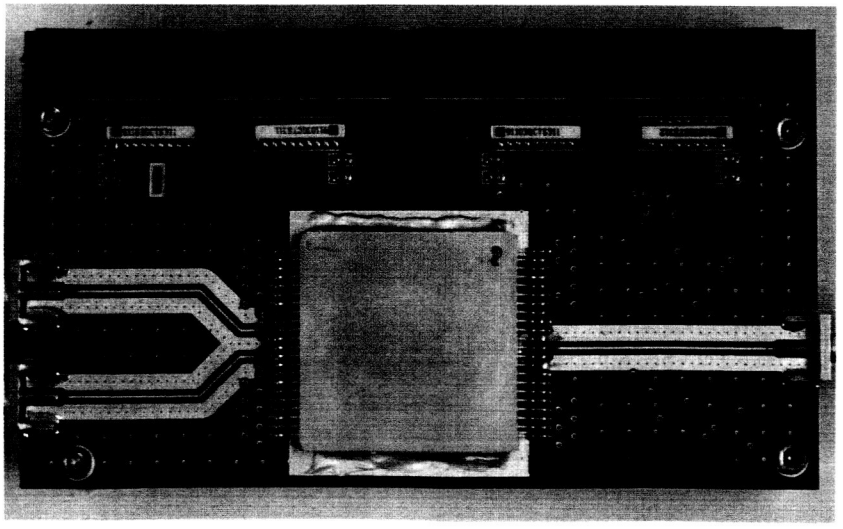

Figure 35 – 183 MHz IF Correlator PCB Assembly

5.2.7.4 IF Amplifier

An amplifier is required to maintain a signal level that is within the square law region of the detector.

Property	Minimum	Nominal	Maximum
Input Impedance		50 ohm	
Output Impedance		50 ohm	
Frequency (MHz)	160-210		
Gain (dB)		20	
Input 1 dB compression	-15 dBm		

Table 24 – Performance Requirements for IF Amplifier

5.2.7.5 Detector

The output of the correlator consists of bursts of RF energy at the SAW devices resonant frequency that peak when a correlation occurs. The RF detector component in the receiver acts as a squaring rectifier when its diode is operated in the "square law" region. The detector also has limited output bandwidth based on its capacitance which makes it a good envelope detector for the correlator output.

Detectors of this type generally do not have a very large dynamic range. At the upper end of the range the diode starts to deviate from its square law region, and noise sets the sensitivity limit at the lower end.

Property	Minimum	Nominal	Maximum
Input Impedance		50 ohm	
Operating Frequency (MHz)	160-210		
Sensitivity (mV/mW)	100		
TSS (dBm)			-40

Table 25 – Performance Requirements for IF Detector

The detector circuit used for the 183 MHz PSAW system was designed and simulated using the PSPICE circuit analysis software. A prototype of the circuit was then built and tested using simulated inputs that are modeled using the data rates and center frequencies that the PSAW device was designed to operate at. Figure 36 and Figure 37 are oscilloscope screen captures of the input (lower trace) and output (upper trace) signals from this test.

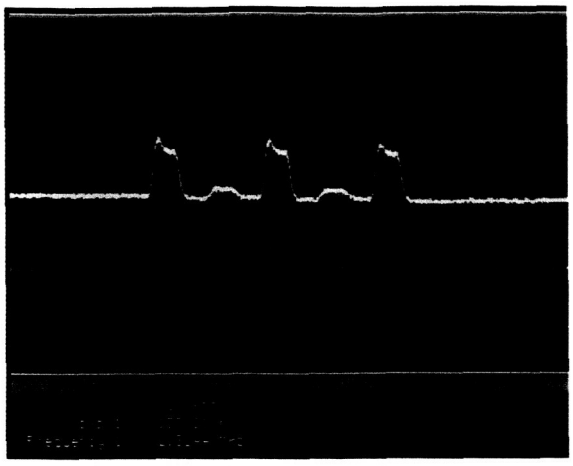

Figure 36 – IF Detector Signals A

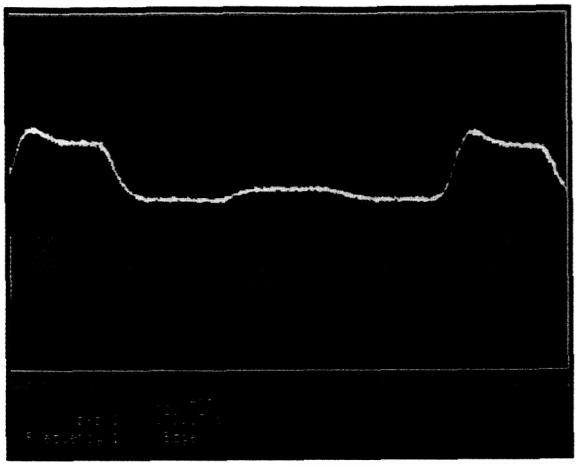

Figure 37 – IF Detector Signals B

These results show very good envelope detection and the squaring effect of the detector is illustrated by the difference in the peak to off peak ratios of the input and output signals.

5.2.7.6 Bit Slicer

Same as 910 MHz RF PSAW transceiver design.

5.2.7.7 RX Baseband Processor

Same as 910 MHz RF PSAW transceiver design.

5.2.7.8 RX System Controller

Same as 910 MHz RF PSAW transceiver design.

5.2.7.9 RX Power Control/Distribution

Same as 910 MHz RF PSAW transceiver design.

5.2.8 Transmitter

Same as 910 MHz RF PSAW transceiver design.

5.2.8.1 TX System Controller

Same as 910 MHz RF PSAW transceiver design.

5.2.8.2 Synthesizer

The synthesizer module is required to provide the 915 MHz carrier frequency that the BPSK modulator uses as well as the 53.8 MHz clock (Equation 7) that the TX baseband processor uses to clock out data at the spread spectrum chipping rate.

$$\frac{915\times10^{6}\,cycles}{s}\times\frac{chip}{17\,cycles}=\frac{53.82\times10^{6}\,chips}{s}$$

Equation 7 – 183 MHz IF PSAW Chipping Rate

5.2.8.3 TX Baseband Processor

Same as 910 MHz RF PSAW transceiver design.

5.2.8.4 BPSK Modulator

Same as 910 MHz RF PSAW transceiver design.

5.2.8.5 TX Power Amplifier

Same as 910 MHz RF PSAW transceiver design.

5.2.8.6 TX Power Control/Distribution

Same as 910 MHz RF PSAW transceiver design.

5.2.9 System Performance

5.2.9.1 183 MHz IF FSAW Devices

To expedite system testing Sandia delivered two 183 MHz fixed code SAW devices in the same package that was selected for the programmable SAWs. This allowed IVC to perform basic device and system testing and provide a benchmark for testing the PSAW devices against. Basic testing of the SAW measures the correlator output when data encoded with the matching code is input (autocorrelation). Figure 38 is a diagram of the test configuration used to measure the correlator response.

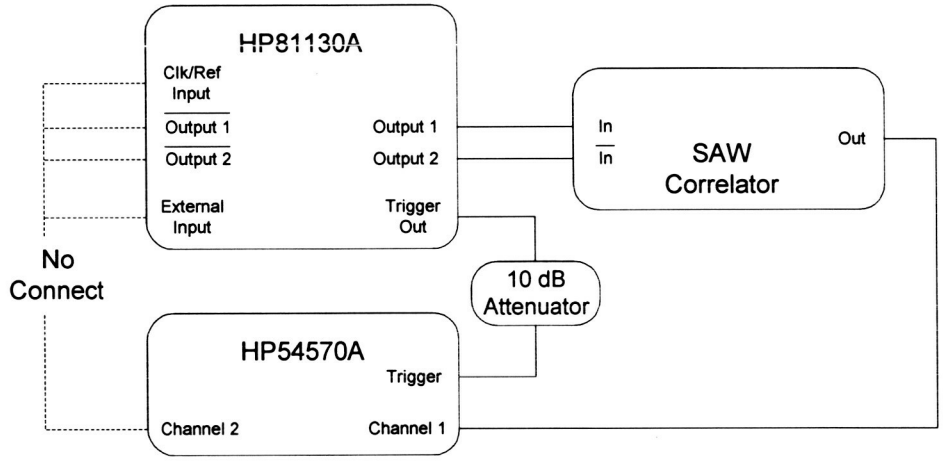

Figure 38 – IF FSAW Test Configuration

The correlation output was measured for both periodic and aperiodic input data. Periodic input simply refers to encoded bits transmitted continuously at the maximum data rate allowed by the chipping code. An aperiodic input is a single encoded bit preceded and followed by no signal. Figure 39 and Figure 40 show the periodic and aperiodic autocorrelation for a fixed code device using the code [11111001001100001011010100011110].

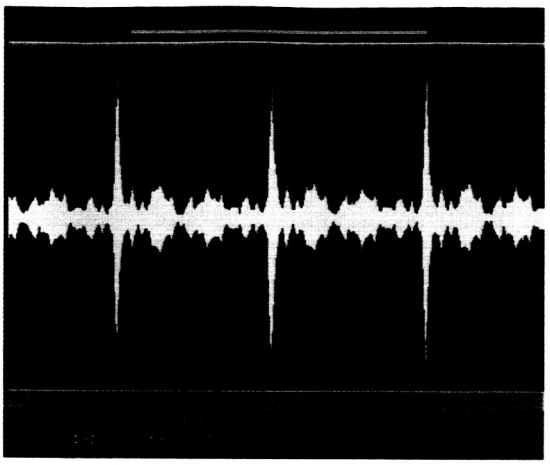

Figure 39 – IF FSAW Periodic Autocorrelation

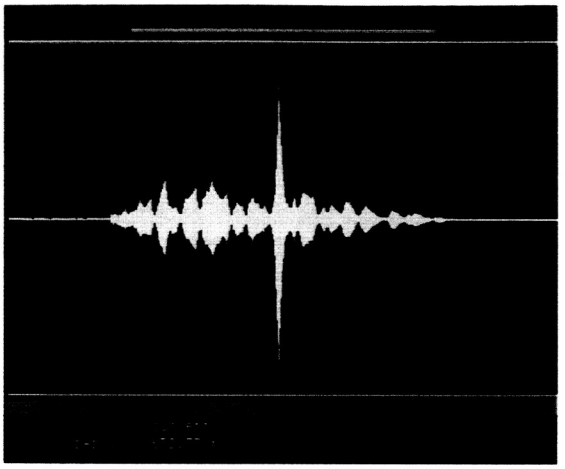

Figure 40 – IF FSAW Aperiodic Autocorrelation

As can be seen from the above figures, the FSAW devices exhibit a clean correlation peak with a peak to off peak (POP) ratio of greater than 3 to 1. The theoretical maximum value for the POP ratio of a 31 bit ideal correlator is 31.

A second measurement of correlator performance is correlator output when data encoded with a non-matching code is input (cross correlation). A code was selected that yields a low cross correlation with the FSAW code (in the ideal sense). The code sequence selected was [11111101111111111111111111111110], which ideally has a cross correlation of 4.43. Data encoded with this code was then alternated with the matching code to demonstrate the performance of the correlator in discriminating transitions between the two codes. The results of these tests are shown in Figure 41 and Figure 42.

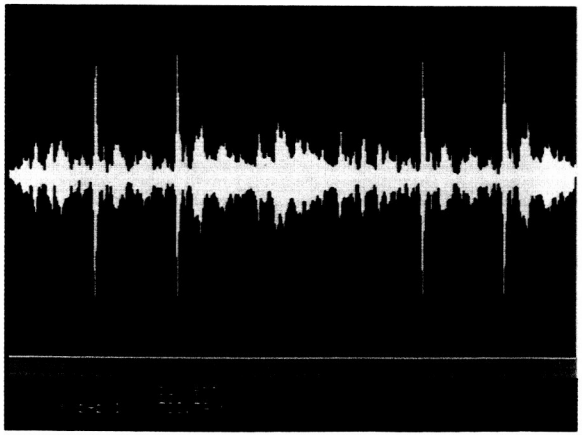

Figure 41 – IF FSAW Sequential Code Correlation

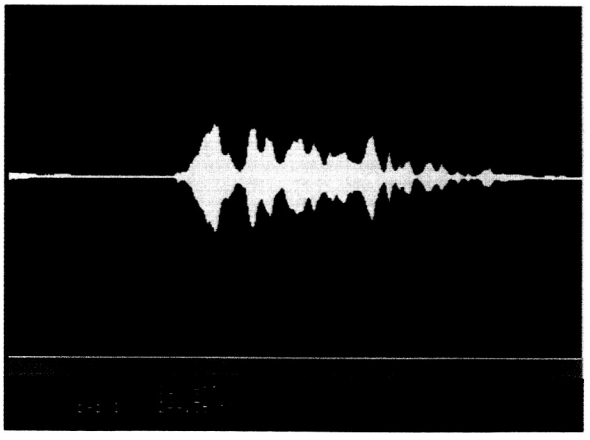

Figure 42 – IF FSAW Aperiodic Cross Correlation

Figure 41 shows that the cross correlation amplitude signal is larger than the auto correlation off peak signal for this code but the overall POP ratio for this signal is still nearly 3 to 1.

5.2.9.2 183 MHz IF PSAW Devices

Upon receiving two PSAW devices from Sandia basic correlator testing was performed to compare the performance of the PSAWs to the FSAW devices previously received. Figure 43 is a diagram of the test configuration used to measure the correlator response.

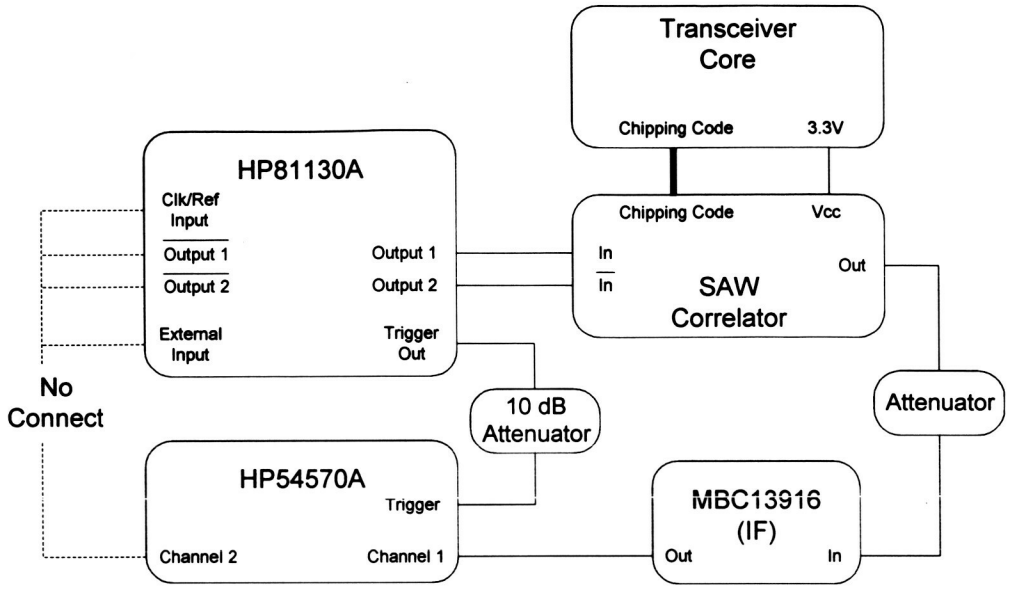

Figure 43 – IF PSAW Test Configuration

The MBC1396 IF amplifier and attenuator were required for this test because the PSAW devices had 15-20 dB less output signal than the FSAW devices for the same input signal. The IF amplifier provides the gain necessary to make up for this loss and present a similar input level to the oscilloscope measuring the correlation. Figure 44 and Figure 45 show the periodic and aperiodic autocorrelation for a PSAW device programmed with the same code as the previously tested FSAW devices.

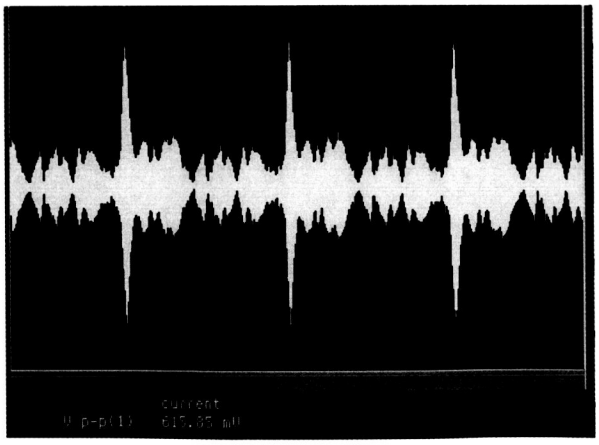

Figure 44 – IF PSAW Periodic Autocorrelation

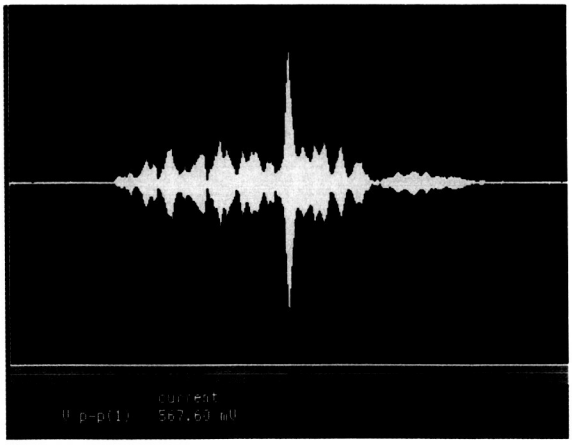

Figure 45 – IF PSAW Aperiodic Autocorrelation

As can be seen from the above figures, the PSAW devices exhibit a clean correlation peak with a peak to off peak (POP) ratio of nearly 3 to 1. This performance is similar to that seen in the FSAW devices for this code.

Cross correlation measurements for the IF PSAW devices are shown in Figure 46 and Figure 47.

Figure 46 – IF PSAW
Sequential Code Correlation

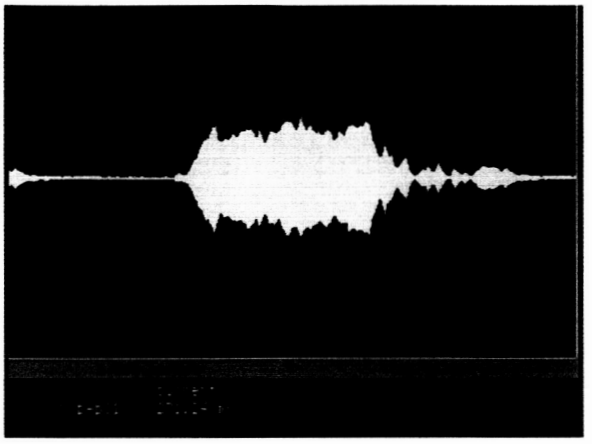

Figure 47 – IF PSAW
Aperiodic Cross Correlation

Compared to the same test in the IF FSAW device the PSAWs have a much worse cross correlation response for this code. This could cause false bit detection in a system that uses one code to represent a '1' bit and the other to represent a '0' bit.

5.2.9.3 Functional Testing

The system design was completed to incorporate both receiver and transmitter on the same controller (transceiver) with minimal additional components. This system used the same controller board that was designed for the 910 MHZ RF PSAW system (Figure 28). However, to facilitate testing and minimize parts separate receiver and transmitter units were constructed. Figure 48 and Figure 49 are photos of the constructed receiver and transmitter.

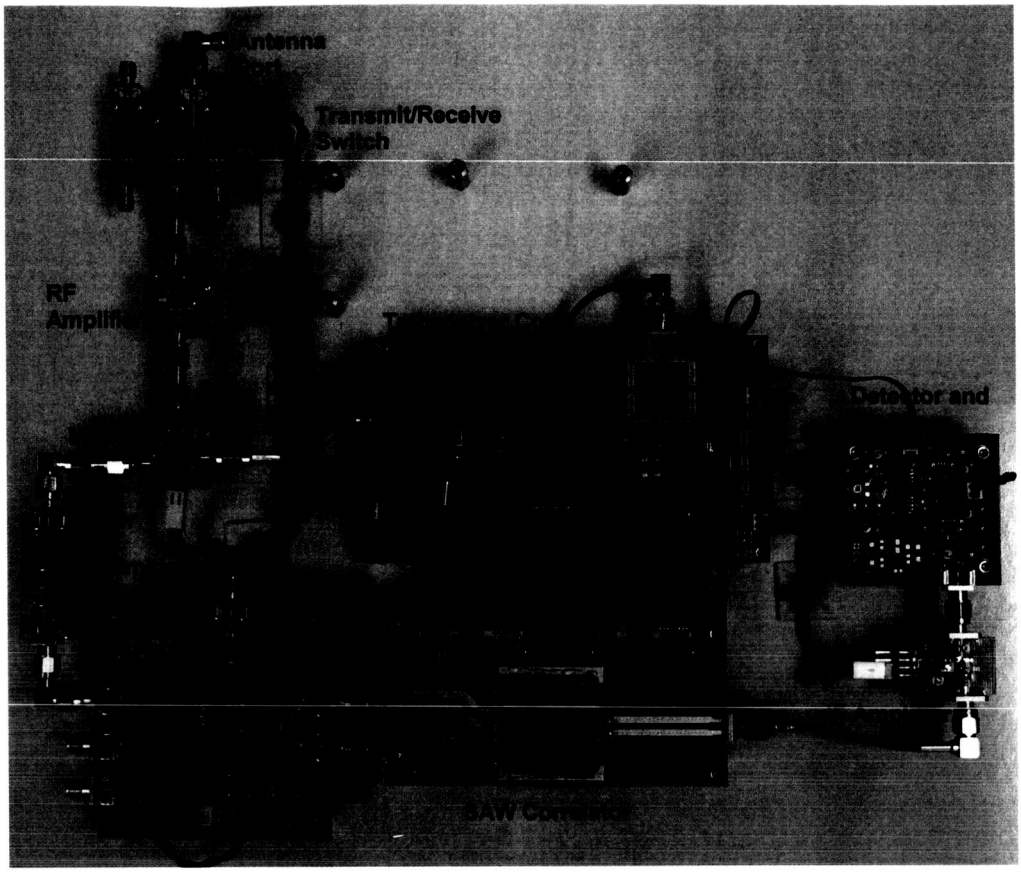

Figure 48 – 183 MHz IF SAW Receiver

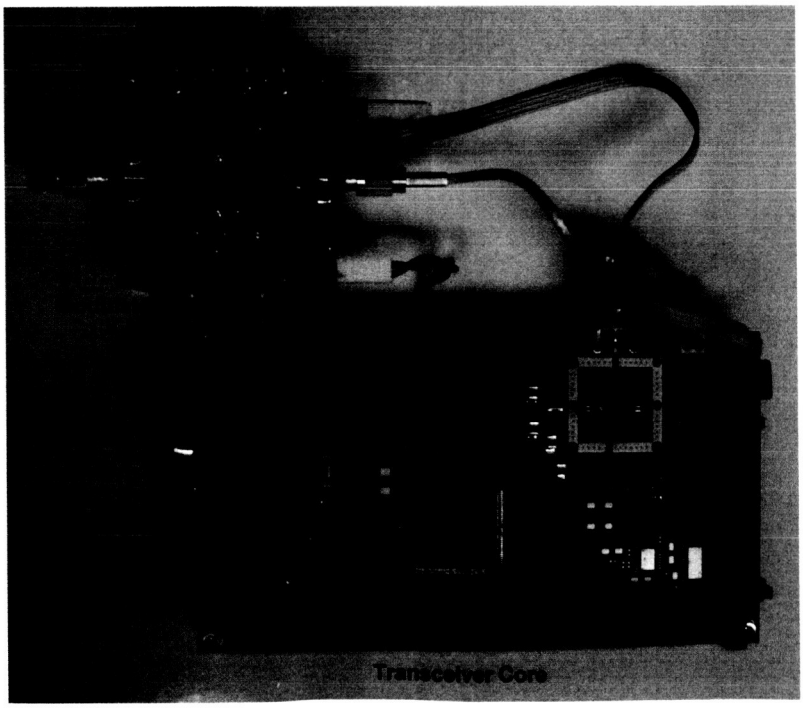

Figure 49 – 183 MHz IF SAW Transmitter

The system is capable of transmitting or receiving packets containing data samples acquired from the sensor interface. These packets transfer data at rates of up to 32 samples per second and include a Cyclic Redundancy Check (CRC) code to detect any errors in the received data. An example packet structure is shown in Figure 50. This example uses a 31 bit preamble to allow time for the receiver to stabilize and the baseband processor to begin data detection. Eight bit fields for source and destination ID's uniquely identify the transceiver unit that the packet originated from and the unit that the packet is intended to be received by. The type field is used to identify different types of payload data. An eight bit length field declares the length of the payload field in bytes. This allows for a variable payload length of up to 255 bytes. The 16 bit CRC field at the end of the packet can detect bit errors that occur within the entire packet length.

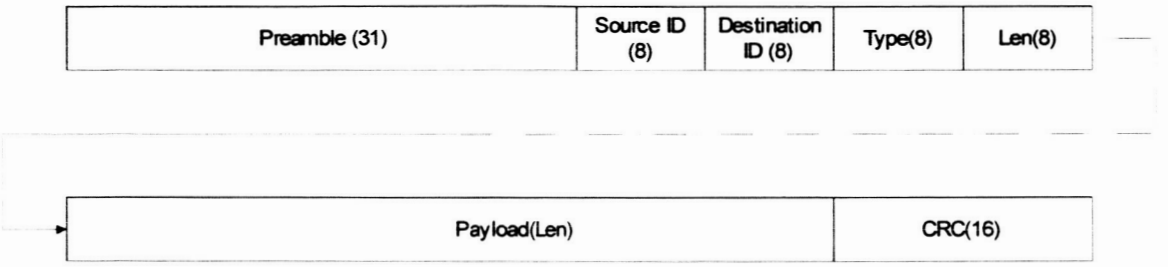

Figure 50 – Packet Structure (bits)

Functional tests performed with on the PSAW system included transmission and reception of data packets formatted as described above. The successful wired and wireless reception of data packets was demonstrated using the 183 MHz PSAW devices. The following section includes some quantitative results of these tests.

5.2.9.4 Receiver Sensitivity and Dynamic Range

Receiver sensitivity and dynamic range were measured using a 183 MHz PSAW in the receiver. The PSAW was programmed with the 183 MHz FSAW code of [11111001001100001011010100011110]. Figure 51 demonstrates receiver performance by displaying the packet error rate vs. signal power measured at the receiver input port. This chart shows that the receiver performs well at signal levels as low as -95 dBm and has a dynamic range of greater than 70 dB.

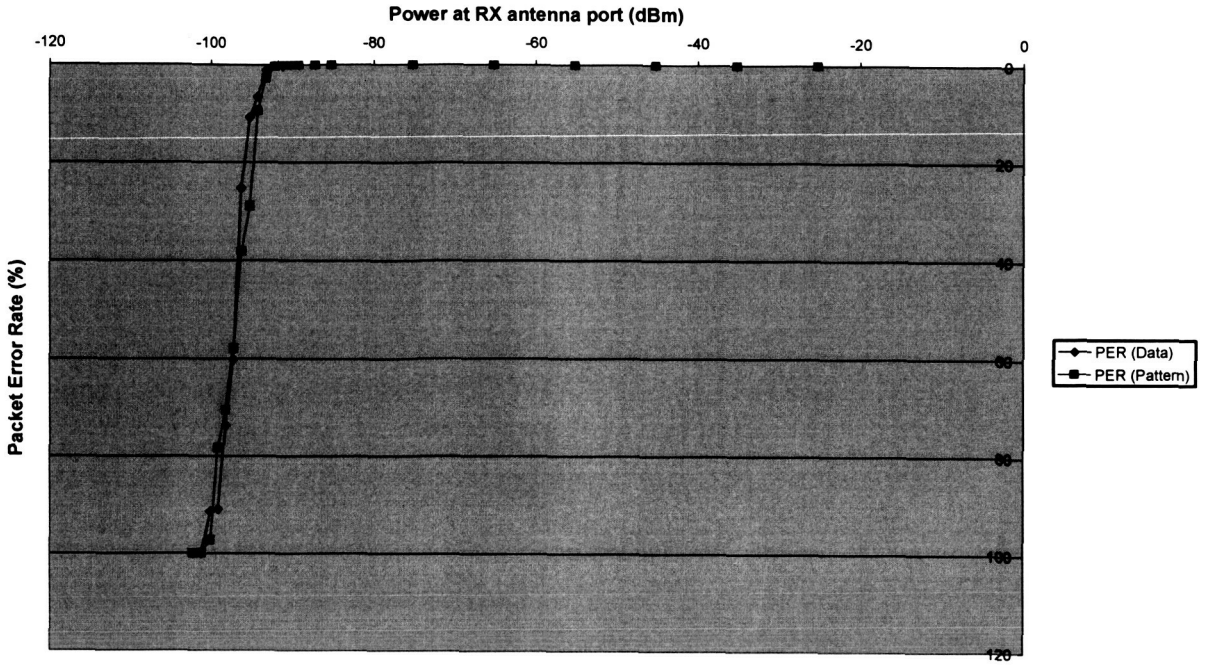

Figure 51 – 183MHz IF PSAW Receiver Performance

6. Conclusions

This report describes a progression of development efforts to produce a Programmable Surface Acoustic Wave (PSAW) device based Direct Sequence Spread Spectrum (DSSS) transceiver. The Phase 2 efforts produced a SAW based receiver and transmitter that operate in the 2.4GHz band with a single fixed code and no programmability. The first attempt at a Phase 3 design was unsuccessful in producing an operable PSAW device. A secondary design successfully demonstrated the usage of a PSAW device operating at 183MHz. The center frequency of the generated signal is then translated to higher frequencies for wireless transmission and reception. A transceiver system was designed around this PSAW device to transmit and receive in the 900-928MHz ISM frequency band. The system has excellent flexibility in programming spreading codes and shows very good sensitivity and dynamic range in receive mode. Improvements to the design of the PSAW itself to achieve higher peak to off peak (POP) ratios could further improve this performance.

This program has successfully demonstrated the feasibility of using PSAW devices to demodulate DSSS signals. A robust and configurable communication network could be constructed with the current transceiver system; however, the design must be scaled down in size and power usage to make it competitive with commercially available transceivers of similar capabilities.

REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	3-SEP-04	Final Report, 07/02/01 – 09/03/04

4. TITLE AND SUBTITLE
PSAW/MicroSWIS [Micro-miniature Surface Acoustic Wave (SAW)-based Wirelesss Instrumentation System] Program

5. FUNDING NUMBERS
NAS3-01118

6. AUTHOR(S)
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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Invocon, Inc.
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8. PERFORMING ORGANIZATION REPORT NUMBER
IVC1420026

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
NASA Glenn Research Center
Gary Hunter/M.S. 77-1
21000 Brookpark Road
Cleveland, OH 44135

10. SPONSORING / MONITORING AGENCY REPORT NUMBER
N/A

11. SUPPLEMENTARY NOTES

12 a. DISTRIBUTION / AVAILABILITY STATEMENT

12 b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

This Final Report for the PSAW program documents the experiments carried out, work performed, testing results and conclusions.

14. SUBJECT TERMS
Fixed and Programmable Surface Acoustic Wave
RF Transmitter, RF Receiver
Data Acquisition

15. NUMBER OF PAGES
58

16. PRICE CODE

17. SECURITY CLASSIFICATION OR REPORT	18. SECURITY CLASSIFICATION ON THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL