High Mobility SiGe/Si n-MODFET Structures and Devices on Sapphire Substrates

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ABSTRACT

SiGe/Si n-type modulation doped field effect structures and transistors (n-MODFETs) have been fabricated on r-plane sapphire substrates. Mobilities as high as 1380 cm^2/Vs were measured at room temperature. Excellent carrier confinement was shown by Shubnikov-de Haas measurements. Atomic force microscopy indicated smooth surfaces, with rms roughness less than 4 nm, similar to the quality of SiGe/Si n-MODFET structures made on Si substrates. Transistors with 2 µm gate lengths and 200 µm gate widths were fabricated and tested. An I_{DS} of 9 mA was obtained by operating the transistor in an enhancement mode (positive V_{GS}) and the maximum transconductance (g_m) was 37 mS/mm at a V_{DS} of 2.5 V. The transducer gain (G_t) measured with a load-pull system was 6.4 dB at 1 GHz for a V_{DS} of 2.5 V and V_{GS}=-0.4 V.

INTRODUCTION

System-on-a-chip (SOC) processes are under intense development for high-speed, high frequency transceiver circuitry. As frequencies, data rates, and circuit complexity increase, the need for substrates that simultaneously enable high-speed analog operation, low-power digital circuitry, and excellent isolation between devices becomes increasingly critical. SiGe/Si modulation doped field effect transistors (MODFETs) with high carrier mobilities are currently under development to meet the active RF device needs. However, since the substrate normally used is Si, the low-to-modest substrate resistivity causes large losses in the passive elements required for complete high frequency circuits [1, 2]. These losses become increasingly troublesome as device frequencies progress to the Ku-band (12 – 18 GHz) and beyond [3]. Relative to Si, the high electrical resistivity of sapphire enables superior performance passive devices, such as inductors [1, 2], and less crosstalk between devices. The use of silicon-on-sapphire circuits for low-power, radiation-hard applications is well known [4]. Thus, sapphire is an excellent substrate for high frequency SOC designs because it supports both active and passive RF devices, as well as low-power digital operations [5].

Both p- and n-type SiGe/Si MODFET devices on sapphire substrates have been reported. Koester et al. [6] reported a 0.1 µm by 50 µm gate, p-MODFET with transit (f_T) and cutoff (f_{max}) frequencies of 50 and 116 GHz, respectively. While p-MODFET structures require a SiGe channel in compressive strain [7], n-MODFET structures require a conducting Si channel in tensile strain. However, the initial Si layer on sapphire is in compressive strain [8]. Thus, it is harder to grow n-MODFET structures, as the

buffer must compensate for the original Si compressive strain and provide the required tensile strain for the channel. Recently, our group reported n-MODFET structures [9, 10], but the initial DC transistor performance for 5 μm gate lengths was extremely poor. The goal of this paper is to expand on earlier n-MODFET materials and device work by showing good transistor performance for a 2 μm gate device and make an estimate of the potential of our material for high frequency (above K_u-band) applications, provided sub-micron lithography is used.

n-MODFET FABRICATION

SiGe/Si n-MODFET structures are deposited via molecular beam epitaxy (MBE) onto modified Si-on-sapphire (r-plane) substrates. The as-received films are 270 nm thick and are subjected to a series of processing steps to improve the crystalline quality and reduce the Si thickness. First, Si ions are implanted into the Si films at a dose of $2x10^{15}$ cm^{-2} and a beam energy of 180 keV. The samples are subsequently annealed for three hours at 1100 °C in flowing N_2, followed by an eight hour O_2 anneal, also at 1100 °C. The oxide is chemically etched to achieve a 100 nm thick Si layer. The SiGe buffer layer, virtual substrate, and n-MODFET structures are deposited using MBE. A schematic drawing of the various layers is shown in Figure 1. The 600 nm thick $Si_{0.7}Ge_{0.3}$ virtual substrate is grown at 755 °C, while the 10 nm thick Si channel and 5 nm thick top SiGe spacer layers are grown at 500 °C. Antimony (Sb) is incorporated into the donor layer via a delta-doping approach using an Sb_4 source, immediately following growth of the top $Si_{0.7}Ge_{0.3}$ spacer layer. The delta-doped Sb layer deposition is also performed at 500 °C. Next, the substrate temperature is decreased to 200 °C for seven seconds, and a thin (~ 1 nm) $Si_{0.7}Ge_{0.3}$ layer is deposited to minimize Sb segregation. The substrate temperature is increased to 500 °C and the remaining 9 nm of the donor layer and 5 nm Si cap layer is deposited. All data reported here is measured on the sample with a total Sb doping of $4x10^{12}$ cm^{-2}.

Device processing started with wet chemical etching of the mesa, P ion implantation and Pt/Ti/Au deposition and rapid thermal annealing for the source and drain ohmic contacts, and finally deposition of Pt/Au (30nm/1500nm) for the Schottky gates. The gate length is 2 μm, the source-to-drain distance is 6 μm, and the gate width is $2x100$ μm^2. The transistors use a double-gate π design, wherein gate regions are located on both sides of the drain terminal, and source regions are located adjacent to the gate, on the sides opposite the drain. The mask also contained a transfer length method (TLM) structure with five $100x100$ μm^2 pads and distances in the range 3-200 μm.

RESULTS AND DISCUSSION

The goal of this work is to optimize transistor performance of SiGe/Si n-MODFET devices on sapphire substrates. Because the device behavior is intimately related to the electron mobility of the n-MODFET structures, and little is known about the mobility behavior of these structures, materials characterization as well as device performance data is presented.

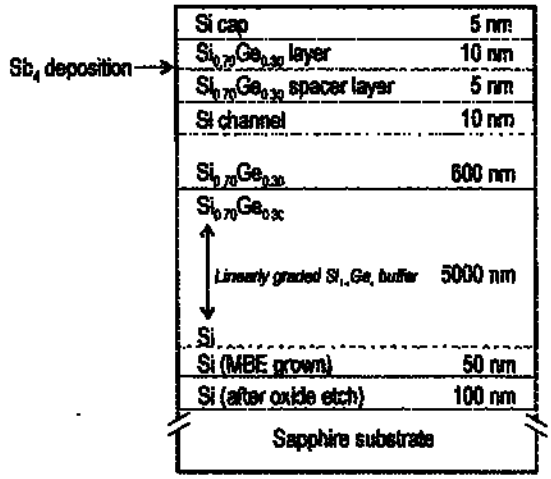

Fig. 1. Schematic diagram of buffer layer, virtual substrate, and n-modulation doped field effect transistor (n-MODFET) structure on r-plane sapphire substrate

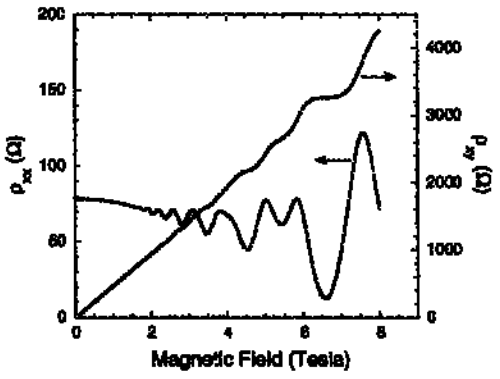

Fig. 2. Longitudinal (ρ_{xx}) and Hall (ρ_{xy}) resistivity versus magnetic field (T). Data taken at 0.25 K.

Electron Mobility in n-MODFET Structures

Electron mobility is measured at room temperature and 0.25 K, using Van der Pauw configurations. Our best sample has a room temperature mobility of 1380 cm^2/Vs and a sheet carrier concentration of $1.8x10^{12}$ cm^{-2}, i.e. a sheet resistance ρ_s of ~2,500 Ω/□. One sample was characterized at both room temperature and at 0.25K. The electron mobilities and associated carrier concentrations are 1,270 cm^2/Vs and $1.6x10^{12}$ cm^{-2} (ρ_s ~3,000 Ω/□) at room temperature, while at 0.25K they are 13,300 cm^2/Vs and $1.33x10^{12}$ cm^{-2} (ρ_s~350 Ω/□). The modest drop in carrier concentration indicates that the Sb_4 delta-doping process provides excellent carrier confinement, pointing to a good probability that the conductivity takes place via a two-dimensional electron gas (2DEG), wherein electrons are physically separated from the donor atoms in the SiGe layer above the tensile-strained Si channel. This conclusion is fully confirmed by the Shubnikov-de Haas (SdH) oscillations at 0.25 K (Figure 2), as the 2DEG carrier concentration obtained from the ρ_{xx} oscillations is equal to the Hall effect result at 0.25K.

Surface Roughness in n-MODFET Structures

Since the channel is only 20 nm below the surface, atomic force microscope (AFM) imaging is an effective means of gauging the interface roughness. Low magnification AFM measurements (Figure 3) show that the surfaces of these structures are reasonably smooth, with an rms surface roughness values of 3 – 4 nm, which is comparable to the data observed in SiGe/Si n-MODFET structures grown on Si substrates [11]. High magnification AFM (figure 4) indicates the surface is uniform, with random undulations

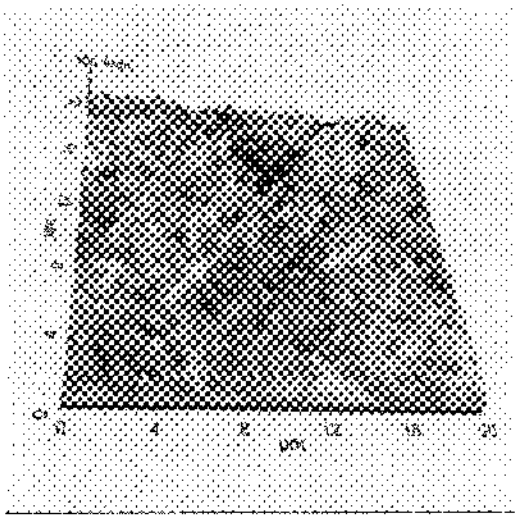

Figure 3. Large area (20x 20 μm^2) Atomic Force Microscopy (AFM) image of SiGe/Si n-MODFET structure on r-plane sapphire. The rms surface roughness is 3.9 nm.

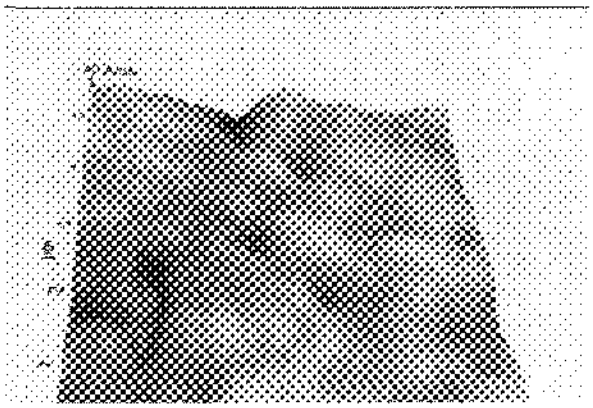

Figure 4. Small area (5x5 μm^2) Atomic Force Microscopy (AFM) image of SiGe/Si n-MODFET structure on r-plane sapphire.

across the surface. There is less than 0.5 nm difference between the rms surface roughness measured at low and high magnifications. Since 4 nm roughness is a common result in SiGe/Si [11] and very large low temperature mobilities are observed in such structures [12, 13], we believe that the roughness scattering mechanism is not a limiting factor in the current SiGe/Si/sapphire structures.

DC and RF Transistor Results

Several transfer length method (TLM) structures around the transistor structures are measured, and the specific contact resistivity (ρ_c) and the semiconductor sheet resistance (ρ_s) are obtained [14]. In all cases, the experimental ρ_s values are inside the range 2700-2900 $\Omega/\square$, which is well within our Hall effect limits. The value of ρ_c has more scatter than ρ_s, with an average result of $\rho_c = (3\pm1)\times10^{-5}\ \Omega cm^2$ (2.9 Ω-mm). The transistors current-voltage (I-V) characteristics were measured on a Tektronix 370A curve tracer and connections to the transistors are made through 150 μm pitch Ground/Signal/Ground microwave probes. The I-V characteristics are shown in Figures 5 and 6. An I_{DS} of 9 mA (45 mA/mm) is obtained by operating the transistor in an enhancement mode (positive V_{GS}) and the maximum transconductance (g_m) is 37 mS/mm at a V_{DS} of 2.5 V. The transconductance is almost flat in the gate voltage V_{GS} range -0.1 to +0.3 V. The measured (extrinsic) transconductance is corrected [15] to obtain the intrinsic transconductance $g_{m,int}$ using the results of the TLM measurements. The main contributor to the correction is the source resistance (R_s), which includes the semiconductor resistance of the source-gate area (R_{SD} =28Ω) and the source contact resistance

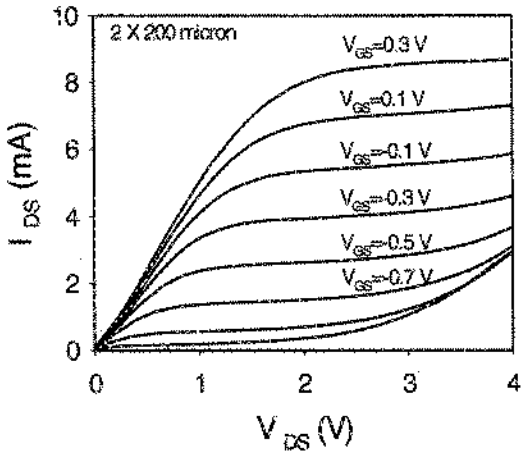

Figure 5. Measured I-V characteristics of a 2 x 200 μm n-MODFET.

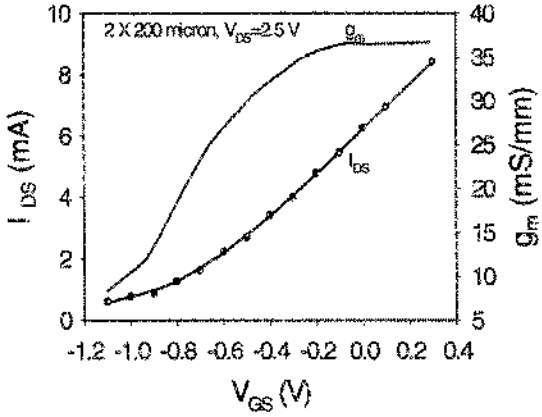

Figure 6. Measured transconductance of a 2 x 200 μm^2 n-MODFET.

(R_c=14Ω). The correction due to the output conductance is negligible. For our 2 μm transistor we obtain $g_{m,int}$=55 mS/mm.

The maximum transducer gain (G_t) as measured on a load-pull system is 4.4 dB at 800 MHz and 6.4 dB at 1 GHz for a V_{DS} of 2.5 V and V_{GS}=-0.4 V. These values are substantially higher than the transistor gain, $|S_{21}|^2$, because of the gain achieved by providing a simultaneous conjugate match at the input and output of the transistor during the load-pull measurement.

An estimate of the capability of our material to yield high quality microwave transistors using electron-beam or VUV lithography is performed assuming a conservative value for the saturated velocity (v_{sat}) of $1.0x10^7$ cm/s, a gate length of 0.1 μm and a 0.5 μm source to drain spacing, which are similar to values common in the literature [16]. The maximum intrinsic current gain cutoff frequency f_T as determined by the saturated velocity approximation ($f_T=v_{sat}/2\pi L_g$, where L_g=0.1 μm), is f_T~160 GHz. However, in practice, much lower f_T values are reported [11, 16], even for shorter gates. The main, but not the only reason for much lower experimental f_T, is the source resistance R_s. Using our TLM results and taking into account only the contribution from R_s for our material (ρ_s=2,800 Ω/□, $\rho_c=3x10^{-5}$ Ωcm^2) on g_m, we obtain a maximum extrinsic transconductance of g_m~150 mS/mm and f_T~55 GHz. This calculation assumes 25 nm between the Schottky gate and the center of the wave function in the channel and an average dielectric constant of 12.5. In this case, the relatively high contact resistivity decreases the performance, as R_{SD} is now smaller than the contact resistance. The best device that can be made from our material will have a much smaller ρ_c. For a reasonable ρ_c value of $3x10^{-6}$Ωcm^2, we obtain the estimates g_m~240 mS/mm and f_T~90 GHz.

CONCLUSIONS

The DC and RF performance of 2 x 200 μm^2 SiGe/Si n-MODFET transistors on r-plane sapphire is demonstrated. Atomic force microscopy shows smooth surfaces, with

rms roughness less than 4 nm, indicating a quality similar to SiGe/Si n-MODFET structures on Si substrates. An I_{DS} of 9 mA (45 mA/mm) is obtained by operating the transistor in an enhancement mode (positive V_{GS}), and the maximum measured extrinsic and intrinsic transconductance (g_m) are 37 mS/mm and 55 mS/mm respectively at a V_{DS} of 2.5 V. The transducer gain (G_t) is 6.4 dB at 1 GHz for a V_{DS} of 2.5 V and V_{GS}=-0.4 V, as measured by a load-pull system. The data suggests that in order for these structures to achieve their full potential at high frequencies, e-beam or VUV lithography should be used, which will result in a transistor with a g_m up to 240 mS/mm and an f_T up to 90 GHz for a 0.1 μm gate device.

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