THE ROSSI X-RAY TIMING EXPLORER (XTE) SOLAR ARRAY ANOMALY

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ABSTRACT

The XTE was launched December 30, 1995. Shortly after launch, it became apparent that the solar array was not performing as expected. On leaving shadow, the array exhibited many discontinuous drops in current output. The size of each of these drops was consistent with the loss of a part of a cell. The current decreases could not be caused by the loss of an entire cell or an entire circuit. This meant that the array may have had numerous cracked solar cells that opened as the array got warmer. Studies performed on the array's qualification panel suggest that the cell cracks may have been caused by extensive tap testing performed on the array and that these cracks were undetectable at room temperature using usual inspection methods.

CONFIGURATION

The XTE's solar array is such that it is always oriented to the sun except when the spacecraft is slewing from one "target" to another. Figure 1 shows that the XTE solar array is divided into eight circuits. Six of these circuits are each contained completely on a single solar panel. The other two, circuits four and eight, are each divided on three panels. Each circuit is further subdivided into nine strings of silicon solar cells. Six of these strings have 100 cells in series and three have 103 cells in series. The strings comprising each circuit are paralleled at the most positive and negative cell. Each cell's size is 3.92 centimeters by 5.70 centimeters. The cells are fixed to aluminum face sheet substrates with CV 2568. The circuits are wired into the spacecraft as depicted in Figure 2; and, their voltages and currents are monitored as shown.

Figure 2 shows that each of the eight circuits feeds into the spacecraft independently. As the battery charges during the sunlit portion of the orbit, the spacecraft needs less current. This current control is accomplished by partially and then sequentially completely shorting out one circuit after another, with circuit eight shorting first. For example, soon after coming into sunlight circuit eight is shorted, circuit seven is partially shorted, and the remaining circuits are fully on line. Sometime thereafter circuits eight, and seven are shorted, circuit six is partially shorted and the other circuits are fully on line; etc.

ARRAY PERFORMANCE

Figures 3 and 4 respectively show the voltage across and the current produced by circuits five and four during the sunlit portion of orbit five. The performance of circuit five is normal in all respects. The voltage rises rapidly across the circuit when it comes into sunlight. It then reaches the battery voltage and is clamped to battery voltage through the diode. The voltage rise continues at a slower rate as the battery is charged. The rise in voltage stops when the battery hits its voltage limit. The voltage then holds steady for about seven minutes. Subsequently, it decreases suddenly. This is due to the power system shorting out the circuit which is no longer needed to maintain the battery at constant voltage. The circuit voltage stays at about 0.6 volt until

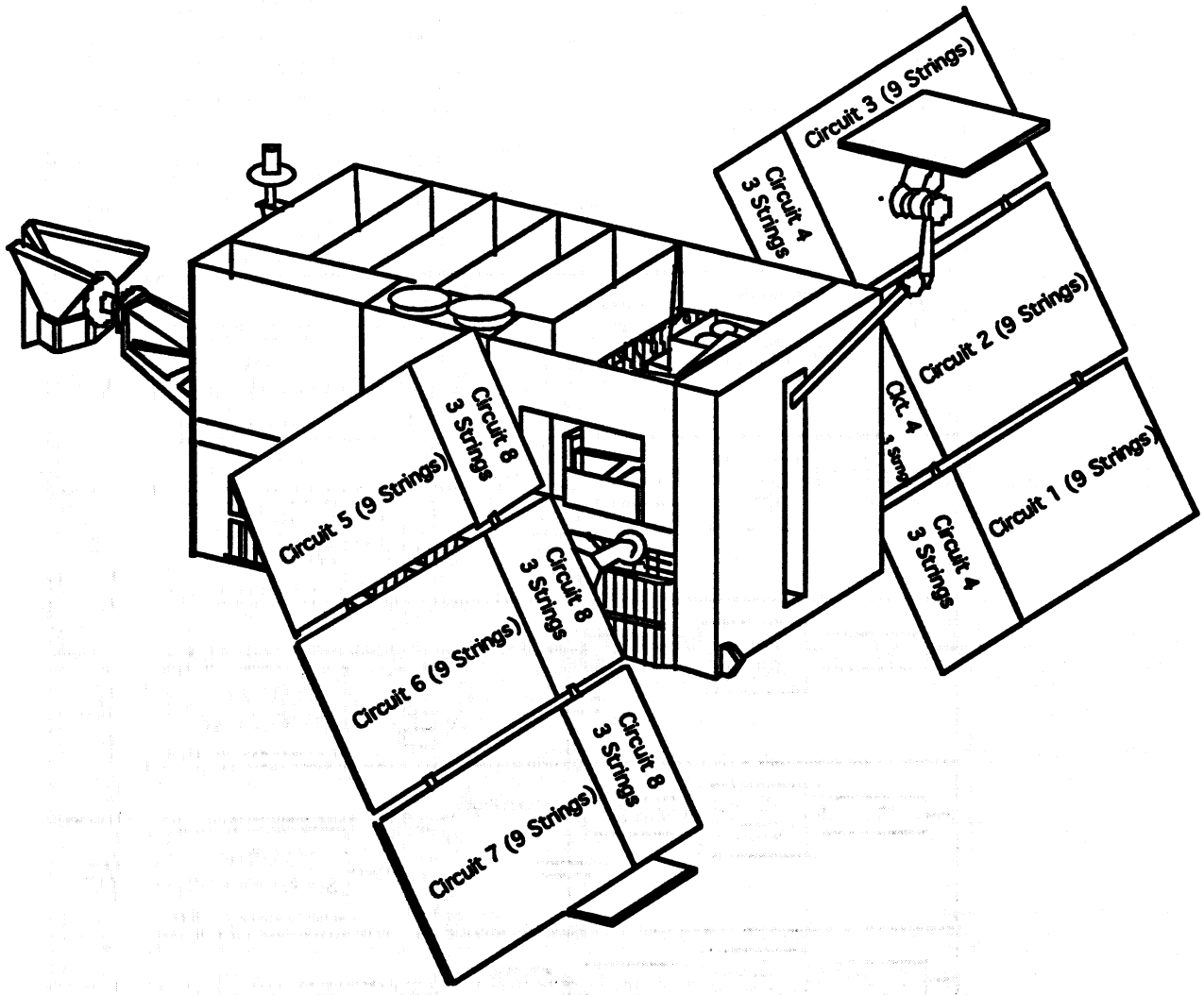

Figure 1
The XTE Spacecraft and Solar Panels

the spacecraft begins to enter darkness. At this point, there is insufficient power to maintain battery voltage, and the power system electronics takes the short off circuit five and its voltage again rises.

The current from circuit five rises rapidly as the circuit comes into sunlight. It then rises more slowly. This second rise is due to two effects. First the array is approaching and then going over the terminator about ten minutes into the orbit. This event corresponds to an increase in the array current due to earth albedo. Second, the array produces more current because its temperature is rising. The current then drops and rises again as the spacecraft crosses the terminator again at about 55 minutes. The shorting of the circuit to about 0.6 volts at about 17 minutes shows little effect on the current. This is because the operating voltage of the circuit is well to the short circuit side of the current versus voltage curve knee. There is nonetheless an effect. It cannot be seen in Figure 3, but a barely perceptible increase in current occurs every time the circuit is shorted. We will contrast the increase to the increase in the malfunctioning circuit four later.

Circuit four performance, shown in Figure 5, is abnormal. For the first nine minutes or so in the sunlit portion of the orbit, the circuit is performing as expected. Then the current from the circuit drops discontinuously. It then recuperates and then drops suddenly again and then again. This occurs while the voltage on the circuit steady. The only explanation is that the circuit current versus voltage characteristic is

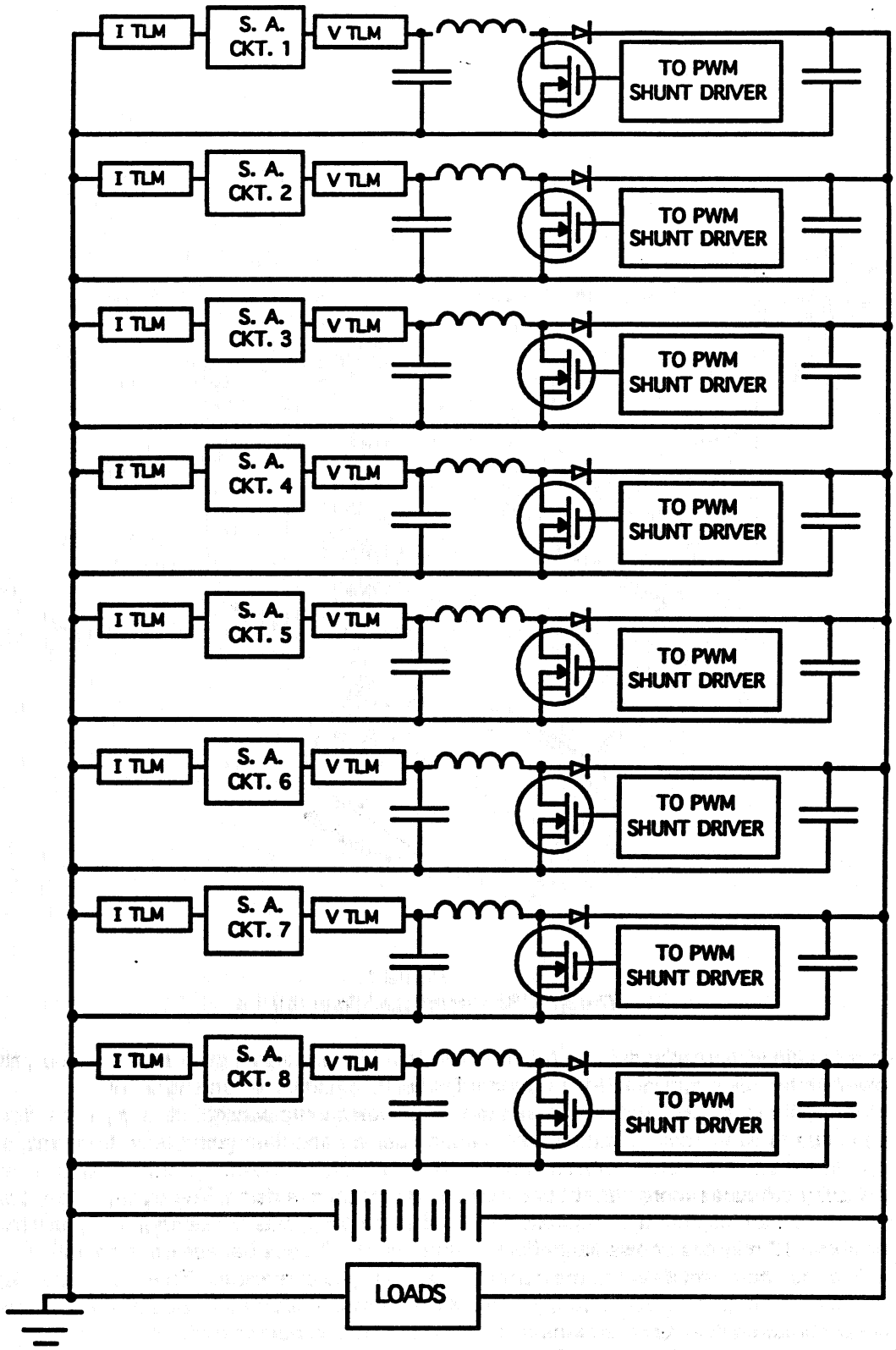

Figure 2
Simplified Schematic of the XTE Power System

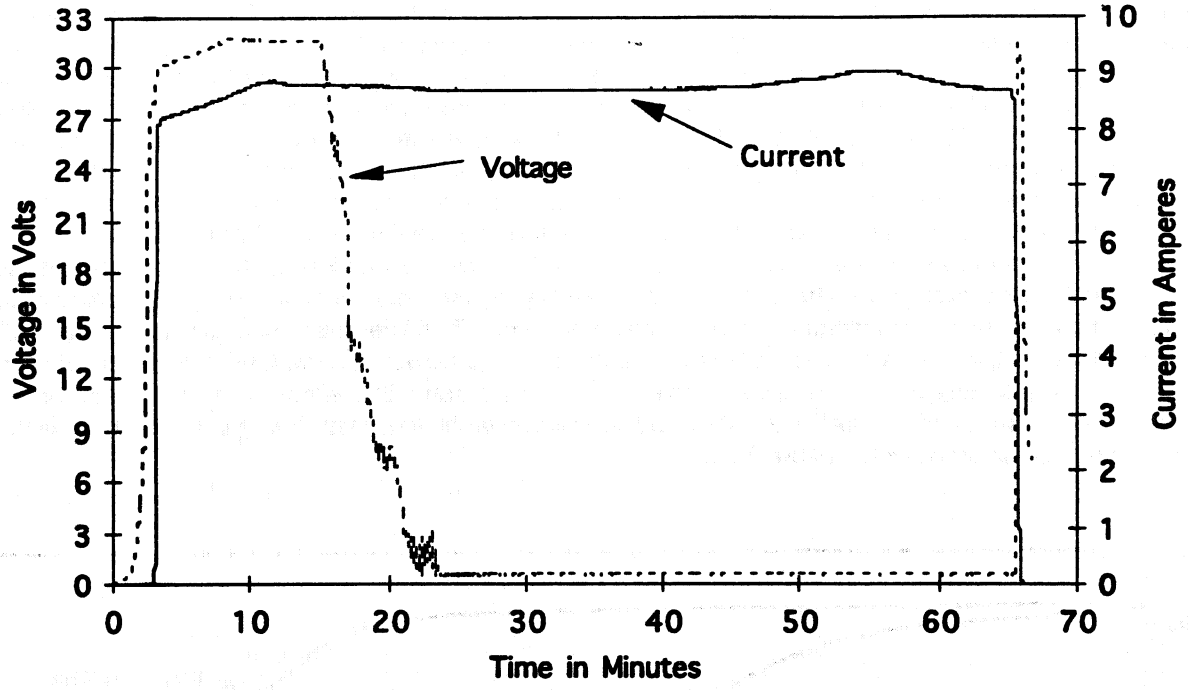

Figure 3
Module Five Voltage and Current Versus Time for Orbit Five

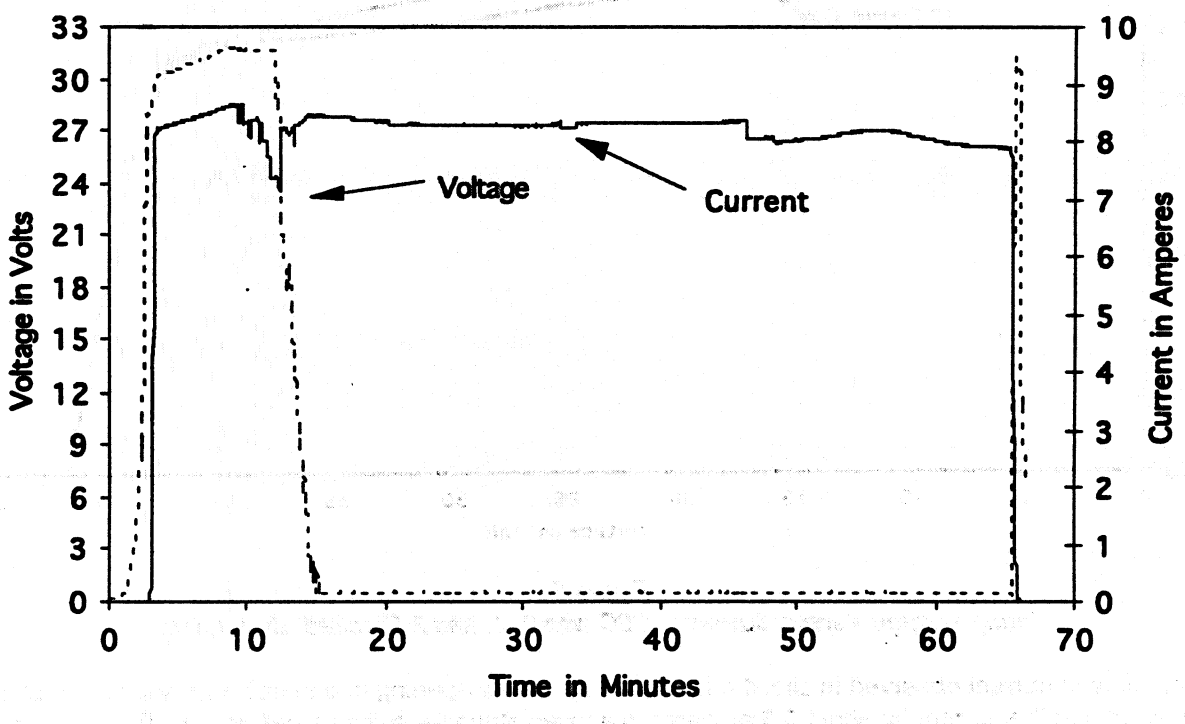

Figure 4
Module Four Voltage and Current Versus Time for Orbit Five

changing anomalously and discontinuously. The current decreases discontinuously until about thirteen minutes after coming into sunlight when the circuit is shorted out by the spacecraft electronics. At this point the current rises quite suddenly. Normally, the current is expected to rise very slightly with decreasing voltage, as with circuit five, but not nearly as much as it does with circuit four. Seven of the eight circuits showed anomalies similar to those in circuit four. Circuits 1 through 8 showed maximum orbital degradations of approximately 5%, 14%, 18%, 22%, 0%, 20%, 4%, and 15%. The total average loss was much smaller.

Circuit four performance, and the performance of the other malfunctioning circuits, is explained by Figure 5 which shows the I-V curve of one of the circuit's strings with none, one and two cracked solar cells. Each cell is cracked such that the maximum amount of cell that can be lost is lost. The Figure was generated by measuring the reverse bias performance of the XTE solar cells, extrapolating what their current versus voltage characteristics would be with a "maximum" cell crack, and then simulating string performance. A complex example of such a "maximum" crack is shown in Figure 7. If the crack were any further to the "left" both pieces of the cell would be connected into the circuit by the parallel redundant interconnects and the cell would function as if it were in a single piece. Such a crack would have little effect on the overall output. If the crack were any further to the "right", the cell would lose somewhat less than the approximate 1/3 it looses with the worst case crack depicted in the Figure.

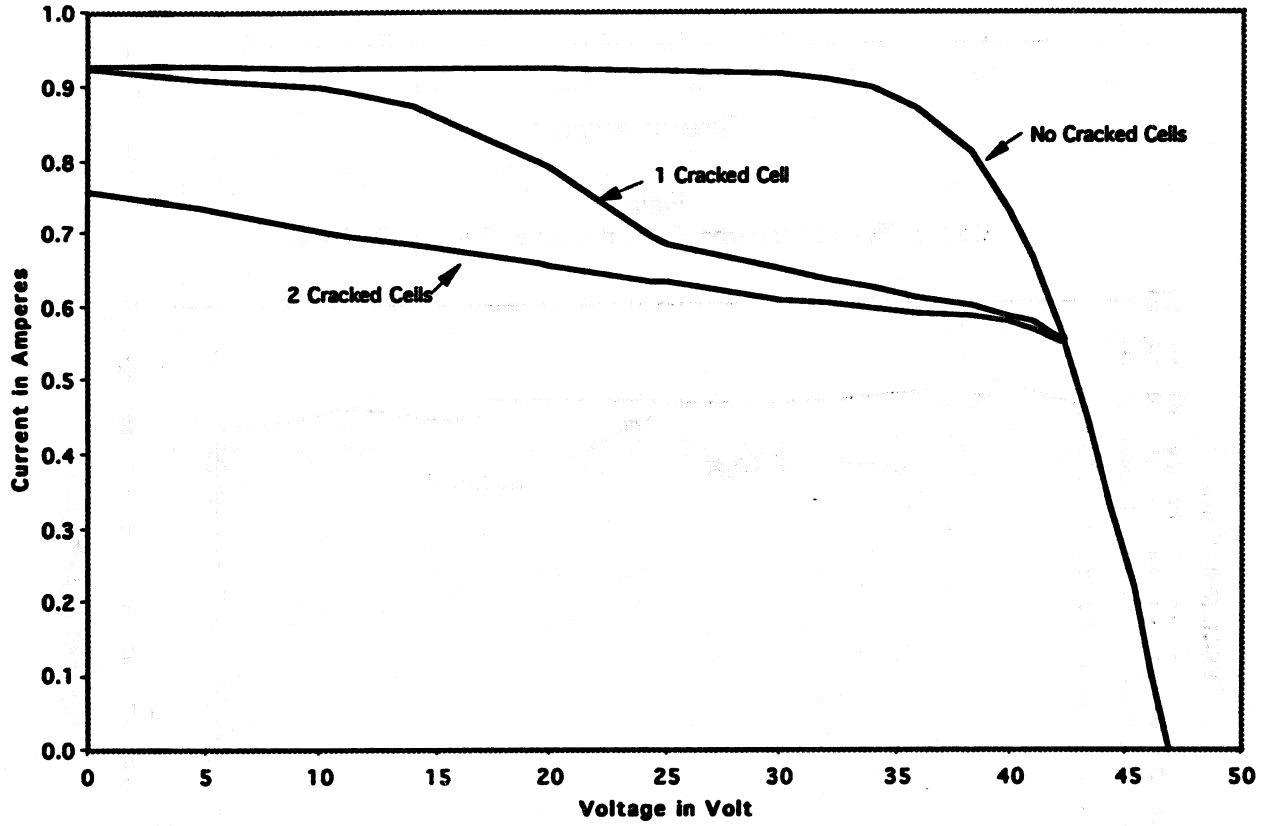

Figure 5
String Voltage Versus Current at 70C with 0, 1, and 2 Cracked Solar Cells

The decrease in current observed in circuit 4 is caused by cracks opening in one cell after another in different strings, dropping the current by about 0.3 amperes in a given string each time a cell opens. Furthermore, the effect of the cracks is not observed at short circuit current if only one cracked cell is present in a single string; but is present with two or more cracks in a string. This explains the current recovery in circuit four after it is shorted. Apparently, some of the strings have just one crack. It also explains how the current recovery is not

complete. If any of the strings in circuit four have more than two cracked solar cells, the current will not recover.

The possibility that there are completely open strings in the circuits was explored. This is easy to eliminate as it would cause current decreases on the order of 0.9 amperes. Current decreases that large are not seen in any of the circuits.

TEST OF THE XTE QUALIFICATION PANEL

Because of the array's unexpected performance in space, the XTE qualification panel was used to help determine the cause. Prior to array delivery, the qualification panel underwent extensive testing including exposure to thermal vacuum cycles, thermal cycles at ambient pressure and an acoustic environment. The panel showed no anomalous behavior due to these exposures. However, all the evaluations of the panel were performed at room temperature. When the panel was flash tested at elevated temperatures, subsequent to the XTE's launch, the panel showed an anomalous I-V curve, see Figure 6. At elevated temperature, a crack was clearly seen that could lead to the anomalous performance, see Figure 7.

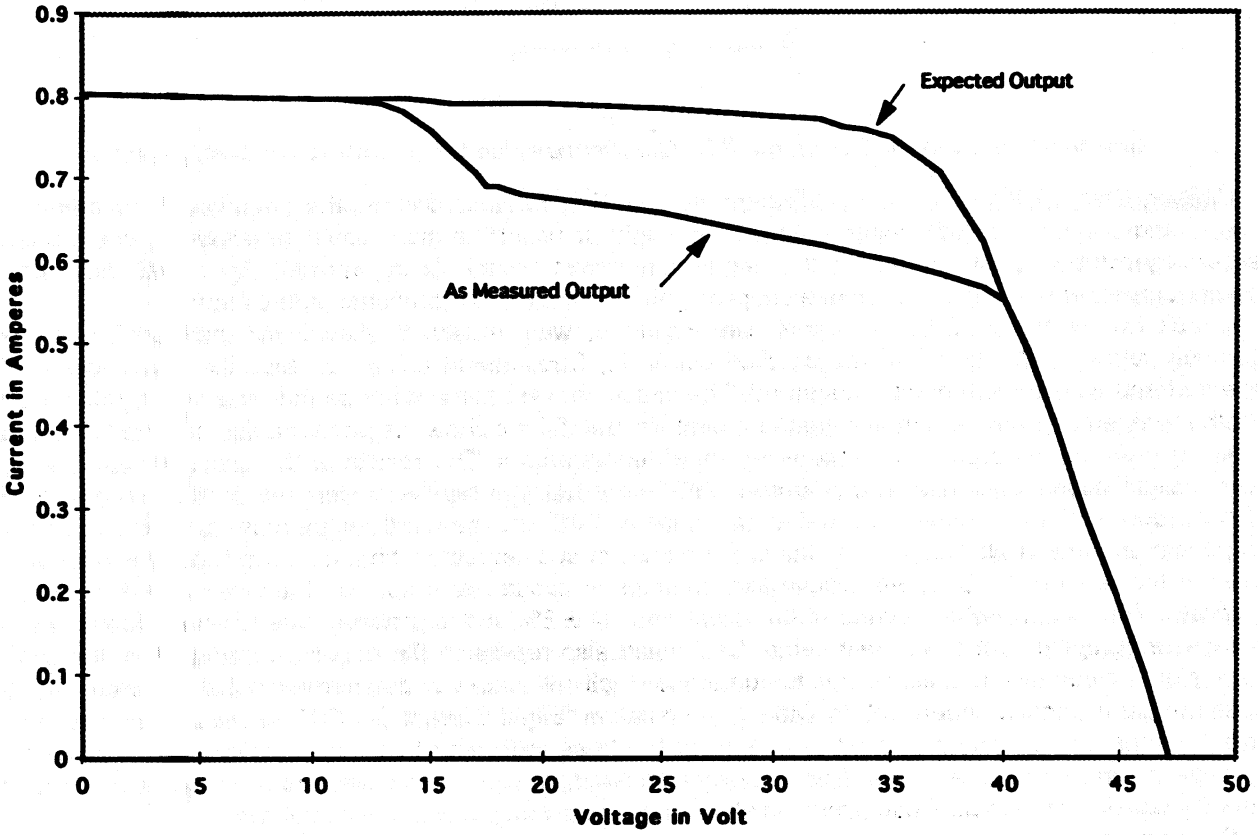

Figure 6
XTE Qualification Panel Circuit One I-V Curve at 70C

However, the crack in the solar cell was such that only one of its four branches could be seen at room temperature with the usual methods the cell manufacturer, Spectrolab, and GSFC use to inspect for cracks. This suggested the possibility that the XTE array was launched with cracked cells that could not be seen. The plausibility of this was increased because the flight panels were extensively and repeatedly tapped tested to check for delaminated substrates. Further inspections were carried out on the qualification panel to determine the conditions under which the crack could be seen, and also, to further determine if tap testing, bending, or

heating could cause cell cracks that were not visible at room temperature. These last two items were performed because the flight panels were bend tested and were subjected to high temperatures in bake out.

The panel was reinspected at Goddard using two methods: infrared light and a stereo microscope with normal light. The cracks in the solar cell were not detected using infrared equipment despite several approaches that were tried. Using a stereo microscope, the GSFC located the "vertical" part of the crack at 7X. This vertical crack actually consists of a small series of 45 degree zigzags that on the whole proceed vertically, not unexpected for a silicon solar cell crack as the zigzags follow the crystalline "planes" in the silicon. The other cracks were not visible using this method until the cell was heated to "45 to 50C" with a heat gun at which temperature they were plainly visible.

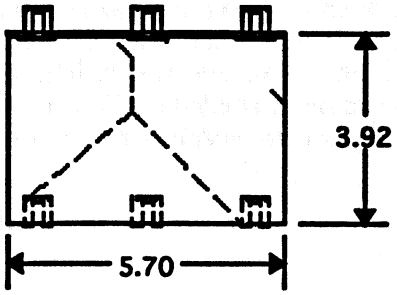

Figure 7
Sketch of the Cracked Cell on the XTE Qualification Panel, Dimensions in Centimeters

Subsequently, GSFC sent the qualification panel to Spectrolab and to another organization to determine if they could see the "cracks" under either infrared light or using the more usual stereoscopic examination. Neither organization picked up the crack using the stereomicroscope. Using infrared, Spectrolab did identify, at room temperature, an anomaly whose shape slightly resembled two branches of the crack.

Circuit two of the qualification panel, see Figure 8, was inspected, electrically measured, and then vigorously tapped. (Circuit 1 had the cracked cell in it.) Subsequent to the tap test, the panel was again inspected and its electrical output measured. The circuit showed some damage that was visually detectable at both room temperature and at elevated temperature, but did not show the phenomenon of a crack that was hidden at room temperature but visible at elevated temperatures. The results of the electrical test, Table I, show a slight power decrease at 28C and at 70C. Note that the results designated as 28C were actually taken at room ambient temperature and extrapolated to 28C, the standard temperature at which solar cells and panels are evaluated. Because of one of the results of subsequent testing, a fairly substantial increase in power at the last test at 28C, we believe that changes in circuit two output on the order of ± 5 % are not significant. This is somewhat outside of the usual error of ± 2% and is probably due to an unknown error in the measuring equipment or our test setup. Or it could also represent the actual performance of the circuit which might be somewhat unstable due to numerous small cell cracks or deteriorated solder after the thermal cycles the panel circuits underwent. In Table I, the notation "Slight Current Cut Off" means that the circuit two current versus voltage curve is a bit too sharp at the knee indicating that one or more cells is producing slightly less current than the others. This is a very mild example of the anomalous curve in Figure 5; but is not generally considered a fault. It can occur simply because a low output cell is in circuit two.

Subsequently, circuit two was tapped using a harder tap than previously. It is not conceivable that the Spectrolab technicians would have tapped the flight panels with such force. Numerous cover cracks and several cell cracks were noted both at room temperature and at elevated temperatures, but there was no evidence of cracks that were "hidden" at room temperature but otherwise visible. Table I provides electrical results at 28C and 70C.

Subsequent to these measurements, the qualification panel was subjected to a "bend" test, the purpose of which was to closely replicate the "bend" tests of the flight array. These tests made certain that the "fixes" for the delaminations on the flight panels worked and verified that there were no additional areas on the panels that might delaminate that had not already delaminated.(Some of the flight panel substrates had delaminated in thermal vacuum exposure). Table I again shows that at both 28C and 70C, there was no significant change in electrical output and visual inspection showed no additional cracks.

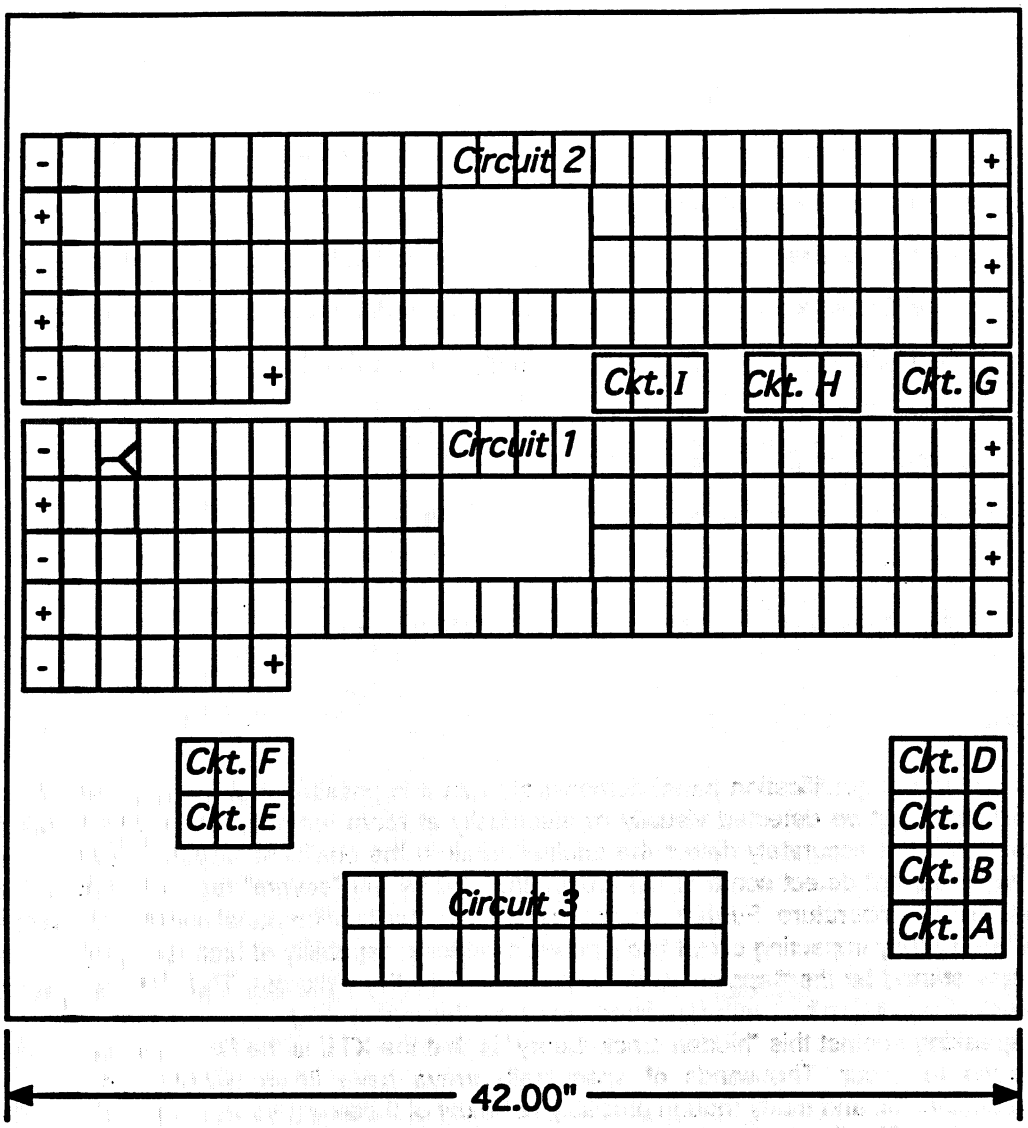

Figure 8
Sketch of the XTE Qualification Panel

As a last environmental exposure, the qualification panel was thermal cycled twice in vacuum between ambient temperature and a nominal 110C with two hour soaks at the extreme temperatures. The panel reached a maximum of 111.9C. Subsequent to this test there was no degradation at room temperature electrical testing, see Table I; but, there was a greater than 50% degradation at high temperatures and a mimicking of the electrical signature of the original crack on the XTE solar panel.

In addition, ten cells in circuit two were inspected with a hood and with the naked eye after the thermal cycle test. A large number of cracks that could not be seen prior to the test were visible. An inspection of the ten cells with a stereo microscope at room temperature and at 70C showed a very large proportion of the cracks visible at 70C that were not visible at 28C.

Table I
Electrical Output of Qualification Panel Circuit 2

Condition	Temp.	Curve Shape	Power Output (W)
Pre Tap Test	28	Slight Current Cut Off	42.5
Post First Tap Test	28	Sight Current Cut Off	42
Post Second Tap Test	28	Slight Current Cut Off	41.3
Post Bend Test	28	Slight Current Cut Off	40.2
Post Bake Test	28	Slight Current Cut Off	44.6
Pre Tap Test	70	Good	32.2
Post First Tap Test	70	Good	31.8
Post Second Tap Test	70	Good	31.7
Post Bend Test	70	Good	29.7
Post Bake Test	70	Cell Reversed	14.8

CONCLUSIONS

The tests run on the qualification panel demonstrate that it is possible that the array was launched with cell cracks that could not be detected visually or electrically at room temperature. Three organizations and several people could not accurately detect the original crack in the qualification panel at room temperature. Additionally, we could not detect some of the cracks induced by the "severe" tap test at room temperature, but could at elevated temperature. Further, thermal cycling the qualification panel seemed to make the hidden cracks worse by severely impacting circuit two's power producing capability at high temperature. Perhaps the cracks were only started by the "tapping" and then "finished" by the bake out. The flight panels underwent a similar sequence of tapping, albeit with less force, and then thermal cycling.

The fact speaking against this "hidden crack theory" is that the XTE is the first time such a phenomenon has been known to occur. Thousands of spacecraft arrays have flown without showing evidence of undetected cracked cells, and many though probably not most of these arrays were tap tested. There are two possible explanations. The first is that the XTE substrates delaminated in test and this resulted in numerous tap tests to the panels' cells, certainly far more than is usual. The second is that the XTE had unusually good telemetry on it. This allowed detection of signatures that definitely had to be cell cracks. Had the XTE had more typical telemetry it only would have been known that the array output was somewhat low, probably not enough to be concerned about.

RECOMMENDATIONS

We recommend that future flight solar panels undergo a visual inspection and an electrical output test at elevated temperatures. The electrical output test need not precisely determine the power output of the array but just the I-V curve shape. This test found the defect on the XTE qualification panel when room temperature tests did not. In addition, a similar test run on a NOAA K qualification panel found failed cell to interconnect connections, when room temperature testing did not. Fortunately the inspection and the test are inexpensive and quickly performed.

Secondly, we recommend that tap testing solar panels, usually performed to determine whether or not they have a delaminated area, be replaced by other less stressful testing. This testing could include acoustic transmittance through the panel, which is really quite equivalent to a tap test, a suction test where the cells

are pulled with a known force and observed for undue motion, or a pressure test where the cells are gently pushed with known force and observed for undue motion.