Current Single Event Effects Results for Candidate Spacecraft Electronics for NASA

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Abstract— **We present data on the vulnerability of a variety of candidate spacecraft electronics to proton and heavy ion induced single event effects. Devices tested include digital, analog, linear bipolar, and hybrid devices, among others.**

Keywords-component; SEE, add others

I. INTRODUCTION

As spacecraft designers use increasing numbers of commercial and emerging technology devices to meet stringent performance, as well as economic and schedule requirements, ground-based testing of such devices for susceptibility to single event effects (SEE) has assumed ever greater importance. The studies discussed here were undertaken to establish the sensitivities of candidate spacecraft electronics to heavy ion and proton-induced single event upsets (SEU), single event latchup (SEL), and single event transient (SET). Note: For proton displacement damage (DD) and total ionizing dose (TID) results please see the companion poster W-5 entitled "Current Total Ionizing Dose and Displacement Damage Results for Candidate Spacecraft Electronics for NASA" by Donna Cochran, et al. that is also being presented at the IEEE Nuclear and Space Radiation Effects Conference (NSREC) Data Workshop [1].

II. TEST TECHNIQUES AND SETUP

A. Test Facilities

All SEE tests were performed between February 2003 and February 2004. Heavy ion experiments were conducted at the Texas A&M University (TAMU) Cyclotron [2] and Single-event effects facility (SEETF) at the National Superconducting Cyclotron Laboratory (NSCL) at Michigan State University (MSU)[3]. The SEUTF uses a twin Tandem Van de Graaff

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accelerator while the TAMU facility uses an 88" cyclotron. The NSCL uses tandem K500 and K1200 cyclotrons to deliver on target ions with energies up to 125 MeV/n. Both facilities provide a variety of ions over a range of energies for testing. At both facilities, test boards containing the device under test (DUT) were mounted in the test area. For heavy ions, the DUT was irradiated with ions with linear energy transfers (LETs) ranging from 0.59 to 174 MeV•cm^2/mg. Fluxes ranged from $7.7x10^1$ to $2.5x10^5$ particles/cm^2 per second, depending on the device sensitivity. Representative ions used are listed in Table I. LETs between the values listed were obtained by changing the angle of incidence of the ion beam on the DUT, thus changing the path length of the ion through the DUT and the "effective LET" of the ion. Energies and LETs available varied slightly from one test date to another.

Proton SEE tests were performed at two facilities: the University of California at Davis (UCD) Crocker Nuclear Laboratory (CNL) [4], and the Indiana University Cyclotron Facility (IUCF) [5]. Proton test energies incident on the DUT are listed in Table II. Proton SEE tests were performed in a manner similar to heavy ion exposures. However, because protons cause SEE via indirect ionization of recoil particles, results are parameterized in terms of proton energy rather than LET. Proton tests also feature higher cumulative fluence and particle flux rates than do heavy-ion experiments.

Laser SEE tests were performed at the pulsed laser facility at the Naval Research Laboratory (NRL) [6] [7]. The laser light had a wavelength of 590 nm resulting in a skin depth (depth at which the light intensity decreased to 1/e - or about 37% - of its intensity at the surface) of 2 mm. A pulse rate of 100 Hz was chosen.

TABLE I. HEAVY ION TEST FACILITIES AND TEST HEAVY IONS

	Ion	Energy, MeV	LET in Si, MeV•cm^2/mg	Normal Incidence Range in Si, µm
TAMU	Ne^{20}	264-285	2.5-2.81	262-331
	Ar^{40}	496-561	8.05-8.9	174-224
	Cu^{63}	750	19.95	120
	Kr^{84}	912-953	28-29.3	116-122
	Ag^{107}	1200	42.85	100
	Xe^{129}	1291-1722	49.3-54	102-127
	Au^{197}	2955	80.2	155
	• Ne^{20}	545	1.7	799
	• Ar^{40}	991	5.4	493
	• Kr^{84}	2081	19.3	332
	• Xe^{129}	3197	37.9	286
	• 25 MeV per nucleon tune			
MSU	Ar^{36}	5148	1.5	8860
	Kr^{78}	9438	6.8	4440
	Xe^{136}	17816	14.1	3070
	Bi^{209}	15048	42	1100

TABLE II. PROTON TEST FACILITIES AND PARTICLES

Facility	Particle	Particle Energy,(MeV)
University of California at Davis (UCD) Crocker Nuclear Laboratory (CNL)	Proton	26.6-63
Indiana University Cyclotron Facility (IUCF)	Proton	54-197

TABLE III. OTHER TEST FACILITIES

Naval Research Laboratory (NRL) Pulsed Laser SEE Test Facility Laser: 590 nm, 1 ps pulse width, beam spot size ~1.2 µm

B. *Test Method*

Unless otherwise noted, all tests were performed at room temperature and with nominal power supply voltages.

1) *SEE Testing - Heavy Ion*

Depending on the DUT and the test objectives, one or more of three SEE test methods were used:

Dynamic – the DUT was exercised continually while being exposed to the beam. The errors were counted, generally by comparing DUT output to an unirradiated reference device or other expected output. In some cases, the effects of clock speed or device modes were investigated. Results of such tests should be applied with caution because device modes and clock speed can affect SEE results.

Static – the DUT was loaded prior to irradiation; data were retrieved and errors were counted after irradiation.

Biased (SEL only) – the DUT was biased and clocked while I_{CC} (power consumption) was monitored for SEL or other destructive effects. In some SEL tests, functionality was also monitored.

In SEE experiments, DUTs were monitored for soft errors, such as SEUs and for hard errors, such as SEL. Detailed descriptions of the types of errors observed are noted in the individual test results.

SET testing was performed using a high-speed oscilloscope. Individual criteria for SETs are specific to the device being tested. Please see the individual test reports for details. [9]

Heavy ion SEE sensitivity experiments include measurement of the saturation cross sections and the Linear Energy Transfer (LETth) threshold (the maximum LET value at which no effect was observed at an effect fluence of $1x10^7$ particles/cm^2).

2) *SEE Testing - Proton*

Proton SEE tests were performed in a manner similar to heavy ion exposures in many regards. Differences include measuring the SEE cross section as a function of proton energy as opposed to LET, as well as differences in cumulative fluence and particle flux rates.

3) *Pulsed Laser Facility Testing*

The DUT was mounted on an X-Y-Z stage in front of a 100x lens that produced a spot size of about 1.2 μm FWHM. The X-Y-Z stage could be moved in steps of 0.1 μm for accurate positioning of SEU sensitive regions in front of the focused beam. An illuminator together with a CCD camera and monitor were used to image the area of interest, thereby facilitating accurate positioning of the device in the beam. The pulse energy was varied in a continuous manner using a polarizer/half-waveplate combination and the energy was monitored by splitting off a portion of the beam and directing it at a calibrated energy meter.

4) *Charge Collection Testing*

A four probe Ion Beam Induced Charge Collection (IBICC) measurement was used to simultaneously measure the charge presented on the collector, emitter, base, and substrate terminal due to a series of ion strikes occurring in and around the transistor's area.

III. Test Results Overview

Abbreviations and conventions are listed in Table IV. Abbreviations for principal investigators (PIs) are listed in Table V. SEE test result categories are summarized in Table VI and SEE results are summarized in Table VII. Unless otherwise noted, all LETs are in MeV•cm^2/mg and all cross sections are in cm^2/device. This paper is a summary of results. Complete test reports are available online at http://radhome.gsfc.nasa.gov [8].

TABLE V. List of Principal Investigators

Abbreviation	Principal Investigator (PI)
SB	Steve Buchner
JH	Jim Howard
SK	Scott Kniffin
RL	Ray Ladbury
PM	Paul Marshall
TO	Tim Oldham
RR	Robert Reed
TS	Anthony (Tony) Sanders

TABLE VI. List of Categories

Following ground SEE irradiation, devices generally are categorized into "useability" categories for spacecraft interest. Recommendations for SEE are color coded according to the following key:

Category 1:	Recommended for usage in all NASA/GSFC spaceflight applications
Category 2:	Recommended for usage in NASA/GSFC spaceflight applications, but may require mitigation techniques
Category 3:	Recommended for usage in some NASA/GSFC spaceflight applications, but requires extensive mitigation techniques or hard failure recovery mode
Category 4:	Not recommended for usage in any NASA/GSFC spaceflight applications
RTV:	Research Test Vehicle - Please contact the P.I. before utilizing this device for spaceflight applications

TABLE IV. Abbreviations and Conventions

H = heavy ion test
P = proton test (SEE)
L = laser test
CC = Charge Collection
LET = linear energy transfer (MeV•cm^2/mg)
LETth = linear energy transfer threshold (the maximum LET value at which no effect was observed at an effective fluence of 1x10^7 particles/cm^2)
SEE = single event effects
SEU = single event upset
SEL = single event latchup
SET = single event transient
SEFI = single event functional interrupt
SEB = single event burnout
SEGR = single event gate rupture
BER = Bit Error Rate
< = SEE observed at lowest tested LET
> = No SEE observed at highest tested LET
σ = cross section (cm^2/device, unless specified as cm^2/bit)
σ_{SAT} = saturation cross section at LET_{MAX} (cm^2/device, unless specified as cm^2/bit)
LDC = Lot Date Code
DAC = Digital to Analog Converter
DUT = Device Under Test
N/A = Not Applicable
Cat. = Category
P.I. = Principal Investigator
Samp. = Sample
HI = Heavy Ion
P = Proton
N/A = Not Applicable
Cat. = Category
ADC = Analog to Digital Converter
ASIC = Application Specific Integrated Circuit
BERT = Bit Error Rate Tester
CMOS = Complementary Metal Oxide Semiconductor
DAC = Digital to Analog Converter
FPGA = Field Programmable Gate Array
HBT = Heterojunction Bipolar Transistor
NV = Non-Volatile
NVM = Non-Volatile Memory
OPTO = Optocoupler
PWM = Pulse Width Modulator
RHrFPGA = Radiation Hardened Re-programmable Field-programmable Gate Array

TABLE VII. SUMMARY OF SEE TEST RESULTS

Part Number	Manufacturer	LDC	Device Function	Process	Particle: (Facility,Date) P.I.	Test Results LET in MeV•cm²/mg σ in cm²/device, unless otherwise specified	SEE Cat.	Supply Voltage	Samp. Size	Test Report
Logic Devices										
54AHCT32	Texas Instrument	0251	OR Gate	CMOS	HI: (TAMU) JH	SEL LET_{th} >53.1; SET LET_{th} >53.1	1	5/5.5V	2	T032803_54AHCT32
54BCT125	Texas Instrument	0251	Quadruple Bus Buffer Gate, 3 state output	BiCMOS	HI: (TAMU) JH	SEL LET_{th} > 53.1; SET LET_{th} ~8; σ_{SAT} ~1.1 x 10^{-4}	2	5/5.5V	2	T032803_54BCT125
SN54LVT162244A	Texas Instrument	0301	16-Bit Buffers/Drivers	BiCMOS	HI: (TAMU) JH	SEL LET_{th} > 76.2; SET LET_{th}~18; σ_{SAT} ~ 1 x 10^{-4}	2	3.3V	2	T061803_ SN54LVT162244A
SN54BCT244W	Texas Instrument	0252	Octal Line Driver	CMOS	HI: (TAMU) JH	SEL LET_{th} >53.1; SET LET_{th} ~9; σ_{SAT} ~2x10^{-4}	2	5/5.5V	2	T032803_ SN54BCT244W
SNJ54ABT16244WD	Texas Instrument	0230	16-Bit Buffer/Driver	BiCMOS	HI: (TAMU) JH	SEL LET_{th} >53.1; SET LET_{th} >53.1	1	5/5.5V	3	T032803_ SNJ54ABT16244WD
SN54LVT16245B	Texas Instrument	0302	Octal Buffer/Driver	BiCMOS	HI: (TAMU) JH	SEL LET_{th} > 76.2; SET LET_{th} ~5; σ_{SAT} ~ 7 x 10^{-5}	2	3.3V	2	T061303_ SN54LVT16245B
SN64BCT126A	Texas Instrument	0144	Quadruple Bus Buffer Gate, 3 state output	BiCMOS	HI: (TAMU) JH	SEL LET_{th} > 53.1; SET LET_{th} ~8; σ_{SAT} ~ 2.5 x 10^{-4}	2	5/5.5V	2	T032803_ SN64BCT126A
SN64BCT244	Texas Instrument	0144	Buffer/Driver	BiCMOS	HI: (TAMU) JH	SEL LET_{th} > 76.2; SET LET_{th} ~9; σ_{SAT} ~ 4.2 x 10^{-4}	3	5V	2	T061803_ SN64BCT244
SN64BCT245	Texas Instrument	0240	Octal Bus Transceiver, 3 state output	BiCMOS	HI: (TAMU) JH	SEL LET_{th} > 53.1; SET LET_{th} < 20; σ_{SAT} ~ 2.5 x 10^{-4}	2	5/5.5V	2	T032803_ SN64BCT245
SN74LVT244B	Texas Instrument	0248	Octal Buffer/Driver	Bipolar	HI: (TAMU) JH	SEL LET_{th} > 53.1; SET LET_{th} ~5; σ_{SAT} ~7 x 10^{-5}	2	3.3/3.6V	2	T032803_ SN74LVT244B
SN74LVCC3245	Texas Instrument	0236	Octal Bus Transceiver	BiCMOS	HI: (TAMU) JH	SEL LET_{th} > 53.1; SET LET_{th} > 53.1	1	3.3/3.6V	1	T032803_ SN74LVCC3245
IDT74LVC2244A	Texas Instrument	0025	Octal Buffer/Driver	CMOS	HI: (TAMU) JH	SEL LET_{th} > 53.1; SET LET_{th} > 53.1	1	3.3/3.6V	3	T032803_ IDT74LVC2244A
Memory Devices										
HX6228	Honeywell	No LDC (Test Chip)	128k x 8 SRAM	SOI	P: (IU) SK P: (UCD) SK	IU: SET σ_{MAX} 2.1x10^{-11} (σ varies with angle) UCD: SET σ_{MAX} 2.1x10^{-11}(σ varies with angle)	2	5V	2	D031504_RS422
CRAM test chip	BAE Systems / Ovonyx	No LDC (Test Chip)	Chalcogenide RAM	CMOS	HI: (TAMU) TO	SEL LET_{th} >116; SEL σ_{MAX} >2x10^{-6}; SET LET_{th} >116(static); <55 (dynamic); SET σ ~ 2x10^{-5}@ LET=89	2	3.3V	2	T091603_CRAM
Floating Gate	Motorola	No LDC (Test Chip)	512k x 8 NV Memory	CMOS	HI: (TAMU) TO	SEL LET_{th} >53; SEU 5x10^{-8} @ LET=53	2	5.5/4V	1	T022204_Motorola
Si-Nano NVMs	Motorola	No LDC (Test Chip)	512k x 8 NV Memory	CMOS nano-crystal	HI: (TAMU) TO	SEL LET_{th} >53; SEU LET_{th} <8.7; SEU σ >2x10^{-8} @ LET=53	2	3.3/2.2V	5	T022204_Motorola
M65656	Matra	9535	32k x 8 SRAM	CMOS	HI: (MSU) RL/RR	SEU σ = 1.25x10^{-2} @ LET=6.3; SEU σ = 4.9x10^{-2} @ LET=8.7	2	5V	1	ref: Late news MSU pub by RR&RL
IDT71256	IDT	N/A	256k Memory	CMOS	HI: (MSU) RL/RR	SEU σ = 1.0x10^{-3} @ LET=6.3; SEU σ = 4.5x10^{-3} @ LET=8.7	2	5V	1	ref: Late news MSU pub by RR&RL
ASIC Devices										
T36T-GAFE7	Agilent	Nov03	ASIC	CMOS	HI: (TAMU) SK	2.7<SEU LET_{th}<8.3, SEU σ_{SAT} ~4x10^{-5}; SEL LET_{th} >51.5	3	5V	2	T111103_GLAST
T36T-GAFE5G	Agilent	Sep03	ASIC	CMOS	HI: (TAMU) SK	2.7<SEU LET_{th}<8.3, SEU σ_{SAT} ~4x10^{-5}; SEL LET_{th} >51.5	3	5V	2	T111103_GLAST
T36T-GARC3	Agilent	Nov03	ASIC	CMOS	HI: (TAMU) SK	2.7<SET/SEFI LET_{th}<8.3; SET/SEFI σ_{SAT} ~1x10^{-4}; SEL LET_{th} >51.5	3	5V	2	T111103_GLAST
Mixed Signal or Linear Devices										
MAX145	Maxim	0310	ADC	CMOS	HI: (TAMU) SK	SEU LET_{th} ~17, SEU σ_{SAT} ~2.8x10^{-5}; SEFI LET_{th} ~10, SEFI σ_{SAT} ~1.1x10^{-6}	3	2.7V	3	T111103_GLAST
MAX494	Maxim	0229	Quad Op Amp	Bipolar	HI: (TAMU) SK	SEL LET_{th} >106.3; SET LET_{th} <35; σ_{SAT} ~8 x 10^{-4}	3	2.5V	2	T032803_MAX494
MAX5121	Maxim	0134	DAC	CMOS	HI: (TAMU) SK	SEU LET_{th} ~18, SEU σ_{SAT} ~8x10^{-4}; SEFI LET_{th} ~18, SEFI σ_{SAT} ~4x10^{-6}	3	3/5V	3	T111103_GLAST; T022404_GLAST
MSK5275	M.S. Kennedy Corp.	0312	Voltage Regulator	Hybrid	HI: (TAMU) JH	SEL LET_{th} > 8.7; SET: oscillation mode immediately upon exposure; power cycle required to recover normal operations	3	5V	2	T061803_MSK5275
LM-117	National Semiconductor	0302	Voltage Regulator	Bipolar	HI: (TAMU) JH	SEL LET_{th} >76.2; SET LET_{th} ~6; σ_{SAT} ~1 x 10^{-2}	3	-48V	3	T061803_LM117
UCC1806	Unitrode	0302	Pulse Width Modulator Controller	Bipolar	HI: (TAMU) JH	SEL LET_{th} >76.2; SET LET_{th} ~1 [~9 (dropout)]; σ_{SAT} ~1.0 x 10^{-3} [1.7 x 10^{-4} (dropout)]; typical dropout duration is on the order of a few milliseconds	4	12V	3	T061703_UCC1806

TABLE VII. SUMMARY OF SEE TEST RESULTS (CONT.)

Part Number	Manufacturer	LDC	Device Function	Process	Particle: (Facility,Date) P.I.	Test Results LET in MeV•cm²/mg σ in cm²/device, unless otherwise specified	SEE Cat.	Supply Voltage	Samp. Size	Test Report
DC-DC Converters and Related Devices										
DVFL286R7S-R	VPT	F0001 & F0004	DC/DC Converter	Hybrid	HI: (TAMU) SB/JH	SEL LET_{th} >53.1; SET LET_{th} ~28.8; SET σ [varies with input voltage and output load conditions]; worst case condition 28V input 90% load $7x10^{-5}$	3	28V	2	T032703_DV
DVTR2815D-R	VPT	F0002 & F0004	DC/DC Converter	Hybrid	HI: (TAMU) SB/JH	SEL LET_{th} >53.1; SET LET_{th} ~28.8; SET σ < $1x10^{-7}$	2	28V	2	T032703_DV
MAX1523	Maxim	Markings: AAOY CYR	DC/DC boost Controller	CMOS	HI: (TAMU) SK	SET and SEL LET_{th} > 76.2; SET and SEL σ <$1x10^{-7}$ @ LET=76.2	1	5V	2	T061703_GLAST
MAX1809	Maxim	0301	DC/DC Converter	CMOS	HI: (TAMU) SK	SET LET_{th} <2.78; SET σ_{SAT} ~ $5.9x10^{-4}$	3	5V	2	T061703_GLAST
MAX1847	Maxim	0313	Inverting DC/DC Converter	CMOS	HI: (TAMU) SK	53.9<SEL LET_{th}<76.2	4	5V	2	T061703_GLAST
MAX1951	Maxim	0237	DC/DC Regulator	CMOS	HI: (TAMU) SK	2.8<SET LET_{th}<4.0, SET σ = $1.7x10^{-4}$	4	5V	2	T061703_GLAST
MAX724	Maxim	0248	DC/DC Regulator	Bipolar	HI: (TAMU) SK	SEL and SET LET_{th} >76.2; SET and SEL σ <1 x 10^{-8}	1	5V	4	T061703_GLAST
MAX726	Maxim	0313	DC/DC Regulator	Bipolar	HI: (TAMU) SK	SEL and SET LET_{th} >76.2; SET and SEL σ <1 x 10^{-8}	1	5V	3	T111103_GLAST; T061703_GLAST
AFL2803R3S	International Rectifier	0351	DC/DC Converter	Hybrid	HI: (TAMU) SK	SEGR LET_{th} > 53.9, SET LET_{th} < 20; SET σ_{SAT} ~$2.7x10^{-5}$; 34.5<SEU LET_{th}<37.2, SEU σ_{SAT} ~$1.9x10^{-5}$	3	27/28/29V	2	T022304_MAX724_ AFL2803R3S
SiGe Devices										
5AM [Test Sample]	IBM	N/A	SiGe 5AMSTC	5AM	HI: (TAMU) PM/RL	SEU sensitive depending on operational conditions; See [Marshall_tns04]	RTV	N/A	2	nsrec04_marshall
JAZZ	IBM	N/A	SiGe JAZZ	JAZZ	HI: (TAMU) PM/RL	SEU sensitive depending on operational conditions; See [Marshall_tns04]	RTV	N/A	2	nsrec04_marshall
7HP [Test Sample]	IBM	N/A	SiGe 127 bit SR	7HP	HI: (TAMU) PM/RL	SEU sensitive depending on operational conditions; See [Marshall_tns04]	RTV	N/A	2	nsrec04_marshall
Communication Devices										
PE926C31	Perigrine	N/A (Test Chip)	RS422 Driver	SOS	P: (IU) SK P: (UCD) SK/PM	IU: SET σ < $2.9x10^{-13}$ (198 MeV) UDC: SET σ < $1x10^{-13}$ (63 MeV)	1	5V	2	D031504_RS422
PE926C32	Peregrine	N/A (Test Chip)	RS422 Receiver	SOS	P: (IU) SK P: (UCD) SK/PM	IU: SET σ < $2.9x10^{-13}$ (198 MeV) UCD: SET σ < $1x10^{-13}$ (63 MeV)	1	5V	2	D031504_RS422
TSS901E	ATMEL	0013	1355 Protocol	CMOS	HI: (TAMU) SB; Laser: (NRL) SB	HI: SEL LET_{th} >79; SEFI LET_{th} ~29; SEU LET_{th} ~12; SEU σ_{SAT} ~$5x10^{-4}$; SEFI σ_{SAT} ~$1.3 x 10^{-4}$; SEFI required softward reboot Laser: Three failure modes observed: miscompares, link errors, and system crashes.	2	5V	1	NRL_112103_ TSS901E; T031604_TSS901E; T090203_TSS901E
UT54LVDS217	Aeroflex	0312	Serializer	CMOS	P: (IU) SB	SETσ = $2x10^{-12}$ and $1x10^{-11}$ (74 MeV) $8x10^{-12}$ and $3x10^{-11}$ (198 MeV) BER = $2x10^{-22}$ and $1x10^{-21}$ (74 MeV) $1.02x10^{-21}$ and $2.73x10^{-21}$ (198 MeV)	3	3.3V	2	I102903_ UT54LVDS217
S2064	AMCC	0303	Transceiver	CMOS	HI: (TAMU) JH	SEU LET_{th} <2; σ_{SAT} $4x10^{-5}$ (bit errors), $5x10^{-3}$ (small burst errors), $4x10^{-4}$ (large burst errors); SEL LET_{th} >28.5; No destructive events to 53.1; low LET_{th} implies a proton sensitivity	3	3.3V	2	T083103_S2064
Miscellaneous Devices										
RHrFPGA	Honeywell	0314	FPGA	0.35um SOI	HI: (TAMU) TS P: (IU) TS	HI: SEU LET_{th} >174; SEU σ <$1x10^{-7}$ @ LET 174 P: SEU σ <$2.9x10^{-4}$ (198 MeV)	1	3V	2	T090203_RHrFPGA_ Honeywell; I103003_RHrFPGA_ Honeywell
CD21CD	Teledyne	0312	Solid-State Relay (OPTO)	Hybrid	HI: (TAMU) JH	SEL LET_{th} >76.2; SET LET_{th} >76.2	1	9.5V	1	T061803_CD21CD
OMR9701	International Rectifier	0313	Solid-State Relay (OPTO)	Hybrid	HI: (TAMU)SB	SEE LET_{th} >29.3	2	5V	1	T061303_OMR9701
JANS2N2222A	Microsemi	0137	NPN Silicon Switching Transistor	Bipolar	HI: (TAMU) JH	SET LET_{th} > 53.1	1	20V	2	T032803_ JANS2N2222A
HV583	SuperTex	N/A	Controller	Microshutter Array (MSA)	HI: (TAMU) SB	SEL LET_{th} > 55.3; SEU LET_{th} < 8.9	2	5/30V	2	T022404_HV583

TABLE VIII. SUMMARY OF SEL TEST RESULTS

Part Number	Manufacturer	LDC	Device Function	Process	Particle: (Facility,Date) P.I.	Test Results LET in MeV•cm²/mg σ in cm²/device, unless otherwise specified	SEE Cat.	Supply Voltage	Samp. Size	Test Report
80387	Intel	9809	Math Coprocessor	CMOS	HI: (TAMU) TS	14.9 < SEL LET_{th} <28; σ_{SAT} = 1.5x10^{-4}	3	5V	2	T032603_80387
XA-16	AMS	Flight Lot	ASIC	CMOS	HI: (TAMU) JH	SEL LET_{th} ~8; σ_{SAT} ~3 x 10^{-3}	3/4	+5V digital +/-5V analog	4	T061803_XA16
TC55257	Toshiba	0030	32k x 8 SRAM	CMOS	HI: (TAMU) SB	SEL LET_{th} >123	1	5V	2	T032803_TC55257
T36T-GTFE	Agilent	N/A	ASIC	CMOS	HI: (TAMU) SK	SEL LET_{th} >51.5; SEL σ <4.0x10^{-6} @ LET=51.5	2	5V	2	T022404_GLAST
T36T-GTRC	Agilent	N/A	ASIC	CMOS	HI: (TAMU) SK	SEL LET_{th} >51.5; SEL σ <4.0x10^{-6} @ LET=51.5	2	5V	2	T022404_GLAST
AD7675	Analog Devices	No LDC (Test Chip)	ADC	CMOS	HI: (TAMU) RL/TS	SEL LET_{th} <8.6	4	5V	2	T111603_AD7675
ADS8323	Texas Instrument	No LDC (Test Chip)	ADC	CMOS	HI: (TAMU) RL/TS	SEL LET_{th} ~17.2	4	5V	2	T111603_ADS8323

IV. FEATURED TEST RESULTS AND DICUSSION

As in our past workshop compendia of GSFC test results, each DUT has a detailed test report available online at http://radhome.gsfc.nasa.gov [8] describing in further detail test method, SEE conditions/parameters, test results, and graphs of data. This section contains a summary of testing performed on a selection of featured parts.

A. Si-Nanocrylstal NVMs

Shown in Figure 1 are the bit errors in a 4M nanocrystal nonvolatile memory for exposures of 1x10^7 particles/cm^2. The memories were produced by Freescale (Motorola), as part of their 90 nm technology development. Both static and dynamic (10kHz) read testing were performed, but all the errors appeared to be static errors, corresponding to electrons lost off the nanocrystal storage element. No errors were observed which could be attributed to the control circuits. These memories are normally programmed by channel hot electron injection and erased by Fowler-Nordheim tunneling, much like floating gate nonvolatile memories. Further testing of the write and erase modes is planned. [T022204_Motorola]

B. AMCC S2064

The AMCC S2064 1.3 GHz Quad Serial Transceiver was monitored for latchup induced high power supply currents and data disruptions and errors by exposing it to a number of heavy ion beams at the Texas A&M University Cyclotron Single Event Effects Test Facility.

Difficulties were encountered during the de-lidded process. The DUT die was encapsulate in two plastics, an outer plastic covers the inner plastic and the top arc of the bond wires. This outer plastic was etched by fuming nitric acid. The inner plastic was insensitive to this acid and needed to be removed by an application of sulfuric acid. During the first effort to de-lid the devices where complete exposure of the die was the goal, the de-lidding process appeared to proceed normally. Initial inspection of the uncovered die appeared normal. However, when the de-lidded devices were taken to the facility, all the bond wires had lifted from the die surface, yielding non-functional devices. The second de-lidding process was to remove as much of the second encapsulant without exposing the bond wires. As this was a very sensitive process, the two devices that were successfully de-lidded had slightly different overlayer thicknesses (12 and 7 mils, for DUTs 1 and 2 respectively).

The test configuration utilized a 3.6 GHz Bit Error Rate Tester (BERT) with generator and detector/analyzer. The DUT was mounted on a commercial board specifically designed for radiation testing of this part. The test setup was wired for either one pass through the DUT or four passes. For further details on the test set-up see the test report "Single Event Effects (SEE) Testing of the AMCC S2064 1.3 GHz Quad Serial Transceiver". [ref: T083103_S2064]

The Xenon particles did not have sufficient range to penetrate into the sensitive regions after passing through the inner encapsulant layer. Therefore, the Xenon beam could not give a sufficient test for latchup. The highest LET beam available with sufficient penetration range was Krypton, but only for DUT 2 with the 7 mil overlayer. After being exposed to 1 x 10^7 Kr ions/cm^2, no latchup events were observed on the 7 mil DUT, therefore, the latchup threshold for the S2064 devices is greater than 28.5 MeV•cm^2/mg.

The simplest method for processing the data is to determine the total number of errors produced in a given run and determine the upset cross-section from the total ion fluence for that run. However, if any events occurred that produced more than one error for a given ion, then this method would misrepresent the upset rate. These multiple bit events, or burst errors were seen during testing of the AMCC S2064. To account for burst errors, a definition of when a burst error starts and stops was defined. We defined this condition to be two control characters (20 bits) being passed correctly. That is, if a second bit error is encountered before 20 bits have transferred correctly, then a burst error has occurred. The burst length (how long the burst error condition lasts in bits, erroneous and valid bits combined) is defined by the start bit as above and the bit that starts 20 correct bits (i.e., two correct control characters were passed). Post-processing the data in this fashion yields single bit errors and burst errors (each burst error has an associated burst length).

A histogram of the burst length was viewed on the BERT and there was a double peak structure noted. Burst lengths ranged from 2 bits up to about 600 – 700 bits, then there were no burst lengths until greater than 6000 bits. It was determined that this second peak in the histogram was from burst events

that were lasting so long that the BERT initiated a RESYNC event and recovered normal operation after the RESYNC. All burst events that lasted less than 700 bits returned to normal operation without any intervention by the BERT system. Therefore, the burst errors in this analysis were split into two categories – ones that recovered with no intervention and ones that required intervention to resume normal operations. These are referred to as small and large burst events, respectively.

Figure 2 shows the cross-section versus LET curve for the single bit errors. There are three results of interest for the single bit error case. First the single bit error upset mode was more than an order of magnitude lower in cross-section than for burst errors. Second, there is little difference between the one-pass and four-pass cases. This implies, at least for the statistic levels of these observations, that the single bit errors are not produced in the data transmitting/receiving stages that are quadrupled in the four-pass case. Third, the errors were produced by all ion beams used, even the Neon beam. This means the LETth to produce single bit errors is >2 MeV•cm^2/mg, implying that protons are likely to produce these events (via spallation reactions and possibly via direct ionization). No proton testing was done to investigate this possibility but is highly recommended.

Figure 3 and Figure 4 show the cross-section for small and large burst errors as a function of the LET. Comparing the saturation cross-section levels of these curves with that for the bit errors, the more than an order of magnitude difference is easily seen. The small burst error events are the most likely events, followed by the large burst errors, and finally by the single bit errors.

Unlike the single bit error case, the burst errors do seem to be sensitive to the number of passes through the DUT. While the exact factor of four is not seen, Figure 3 and Figure 4 do show that the four-pass case is significantly larger than the single-pass case. This implies that the data transmission/receiving section of the device is the main area sensitive to producing burst-type errors.

In summary, all three types of errors observed were seen at the lowest test LET (2 MeV•cm^2/mg), yielding threshold LETs of less than two. Saturation cross-sections for the three error modes were 4 x 10^{-5} cm^2 (bit errors), 5 x 10^{-3} cm^2 (small burst errors), 4 x 10^{-4} cm^2 (large burst errors).

The AMCC S2064 1.3 GHz Quad Serial Transceivers are considered category 3 devices. While no destructive events were observed to the highest LET able to penetrate the overlayer (approximately 28 MeV•cm^2/mg), the upset rate and modes may require substantial mitigation to achieve successful operation. Additionally, the low threshold LET implies a proton sensitivity that was not investigated. Space-borne rates could be substantially higher than predicted with heavy ions alone if proton sensitivity is shown, especially if the devices are sensitive to direct proton ionization.

C. *Honeywell RHrFPGA*

Heavy Ion testing was performed at Texas A&M University Radiation Effects Facility on the Honeywell Radiation-Hardened re-programmable Field-Programmable Gate Array (RHrFPGA). Testing characterized the RHrFPGA Single Event Upset (SEU) sensitivity to verify compliance with its Soft Error Rate (SER) radiation design requirements. The test evaluated the FPGA using eight different test programs and configurations. Seven were optimized for SEU testing to evaluate specific internal memory elements within the FPGA, and one test program represented a current RHrFPGA application. The RHrFPGA test devices did not experience SEU or other SEE to the maximum available test LET of 174 MeV•cm^2/mg at minimum rated supply voltage (3.0 V). This result applied to all eight tests for fluences of 1.0x10^7 ions/cm^2 per test.

Proton testing was performed at Indiana University Cyclotron Facility. Testing characterized RHrFPGA sensitivity to proton-induced SEU. The test included six different test programs and FPGA configurations, which were optimized to evaluate the RHrFPGA's two unique types of memory elements. The RHrFPGA test device was irradiated to a proton fluence of 3.4 x 10^{13} p/cm^2 at 203 MeV beam energy, corresponding to 2.0 Mrad(Si) total dose per device. The test parts did not exhibit SEU or any other SEE, demonstrating that the RHrFPGA is essentially immune to proton-induced SEU. [T090203_RHrFPGA_Honeywell] [I103003_RHrFPGA_Honeywell]

V. Summary

We have presented recent data from SEE on a variety of mainly commercial devices. It is the authors' recommendation that this data be used with caution. We also highly recommend that lot testing be performed on any suspect or commercial device.

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