Silicon Carbide Schottky Barrier Diode

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Abstract

This chapter reviews the status of SiC Schottky barrier diode development. The fundamental of Schottky barrier diodes is first provided, followed by the review of high-voltage SiC Schottky barrier diodes, junction-barrier Schottky diodes, and merged-pin-Schottky diodes. The development history is reviewed and the key performance parameters are discussed. Applications of SiC SBDs in power electronic circuits as well as other areas such as gas sensors, microwave and UV detections are also presented, followed by discussion of remaining challenges.

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1. Introduction

Silicon Carbide was one of the earliest semiconductor materials discovered. However, due to the difficulties of growing good quality crystals, the progress of SiC devices has lagged behind those of its counterpart materials. In recent years, SiC devices development have enjoyed remarkable progress and demonstrated significant advantages over Si devices in the area of high power electronics due to its superior physical and electrical properties.

With a significantly wider band gap (2.3eV for 3C-SiC, 2.9eV for 6H-SiC and 3.3eV for 4H-SiC) than silicon, the critical field of SiC is approximately eight to ten times higher than that of the latter. As a result, SiC high voltage devices can be realized on much thinner drift layers with higher doping, leading to orders-of-magnitude lower device on-state resistance.

Silicon Carbide (SiC) Schottky Barrier Diode (SBD) was the first SiC power device demonstrated. It was studied as early as 1974 [1]. Throughout the years, as single-crystalline SiC material became commercially available and its quality improved steadily, substantial amount of work and study has been done on SiC SBDs as well as Merged P-i-N Schottky diodes (MPS) and Junction Barrier Schottky (JBS) diodes. Schottky contacts on 3C, 6H and 4H SiC with a large variety of metals were made and their performance studied. Device designs on SBD, MPS and JBS diodes were also extensively investigated. Impressive progresses and developments have been made. Recently, SiC SBDs with breakdown voltage higher than 10kV has been reported [2]. SiC MPS diodes capable of ??kV were also reported [3]. SiC SBD has proved itself to be an important device as it became the first commercially available SiC power device. It is poised to replace existing Si power fast recovery diode in most power electronics applications because of their orders-of-magnitude faster speed, substantially reduce system losses and improve system efficiency.

In this chapter, recent developments on physics of Schottky contact study, the design and development of power and high voltage SiC SBD, MPS and JBS diodes and their applications in power electronics will be reviewed and summarized.

2. SiC Schottky Contacts

2.1 Theory of SiC Schottky contact

When a metal is making intimate contact with SiC material, the Fermi levels in the two materials must be coincident at thermal equilibrium and the vacuum level must be continuous across the interface. In addition, the metal work function is different from that of the semiconductor. These two requirements determine a unique energy band diagram for an ideal metal-semiconductor contact where surface states are absent, as shown in figure 1 [4]. (In this discussion we will refer principally to n-type semiconductors. Similar arguments apply for p-type semiconductors). For this ideal case, the potential barrier at the metal-semiconductor interface is simply the difference between the metal work function ϕ_M and the electron affinity of the semiconductor χ_S:

$$q\phi_{Bn} = q(\phi_M - \chi_s) \quad (1)$$

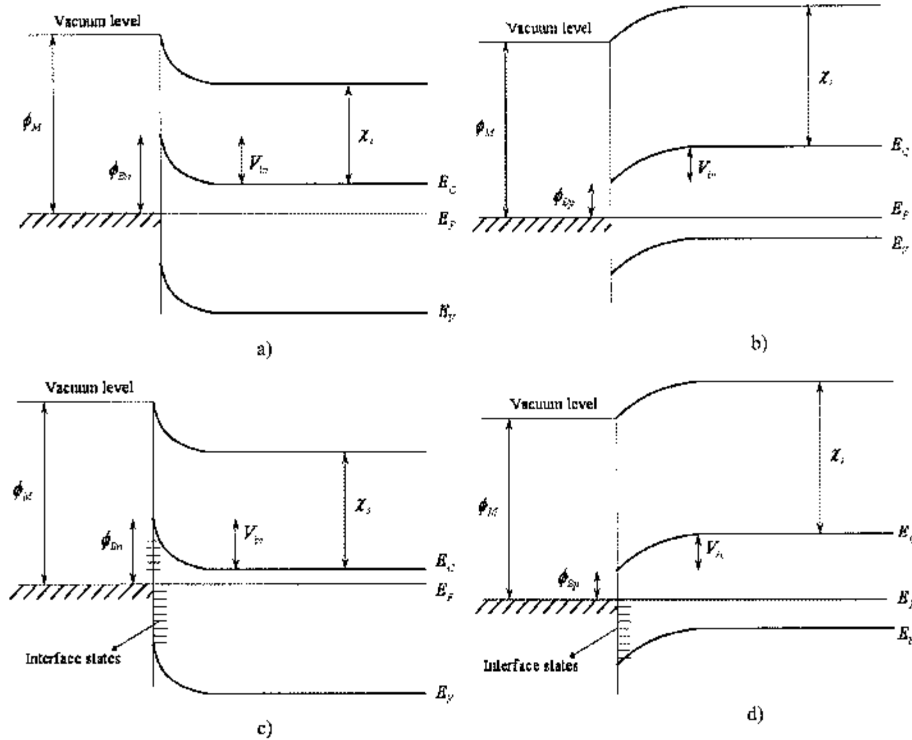


Fig. 1 Energy band diagram of metal-semiconductor contact. a) n-type SiC contact, b) p-type SiC contact without interface states, c) n-type SiC contact and d) p-type SiC contact with a large amount of interface states.

If the semiconductor material is p-type, the barrier height can be determined using a similar procedure:

$$q\phi_{Bp} = E_g - q(\phi_M - \chi_s) \tag{2}$$

In these equations, q is the electron charge and E_g is the band gap energy. The barrier potential determines the characteristics of a metal-semiconductor contact. Note that these equations apply to the ideal MS contact where the interface states have been neglected (parts a and b of Fig. 1).

The other extreme case would be that when the interface state density is large, the position of the Fermi level is pinned down to a certain level within the forbidden gap of the semiconductor. In this case, the barrier height

$$\phi_{Bn} = E_g - E_F \tag{3}$$

will be independent of the metal work function. This case is often referred to as Bardeen's limit. Most metal-semiconductor contacts in reality do have interface states but they are typically not large enough to pin down the Schottky contact barrier height. Therefore, their barrier heights will be affected by both the metal work function as well as the interface state density. In practice, the barrier heights are found to be dependent on the

SiC poly-type, the metal, the surface condition before contact formation and the interfacial chemistry.

If the presence of a thin layer of insulator between the metal and the SiC material is taken into account, the barrier height can be given as follows.

$$\phi_{Bn} = [c_2(\phi_m - \chi) + (1 - c_2)(\frac{E_g}{q} - \phi_0) - \Delta\phi_b]$$
$$+ \left\{ \frac{c_2^2 c_1}{2} - c_2^{1/2} \left[c_1(\phi_m - \chi) + (1 - c_2)(\frac{E_g}{q} - \phi_0)\frac{c_1}{c_2} - \frac{c_1}{c_2}(V_n + \frac{kT}{q}) + \frac{c_1^2 c_2}{4} \right]^{1/2} \right\} \quad (4)$$

where $c_1 = \frac{2q\varepsilon_s(N_d - N_a)\delta^2}{\varepsilon_i^2 \varepsilon_0}$, and $c_2 = \frac{\varepsilon_i \varepsilon_0}{\varepsilon_i \varepsilon_0 + q^2 \delta D_s}$

Where ϕ_{Bn} denotes the barrier height at flat band condition, $\Delta\phi_b$ is the image force lowering of the potential barrier, and

$$\Delta\phi_b = \sqrt{\frac{q\mathrm{E}_m}{4\pi\varepsilon_s}} \quad (5)$$

Where δ is the thickness of the insulating layer, E_m is the field intensity at the surface of the semiconductor, ε_i and ε_s are the absolute dielectric constants of the insulator and the semiconductor, respectively, and D_s is the density of the interface states.

There are four mechanisms that contribute to the current density of current transport across a metal-semiconductor interface: (i) thermionic emission over the potential barrier, (ii) quantum-mechanical tunneling of the carriers through the potential barrier, (iii), carrier recombination in the depletion region and (iv) carrier recombination in the neutral region of the semiconductor [5]. For wide band gap semiconductor materials such as SiC, the dominant contribution to the current transport comes from the thermionic emission (TE) of electron over the barrier and the tunneling of the electron through the barrier. If the SiC material of Schottky contacts is not heavily doped and the operating temperature is not very low, the thermionic emission (TE) term will be dominant. The tunneling term will only be significant if the SiC is heavily doped, the device is operating under low temperatures or is blocking high reverse voltage. The thermionic emission current can be expressed as:

$$\begin{aligned} J_n &= [A^* T^2 \exp(-\frac{q\phi_{Bn}}{kT})][\exp(\frac{qV}{kT} - 1)] \\ &= J_{ST}[\exp(\frac{qV}{kT} - 1)] \end{aligned} \quad (6)$$

where $J_{ST} \equiv A^* T^2 \exp(-\frac{q\phi_{Bn}}{kT})$, $A^* = \frac{4\pi q m^* k^2}{h^3}$

The tunneling current can be written as:

$$J = J_S[\exp(qV / nkT) - 1] \quad (7)$$

where J_S is the saturation current density obtained by extrapolating the current density from the log-linear region to V=0 and n is the ideality factor defined as

$$n \equiv \frac{q}{kT}\frac{\partial V}{\partial(\ln J)} \qquad (8)$$

In silicon, thermionic emission is typically the dominating mechanism for forward current flow (semiconductor-to-metal electron transport) and carrier generation-recombination also contributes to the reverse leakage current. For SiC Schottky contact, because of a ten times higher critical electric field, the likelihood of quantum-mechanical tunneling of the carriers through the potential barrier is much higher. At high reverse bias voltage, electron tunneling current can also contribute significantly to the reverse current of the contact.

2.2 Schottky barrier height of different metal contacts to SiC

Extensive work has been carried out in investigating the Schottky contact of different metals to the SiC [6-42]. As pointed out in the previous section, the behavior of the Schottky contact is dependent on the contacting metal, the poly type of SiC, surface condition as well as the interfacial chemistry.

Some basic material properties of the three main poly-types of SiC and Silicon are listed in table 1 and the work functions of some metals are shown in table 2.

Table 1 Material property comparison of Silicon and SiC with different poly-types

	Silicon	3C-SiC	6H-SiC	4H-SiC
Bandgap (eV)	1.1	2.3	2.9	3.3
Relative dielectric Constant	11.9	9.7	9.7	9.7
Breakdown field at (N_D=5e15cm^{-3}) (MV/cm)	0.3	1.5	2.2	2.3
Electron mobility (cm^2/V/s)	1350	900	370	800
Hole mobility (cm^2/V/s)	480	40	80	120
Saturated electron velocity (10^7cm/s)	1.0	2.0	2.0	2.0
Electron affinity (eV)	4.05	3.8	3.3	3.1

Table 2 Work functions of various metals being investigated for Schottky contact to SiC.

Metal	Mg	Mn	In	Ag	Al	Ti	Mo	Cu	Au	Pd	Ni	Pt
ϕ_M(ev)	3.65	4.15	4.20	4.25	4.28	4.33	4.6	4.65	5.1	5.12	5.15	5.65

The electron affinities of the 3C, 6H and 4H SiC (0001) are 3.8eV, 3.3eV and 3.1eV, respectively. As mentioned above, the Schottky barrier height will also be dependent on the work function of the metal. In table one, the work functions of various metals are shown. In the ideal contact case described by equation 1, as the metal work function increases, the barrier height for a certain SiC poly-type will increase with the same amount. In practice, the dependence of the barrier height on the metal work function is weaker, as can be seen in equation 4.

The barrier height of a specific Schottky contact can be extracted from either current-voltage curves or the capacitance-voltage curves.

For moderately doped semiconductors, according to the thermionic-emission theory [5], the current density (J) versus forward voltage (V) characteristics direction with V>3kT/q can be given by:

$$J = J_S\left[\exp\left(\frac{qV}{\eta kT}\right)-1\right],\ J_S = A^*T^2\exp\left[-\frac{q}{kT}(\phi_B-\Delta\phi_b)\right] \qquad (9)$$

where J_S is the saturation current density, η is the ideality factor, A* is effective Richardson's constant (for 4H-SiC 146Acm^{-2}K^{-2}) [43], ϕ_B is the barrier height, and $\Delta\phi_b$ is the image force lowering. From equation 9, the barrier height (ϕ_B) and the ideality factor (η) can be obtained.

$$\phi_B = \frac{kT}{q}\ln\left(\frac{A^*T^2}{J_S}\right),\ \eta = \frac{q}{kT}\left[\frac{\partial V}{\partial(\ln J)}\right] \qquad (10)$$

The Saturation current density (J_S), and the barrier height (ϕ_B) can be extracted in a plot of Ln*J* versus forward voltage V.

The ideality factor is a good indication of contribution different current mechanisms. As can be seen in equation 6, the thermionic emission current components has an ideality factor of 1 while that of the tunneling current component will be higher than 1. In practice, an ideality factor extracted to be very close to 1 is an indication that current is dominated by thermionic emission.

The barrier height can also be extracted from the C-V curves [5].

$$\phi_B = V_I + \frac{kT}{q}\ln\left(\frac{N_{DA}}{N_C}\right)+\frac{kT}{q}-\Delta\phi_b,\ N_{DA} = \frac{2}{q\varepsilon_S\left[-\frac{d(1/C^2)}{dV}\right]A^2} \qquad (11)$$

where N_C is the conduction band density of states for SiC (1.66e19cm^{-3} for 4H-SiC) [44], V_I is the intercepting voltage of the 1/C^2 versus voltage curve, as seen from figure 2, and A is the area of the diode. In addition to the two methods described above, the x-ray photoemission spectroscopy (XPS) can also be used to extract the barrier height.

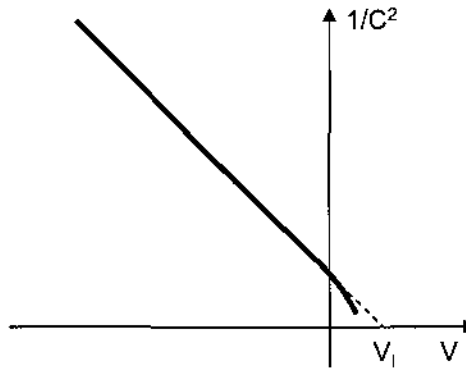


Fig. 2 Extraction of Schottky barrier height from the capacitance versus voltage curve, the intercepting voltage (V_I) is used in equation 11 for SBH calculation

A list of Schottky barrier height from n-type SiC Schottky contact studies reported in the literature for the recent years have been shown in table 3. Only the most commonly used 3C, 6H and 4H SiC poly-types are included. In the table, the SiC poly-type, the terminating surface layer of SiC, the contacting metal, its resultant barrier height extracted from the I-V and/or C-V method and the ideality factor

are shown. For the same SiC poly-type, the entries are listed with increasing metal work function. While the p-type SiC Schottky contacts are of less interest, there are also some reported works in the literature. Table 4 listed the SBH of these reported p-type Schottky contacts.

As explained in the previous paragraphs, the barrier height is dependent on various conditions and therefore does not simply increase with increasing metal work function, mainly due to the highly process dependent interface state density. Table 3 shows that, a fairly wide range of SBH (0.3eV to 2.0eV) can be achieved with different metals and processing conditions for the three SiC poly-types shown.

In the following paragraphs, SBH as a function of the influencing factors such as metallization choice, SiC poly-type, face polarity, surface treatment, post deposition annealing and SiC material doping will be discussed.

Table 3 Barrier height of n-type Schottky contact to different SiC poly-types for various metals (300K unless otherwise stated)

Poly-type	face	Metal	Barrier Height (eV)		Ideality Factor (η)	Comments	Refs
			I-V	C-V			
3C		Au		1.15			[45]
		Au		1.2	1.5		[46]
		Au	0.4-0.7		1.6-2.3		[28]
		Pt		0.95	1.5	Increase to 1.35eV after 800°C, 20min annealing	[47]
6H	Si-	Mg	0.34		1.22	Measured at 175K	[14]
		Mg	0.69		1.3		[18]
	Si-	Mn	0.79	0.96	1.05		[14]
		In	0.84		1.3		[18]
	C-	Ag	1.1	1.21	1.08		[14]
	Si-	Ag	0.83	0.97	1.07		[14]
	C-	Al	0.89	0.96	1.06		[14]
	Si-	Al	0.26		1.72	Measured at 150K	[14]
		Al	0.92		1.3		[18]
	C-	Al	0.25		1.6		[20]
	Si-	Al	0.25		1.6		[20]
		Ti	0.85	0.85	<1.1	$N=2\text{-}6e16cm^{-3}$	[15]
	C-	Ti	1.03	1.09	1.08		[48]
	Si-	Ti	0.73	0.75	1.05		[48]
		Ti		0.3	1.0	HF treatment + boiling water	[22]
		Ti/Pt		0.8			[49]
	C-	Mo	0.5		1.8		[20]
	Si-	Mo	0.3		1.6		[20]
		Mo		0.7	1.0	HF treatment + boiling water	[22]
	C-	Au	1.19	1.3	1.08		[14]
	Si-	Au	1.37	1.48	1.07		[14]
		Au	1.12		1.15		[50]

	C-	Pd	1.62	1.58	1.05		[14]
	Si-	Pd	1.11	1.26	1.09		[14]
		Pd	1.01		1.3		[18]
	C-	Ni	1.68	1.76	1.04		[48]
	Si-	Ni	1.29	1.29	1.03		[48]
	Si-	Ni	1.41				[21]
	C-	Ni	1.30				[21]
		Ni		1.19	1.0	HF treatment + boiling water	[22]
		Ni	1.39		1.02		[51]
		Pt	1.04	1.1			[52]
		Pt	1.05	1.05	<1.1	$N=2\text{-}6e16cm^{-3}$	[15]
		$NiSi_2$	0.40				[53]
4H	Si-	Ti	0.95	1.17	1.02~0.2		[23]
	C-	Ti	1.16	1.3	1.02~0.2		[23]
	Si-	Ti	0.8		1.15	I-V, As deposited, measured 20°C	[54]
	Si-	Ti	0.85		1.1	I-V, measured 122°C	[54]
		Ti/Au/Pt/Ti	1.17		1.09		[55]
		Ti	1.17		1.06		[56]
	Si-	TiW	1.22	1.23	1.05	As deposited	[57]
		TiW	1.18	1.19	1.1	500°C, 30min	[57]
		Ni_2Si	1.4		<1.1	After defect-removal treatments	[38]
		Cu	1.6		<1.1	As deposited	[58]
		Cu	1.8		<1.1	After 500°C, 5min	[58]
	Si-	Au	1.73	1.85	1.02~0.2		[23]
	C-	Au	1.8	2.1	1.02~0.2		[23]
		Au		1.59			[59]
	Si-	Ni	1.62	1.75	1.02~0.2		[23]
	C-	Ni	1.6	1.9	1.02~0.2		[23]
		Ni		1.67			[60]
		Ni		1.64			[61]
	Si-	Ni	1.3		1.21	I-V, measured 20°C	[54]
	Si-	Ni	1.4		1.12	I-V, measured 122°C	[54]
	Si-	Ni	1.5		1.12	I-V, measured 255°C	[54]
	Si-	Ni	1.59		1.05		[63]
		Ni	1.35		1.05		[63]
		Ni		1.7	1.07		[64]
		Ni	1.63		1.1		[65]
		Ni		1.63			[66]
	Si-	Pt	1.39		1.01		[63]

Table 4 Barrier height of p-type Schottky contact to different SiC poly-types for various metals (300K unless otherwise stated)

	face	Metal	Barrier Height (eV)		Ideality Factor (η)	Comments	Refs
			I-V	C-V			
3C		Au	1.12	1.11		1~5e16cm^{-3}	[67]
6H		Ti/Al		1.95		5e16cm^{-3}	[25]
		Al	1.23	2.87	2.18	2~9e15cm^{-3}	[37]
		Mo	1.6				[19]
		Cu	1.22	1.39	1.01	2~9e15cm^{-3}	[37]
		Au	1.18	1.45	1.51	2~9e15cm^{-3}	[37]
4H		Ti/Al		1.5		1e16	[25]
		Ti	1.94	2.07	1.07	1.2e16	[35]
		Au	1.35	1.49	1.08	1.2e16	[35]
		Au	1.57				[19]
		Ni	1.31	1.56	1.29	1.2e16	[35]
		Ni	1.43		1.29	3e15	[68]

As shown in figure 1, the energy band structure of the SiC is very important in determining the nature of Schottky contact. For SiC, the energy bandgap value increases with the degree of hexagonality in the polytype. Among the three poly-type listed, 3C-SiC (pure cubic structure) has the narrowest and 4H-SiC (4H has 50% hexagonality and 6H has 33.3% haxagonality) has the widest bandgap [69].

While limited reports are available for 3C-SiC Schottky contact, it is still observable from the table that, for the same metal, the poly-type with a wider bandgap and hence lower electron affinity (i.e., 4H-SiC) has a higher SBH than that for the poly-type with narrower bandgap (3C-SiC). For Au, the barrier height is ~1.15eV, ~1.4eV and ~1.8eV for 3C, 6H and 4H SiC, respectively. Similar trend can be seen for Pt. This agrees with the analysis provided above and with equation 4.

In addition to the poly-type bandgap dependence, it has been established previously that the SBH is also dependent on the interface state density which in turn depends heavily on the poly-type and the process conditions for surface treatments. In an attempt to quantify the degree of dependence of the interface state density on SiC poly-type, Jacob and coworkers [70] performed a detailed analysis of the interface slope parameters for various metallization on 6H and 3C-SiC. The interface slope parameter is defined as $S=d\phi_B/d\phi_M$ or $S=d\phi_B/d\chi_M$, depending on whether the work function $d\phi_M$ or electronegativity χ_M of the metal is used. For most Schottky contacts under investigation with doping <1e18cm^{-3}, the interface slope parameter S is almost the same as parameter c_2 in equation 4 [5]. Plots of the n-type contact SBH versus different metal work functions of 6H and 4H-SiC are shown in figure 3. While the SBH of different reports can vary in a wide range, there is a general trend of an increasing SBH with increasing metal work function. A few observations can be made from figure 3. Firstly, SBH of the Schottky contact is dependent on the SiC surface polarity, i.e., C-face of Si-face. It can be clearly seen that SBH of the same metal is significantly higher when making contact to a C-face SiC when compared to Si-face SiC. This dependence of SiC SBH on the SiC surface polarity was extensively investigated in [14, 48, 71, 72]. Secondly, the SBH data extracted from measurement is also slightly dependent on the extraction methods. The SBH extracted with the C-V method is generally higher than that extracted with the I-V method by 0.05~0.15eV. Thirdly, the SBH is generally higher for 4H-SiC than for 6H-

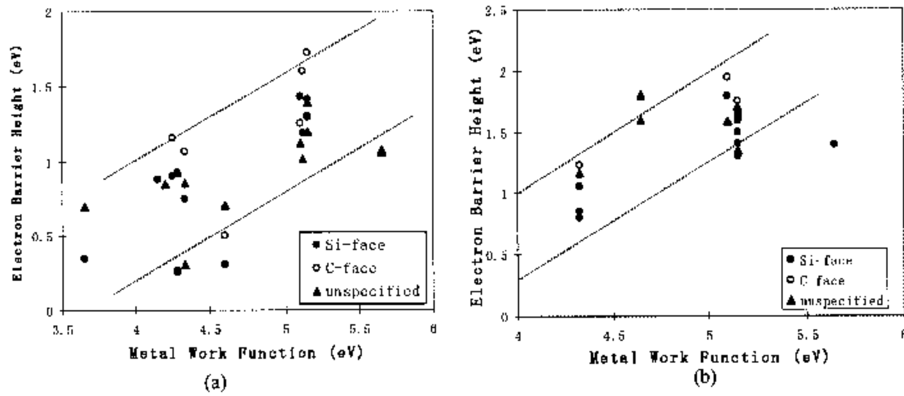


Fig. 3 The dependence of n-type Schottky barrier height on metal work functions, (a), 6H-SiC and (b), 4H-SiC. Solid circle: Si-face, open circle: C-face, solid triangle: unspecified. Both poly-types has similar interface slope parameters.

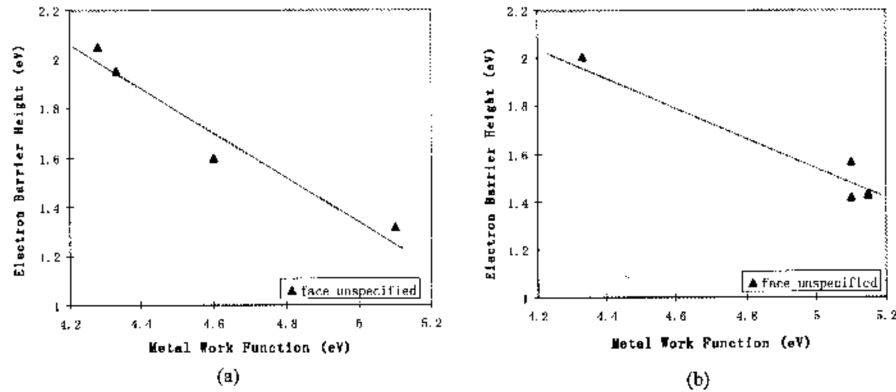


Fig. 4 The dependence of p-type Schottky barrier height on metal work functions, (a), 6H-SiC and (b), 4H-SiC. The limited data show that 4H-SiC has more severe interface Fermi-level pinning

SiC, as explained previously. Lastly, due to the interface state density, the overall interface slope parameter shown in figure 3 is found to be around 0.6 for 6H-SiC and 0.9 for 4H-SiC, indicating a stronger Fermi-level pinning for 6H-SiC. The interface state density was estimated to be in the range of 10^{13}~$10^{14}cm^{-2}eV^{-1}$ for 6H-SiC [73].

A similar plot for p-type SiC Schottky contact can be seen in figure 4. The interface slope parameter S can be extracted to be around 0.85 for 6H-SiC and 0.65 for 4H-SiC.

The Schottky contact interface property is strongly influenced by the surface condition prior to metal deposition as well as the post deposition annealing. Therefore, contaminations and interfacial oxide layers before metal deposition can significantly alter the SBH as well as junction electrical characteristics. This can be seen from the variation in SBH for the same metal for a specific SiC material.

There have been reports on surface treatment methods that will allow the Fermi-level to be un-pinned, i.e., virtually eliminates the interface state density. It has been reported in [22] that by a sequence of sacrificial oxidation, 5% HF etching and dipping into boiling water for 10min, the surface interface states can be reduced drastically. As a result, the contact approaches the ideal Schottky contact described in Fig. 1.a and the interface slope parameter (S or C_2 in equation 4) can approach unity. Plots of SBH versus metal work functions are shown in Fig. 5. Another report [38] reported that by annealing the Ni-SiC Schottky contact at 600-800°C in N_2 ambient, a layer of Ni_2Si will be formed, which consumes a layer of SiC on the surface and hence eliminates the material damage caused by preceding process steps. This gives rise to a silicide-SiC interface that is relatively independent of surface treatment and obtain a reproducible, close-to-ideal Schottky contact.

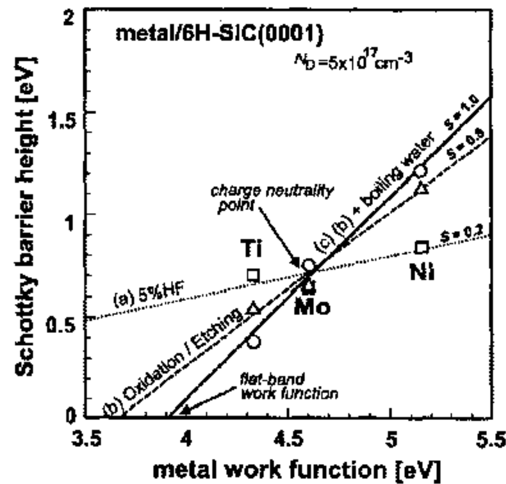


Fig. 5 Schottky barrier heights as a function of metal work functions. No treatment (short dashed line), oxidation followed by HF etching treatment (long dashed line), and dipping treatment in boiling water (straight line) are indicated. [22]

Schottky interface property is also strongly influenced by the post deposition annealing process. With high temperature annealing, chemical reaction takes place on the interface of SiC and the Schottky metal. A silicide can develop on the interface and hence change the band diagram and hence the barrier height of the whole contact. It was reported that the SBH Pt Schottky contact on 6H-SiC will increase significantly after post deposition annealing at temperatures of 600°C and above [47, 15, 74]. As shown in figure 6, SBH of the Pt-SiC contact increased from 0.45eV to 1.35eV after annealing at 900°C. This was attributed to the formation of Platinum silicide at temperatures above 600°C, which forms a contact with higher Schottky barrier with 6H-SiC. Dependent on the metal and hence the silicide formed, post deposition annealing can also cause a barrier height to decrease [75]. Similarly, the SBH of a Ni contact to SiC with Si-face polarity is also found to decrease with the substrate temperature during metal sputtering [21].

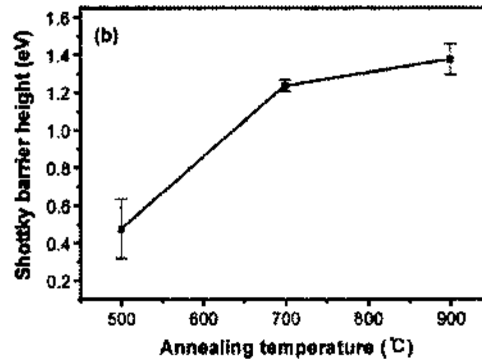
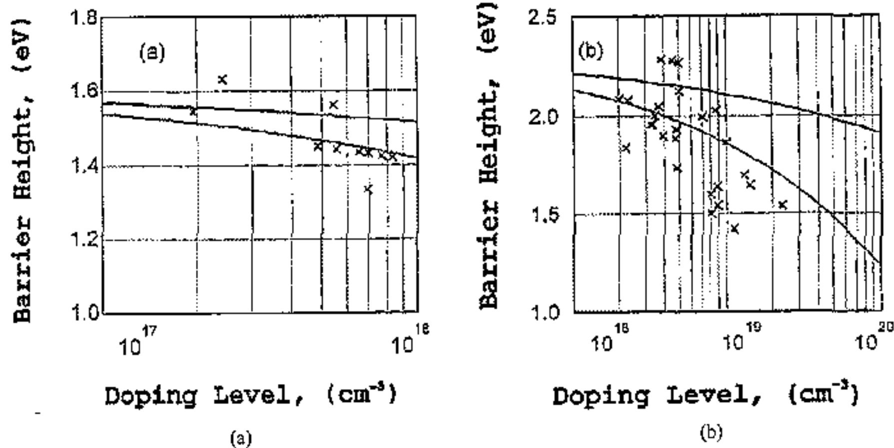


Fig. 6 Variation of Pt-SiC Schottky barrier height (SBH) as a function of annealing temperature [74]

In [21], Ni barrier height is



(a) (b)

Fig. 7 4H-SiC Schottky barrier heights against doping for (a), Au-n-4H-SiC contacts and (b), Au-p-4H-SiC contact. (symbol: experimental, top line: calculation according to image force barrier lowering and bottom line: calculation including total charge balance at the surface according to equation 4). [19]

found to decrease with substrate temperature before metal sputtering for Si-face but increase for C-face 6H-SiC.

The SBH is also found to be dependent on the doping of the semiconductor for relatively highly doped materials. As shown in figure 7, the SBH tends to decrease as the donor concentration increases above the 2e17cm^{-3} level and the acceptor concentration increases above 1e18cm^{-3}. The barrier reduction is more significant than that caused by the image force lowering effect, as evident from figure 7. A calculation based on equation 4 taking into account the total surface charge balance gives a reasonable fit to the experimental data.

There have been some reports on the temperature dependence of the SBH [16, 76, 77, 78]. It was reported in [76] that, as the temperature increases, both the conduction band and valence band move downward relative to the semiconductor Fermi-level. As a results, the n-type SBH decreases and the p-type SBH increases with increasing temperature. Variation of the intercepting voltage of the $1/C^2$ versus voltage curve (V_I in equation 11, also named as the diffusion potential) against temperature for Ag contacts on n-type 6H-SiC is plotted in figure 8. A clear reduction in V_I, and hence the SBH can be seen. On the other hand, the SBH of a p-type contact on 6H-SiC demonstrated positive

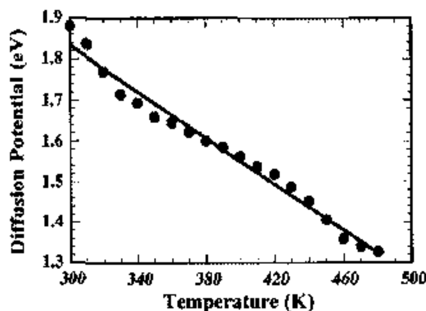


Fig. 8 Variation of the diffusion potential (V_I) against temperature for Ag contacts on n-type 6H-SiC [76]

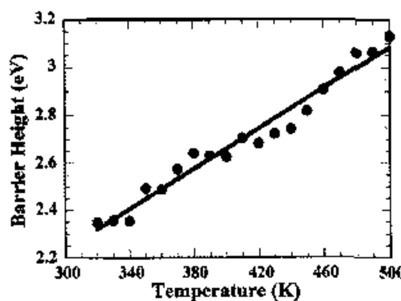


Fig. 9 Schottky barrier height of Al contacts on p-type 6H-SiC. A substantial increase with temperature is observed [76]

temperature coefficient, indicating a shift of valence band away from the Fermi-level as temperature increases. The rate of change against temperature was found to be significantly higher for the p-type contacts when compared to the n-type contacts. While the bandgap is expected to narrow as temperature increases, which will lead to n-type SBH reduction, the magnitude of variation on the SBH reported is 10 to 20 times higher than that predicted by the bandgap narrowing. For Ag contacts on n-type 6H-SiC, temperature coefficient of the intercepting voltage (V_I) is 2.8meV/K. This V_I temperature coefficient was also found to be dependent on the electronegativity of type of metal being used. A metal with higher electronegativity will give a stronger SBH dependence on temperature.

Electronegativity describes the ability of an atom to attract an electron to itself in a molecule. As the temperature of a metal-semiconductor contact is increased, more carriers are freed in semiconductor. The Fermi level moves toward midgap. The barrier created at the interface initially separated carriers to achieve charge neutrality; as the temperature is increased, excess carriers will be drawn into the metal in order to maintain this charge neutrality at the interface and hence lowering the barrier height. The better the metal's ability of attracting these carriers, the more barrier lowering occurs.

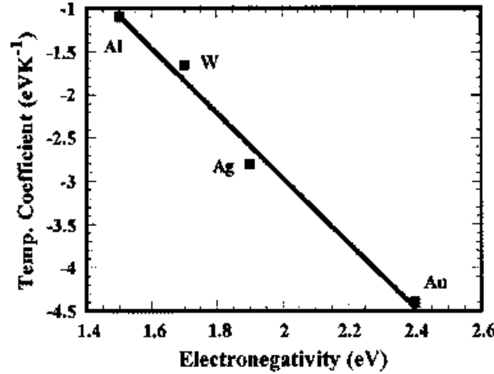


Fig. 10 Schottky barrier height temperature coefficient (in *meVK^{-1}*) versus electronegativity for different metals [76]

The temperature coefficients of the intercepting voltage (V_I) for n-type 6H SiC contacts of four different metals are plotted in figure 10 against their electronegativity and a linear relation can be observed [76]. For metals with low electronegativity such as Al and Ti, the temperature coefficient of the intercepting voltage (V_I) and hence the Schottky barrier height is small and insignificant.

A similar SBH reduction with increasing temperature was also reported in [77]. No clear physical mechanism was suggested to account for the magnitude of SBH change. It is also recognized in [16, 78] that the temperature dependence of the SBH become significantly weaker at temperatures less than 300K.

3. High Voltage SiC SBD, JBS and MPS diodes

For high power applications, it is well known that the specific on-resistance (defined as product of device resistance and active device area) of unipolar semiconductor device is a function of both the doping and thickness of the voltage-blocking layer (commonly referred to as the drift layer). Such specific on-resistance is limited by the following equation [79]:

$$R_{sp,on} = \frac{t_{dr}}{q\mu N_D} = \frac{4V_B^2}{\mu\varepsilon_S E_C^3} \tag{12}$$

Due to its superior electrical material property, SiC as a semiconductor material has a unique advantage in high power and high temperature applications. According to equation 12, when compared to silicon, the roughly ten times higher critical electric field of SiC (4H) material will give approximately three orders of magnitude improvement over the specific on-resistance for a given blocking voltage requirement. For this reason, extensive amount of effort has been invested in demonstrating and commercializing SiC unipolar device for power applications. Schottky Barrier Diode (SBD) is the simplest unipolar device to fabricate and hence has been the first SiC power device commercialized. SiC SBD also has its unique advantage over SiC P-i-N diodes because of the high build-in voltage of the latter.

In this section, the development of SiC SBD will be discussed together with a few close variants such as SiC Junction Barrier Schottky (JBS) diode, Mergied P-i-N Schottky (MPS) diode, Dual Metal Trench (DMT) diode and Trench MOS Barrier Schottky (TMBS) diode. Termination techniques used to achieve a high blocking voltage; device structures used to minimize reverse leakage current; design approaches taken to obtain low on-state voltage/resistance and device performance under different temperatures will be discussed.

3.1 SiC SBD development

One of the earliest high voltage SBD was fabricated in 1975 [6] on 6H-SiC with an avalanche breakdown voltage of around 200V. More SiC devices were fabricated as high quality SiC become available in early 1990s and both the voltage and current capabilities of these SiC SBDs increases quickly in the years followed [54, 64, 66, 80-94]. Recently, a 4H-SiC SBD with a breakdown voltage of 10.8kV was reported with a specific on-resistance of $187m\Omega cm^2$ [2].

In table 5, some of the SBD reported in the literature is listed. They represent one of the highest voltage or current capability of SiC SBD at the time of the report. The progressive increase of voltage and current rating of SiC SBD can be clearly seen in the table. SiC SBDs with breakdown voltage of close to 1000V was first reported in [80] on 10μm, $1\times10^{16}cm^{-3}$ Nitrogen doped 6H-SiC by using Pd in 1993. In mid-1990, as 4H-SiC material become available, it attracted most interests for SiC SBDs from 6H-SiC. This is because of its higher electron mobility and critical electric field resulted from its wider bandgap. 4H-SiC SBDs up to 1000 V were reported using a drift layer of 10μm, $1\times10^{16}cm^{-3}$ Nitrogen doped 4H-SiC in 1995 [82]. The 1000-V 4H-SiC SBDs were later reported by using higher barrier metals of Ni and Pt, again based on a 10μm thick drift layer doped in the range of cm to cm in 1998 with improved current density [26, 54]. Breakdown voltage of 4H-SiC SBD reached 2.5kV in 1998 and 4kV in 1999. In 2002, SiC SBD with a breakdown voltage of 4.9kV was demonstrated on $7e17cm^{-3}$ doped, 100μm thick 4H-SiC [94]. In the same paper, a 1.7kV, $0.64cm^2$, 130A SBD was also reported

Table 5 High voltage Schottky barrier diodes reported in the literature. Work listed here has one of the highest voltage or current at the time when the work was reported. (300K unless otherwise stated)

Poly-type	Device	Metal	V_{br} (V)	V_F(V) /$R_{sp,on}$ (Ωcm^2)	year	Comments	Ref

6H	SBD	Pt	205		1975	1e16cm^{-3},	[6]
6H	SBD	Pt	400	1.1V	1992	3.6e16cm^{-3}, 100A/cm^2	[95]
6H	SBD	Ti	500	1.1V	1992	2-6e16cm^{-3}, 100A/cm^2	[15]
6H	SBD	Pd	1000		1993	1e16cm^{-3}, 10μm	[80]
6H	SBD	Au	1100	8e-3	1993	5.8e15cm^{-3}, 9.6μm	[81]
6H	SBD	Ti	1000		1994	2e16cm^{-3}, 10μm, argon impl.	[96]
4H	SBD	Au	800	1.4e-3	1995	5e15cm^{-3}, 10μm	[83]
6H	SBD	AlTi	600		1995	1.3e16cm^{-3}, 4.7μm, guard ring	[97]
4H	SBD	Ti	1000	2e-3	1995	1e16cm^{-3}, 10μm	[82]
4H	SBD		1750	5e-3	1995	7e15cm^{-3}	[98]
4H	SBD	Ti	1100		1996	0.7~2e16cm^{-3}, 10μm, B^+ impl.	[99]
4H	SBD	Ti	1300		1996	8e15cm^{-3}, 10μm, argon impl.	[100]
4H	SBD		1400	1.5e-3	1996	1e16cm^{-3}, 10μm	[84]
4H	SBD		>1000		1998	Large area, 7mm^2, 30A/pulse	[101]
4H	SBD		2500		1998		[86]
4H	SBD	Ti	600	7e-2	1998	1e16 cm^{-3}, 2μm, P-type	[25]
4H	SBD	Ni	3000	3.4e-2	1998	0.7~2e15cm^{-3}, 42~47μm	[61]
4H	SBD		4000		1999		[93]
4H	SBD		3850		2000		[66]
4H	SBD		1700		2001	Large area, 25A	[102]
4H	SBD		1700		2002	5e15cm^{-3}, 15μm, 0.64cm^2, 130A	[94]
4H	SBD		4900	1.7e-2	2002	7e14cm^{-3}, 100μm, B^+ impl.	[94]
4H	SBD		10800	1.87e-1	2003	5.6e14cm^{-3}, 115μm, MJTE	[2]

The increase of SiC SBD breakdown voltage from the beginning of the 1990s is plotted in figure 11. SiC SBD with the highest breakdown voltage reported so far was reported with a 5.6e14cm^{-3} doped, 115μm thick drift region on 4H-SiC [2]. While further improvements on the SiC SBD breakdown voltage are still possible, the rapidly increasing specific on-resistance at higher voltages makes unipolar devices like SBD less attractive.

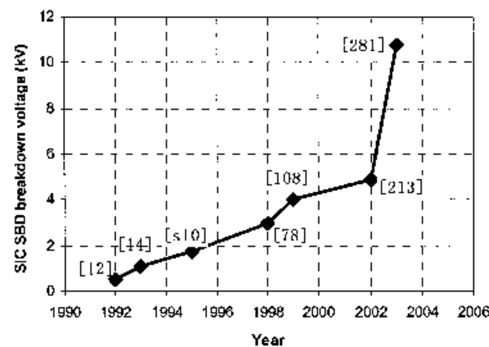


Fig. 11 The increase of SiC SBD breakdown voltage since 1992

3.2 Termination techniques

With appropriately selected drift region and thickness, the most important factor in achieving a high blocking voltage for SiC SBD is the edge termination technique used to reduce electric field crowding at the periphery of the power device. Many works were reported on edge termination of SiC SBD to achieve high breakdown voltages [2, 15, 51, 63, 95-100, 103-119].

Several techniques of edge terminations have been used to reduce the electric field crowding and to achieve a breakdown voltage close to the ideal parallel-plane avalanche breakdown voltage. These techniques include floating metal rings, metal field plating, argon/B^+ implantation termination, RESURF assisted field plate, and modified field plate and multi-step junction termination extension (MJTE), etc.

The schematic structures of these termination techniques are plotted in figure 12.

Floating metal ring method (Fig. 12.a) was used in [103] on 6H-SiC SBDs. A breakdown voltage of 600V was obtained with three rings. Similar approach was used in [114, 115] with multiple implanted P^+ and V^+ (Vanadium ion) regions as floating guard rings. Breakdown voltages of 1300V and 1630V were achieved on 4H-SiC wafers with drift regions of 10μm, 5e15cm^{-3} and 10μm, 1e16cm^{-3}, respectively. A p-epi guard ring termination approach was taken in [104, 97] on 6H-SiC where 600V was achieved. The shape of the p-epi (Fig. 12.b) was created by using a field oxidation process. It also gives rise to a smooth metal step over the p-epi, avoiding field crowding at the corner. In [108], a field plating techniques was proposed and demonstrated in [51] on a ramped oxide (Fig. 12.d) to achieve a device breakdown voltage (800V) close to its ideal value. However, it was suggested in [119] that the method is only efficient at relatively low voltage and could also give rise to electric field crowding in the passivation oxide at the edge of the field plate, raising concern of oxide reliability at high temperatures. The method of implanting a high dose of argon into the surface of the SiC area at the periphery of the device has been used and voltages close to ideal breakdown were also achieved [95, 15, 103, 96, 84]. By implanting a high dose of inert specie into SiC, the exposed SiC will be damaged and turn into a high resistive region, which effectively reduces the field crowding at the device periphery (Fig. 12.c). The method was proven to be effective at voltage levels like 1kV [96] and 1.4kV [84] but was not verified for higher voltages. An approach was used in [98] by similarly implanting B^+ to the device periphery and achieved a blocking voltage of 1.75kV. In [117], a method combining the floating guard ring and the RESURF effect was adopted (Fig. 12.e) and found to be able to achieve a good breakdown voltage (~1.2kV) for a wide range of implantation doses. On the other hand, the multi-step JTE (MJTE) approach was used in [116] and [2], achieving breakdown voltages of 1kV and 10.8kV, respectively. The MJTE structure shown in Fig. 12.f uses the multiple p-extension zones to gradually reduce the electric field toward the edge of the SBD. Each step can be obtained through inductively coupled plasma (ICP) etching which can provide very accurate etching control. It was demonstrated that close to ideal breakdown voltage can be achieved for both very high and medium voltage devices.

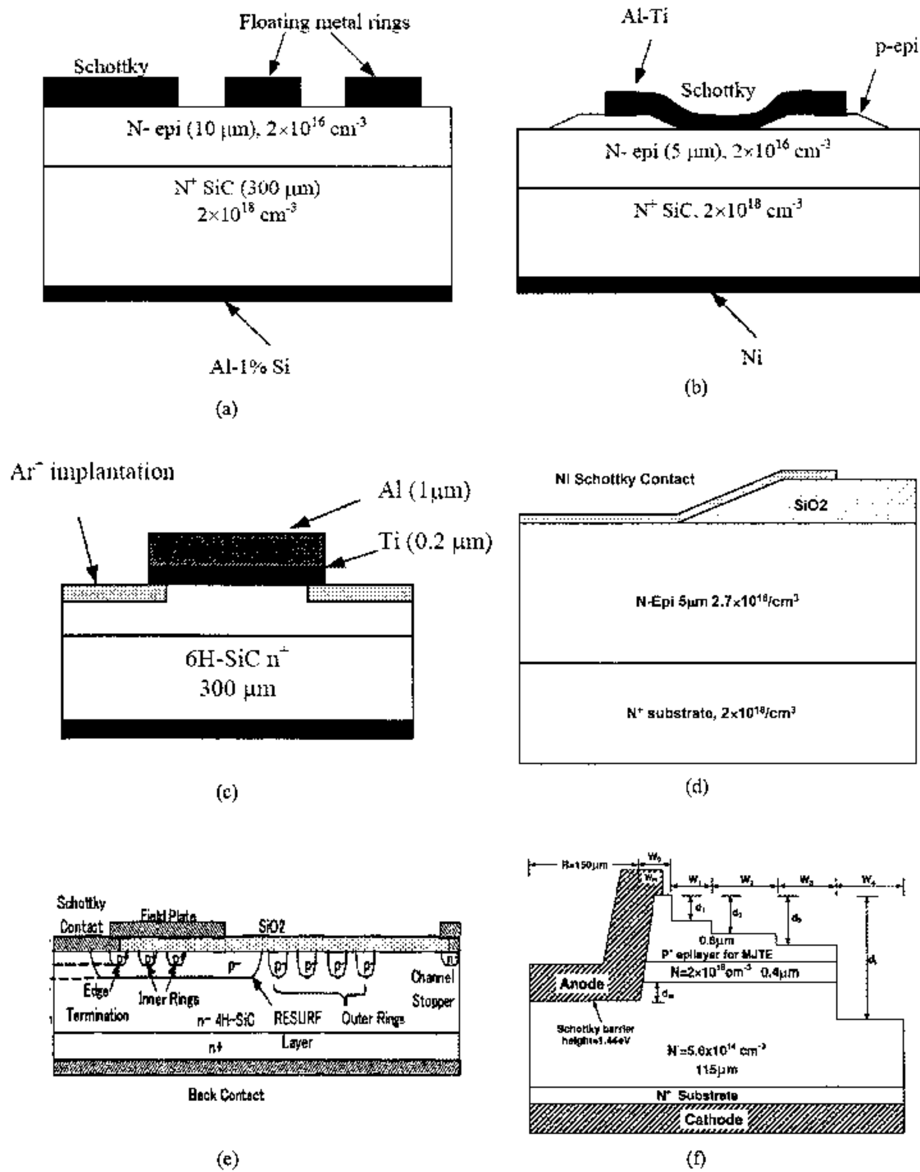


Fig. 12 Various termination techniques used for high voltage SiC SBDs. (a), floating metal rings, (b), p-epi guard rings, (c), argon implantation, (d), ramped oxide field plating, (e), guard ring assisted RESURF and (f), multi-step JTE [2, 92, 117].

3.3 Reverse leakage current

Reverse leakage current is an important parameter for a diode used in power electronics systems. When blocking reverse voltage, a high leakage current can cause significantly amount of heat dissipation. Because the reverse leakage current of a SBD is typically very sensitive to the junction temperature, if the leakage-current-caused heat dissipation reaches certain level, the resultant temperature increase can initiate a positive feedback in the thermal system and a thermal run-away will take place. The damage caused by a thermal run-away is normally permanent. Therefore, minimizing the reverse leakage current is always an important consideration for the device designers.

Two components out of the four listed in section 2.1 will contribute significantly to the reverse leakage current of a SiC SBD. The first is the thermionic emission current which is the dominating component for SBDs on silicon. The thermionic emission current can be calculated according to equation 6. It is worth noting that as the reverse bias voltage increase, the image force lowering effect described in equation 5 will continuously decrease the Schottky barrier (ϕ_B) and hence cause the reverse leakage current to increase. For a one-dimensional Schottky junction, the surface electric field (E_m) in equation 5 can be written as:

$$E_m = \sqrt{\frac{2q\mathrm{N_D}}{\varepsilon_S}(V_R + V_{bi})} \qquad (13)$$

where V_R is the reverse bias voltage and V_{bi} is the built-in voltage for the Schottky junction. The amount of Schottky barrier lowering resulted from the increasing reverse bias voltage can be calculated as shown in figure 13. Because of the exponential dependence of the reverse leakage current on the Schottky barrier height, the barrier lowering can have significant effect on the increase of leakage current with increasing reverse bias voltage.

The second component that will also contribute to the reverse leakage will be the tunneling current. Because of the wide bandgap and hence high critical electric field of the SiC material, as the reverse bias voltage of the diode increases, the Schottky junction can experience electric field as high as >2MV/cm. This can contribute to the reverse leakage significantly.

Figure 14 shows the reverse leakage of the 10.8kV 4H-SiC SBD in [2], which can

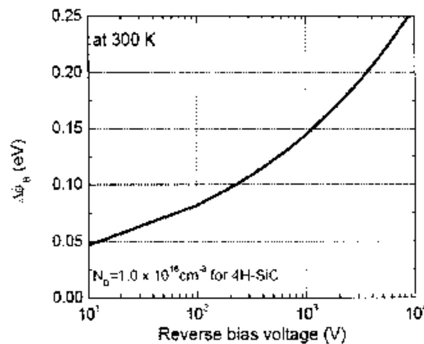


Fig. 13 Calculated Schottky barrier height reduction at room temperature due to the image force lowering versus reverse bias voltage [92].

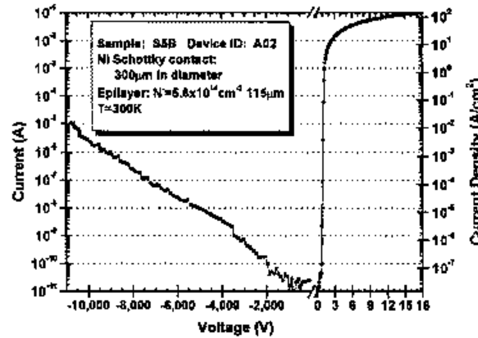


Fig. 14 Reverse and forward I-V and J-V curves for the 10.8kV Schottky barrier diode, after [2]

be seen to increase over almost six orders of magnitude. Although the device has not reached avalanche, measurement of the device was stopped at 10.8kV because of the concerns on the device self-heating. It is common for SiC SBDs that the avalanche breakdown can not be safely measured because of the excessive reverse leakage current at high reverse blocking voltage, prompting serious self-heating problems.

Barrier height inhomogeneous has also been investigated as a possible reason of a much larger reverse leakage current than predicted by the thermionic emission current in the SiC SBD [120-123]. It was suggested in [120] that there are localized regions at the SiC/metal interface where Schottky barrier height is lowered due to the presence of epitaxial layer defects at the interface. Material inhomogeneous has also been suggested as possible causes.

3.3.2 Hybrid structures for leakage current reduction

In order to reduce the amount of reverse leakage current of SiC SBDs, various methods have been proposed through the years [116, 124-141]. These include the Junction Barrier Schottky (JBS) diode, Mergied P-i-N Schottky (MPS) diode, Dual Metal Trench Schottky (DMTS) diode, Dual Metal Planar (DMP) diode, Trench MOS Barrier Schottky (TMBS) diode.

In Table 6, various structures reported to reduce the reverse leakage current and increase on-off current ratio of the SBD are listed through recently years.

Table 6 High voltage JBS/MPS/DMT/TMBS diodes reported in the literature. (300K unless otherwise stated)

Poly-type	Device	Metal	V_{br} (V)	V_F(V) / $R_{sp,on}$ (Ωcm^2)	year	Comments	Ref
4H	DMTS		300	tbd	1998	3e15cm^{-3}, 13μm, 2μm deep trench	[124]
4H	JBS		tbd	tbd	1998	Tbd, ICSCRM proceedings	[136]
4H	JBS		Tbd	Tbd	1998	Tbd ICSCRM proceedings	[137]
4H	JBS		Tbd	Tbd	1999	Tbd ICSCRM proceedings	[138]
4H	JBS		Tbd	Tbd	2000	Tbd ICSCRM proceedings	[139]
4H	JBS		Tbd	tbd	2000	Tbd ICSCRM proceedings	[140]
4H	JBS		Tbd	Tbd	2000	Tbd ICSCRM proceedings	[141]
4H	MPS		800	Tbd	2001	140A	[135]
4H	JBS		>1000	Tbd	2001	9.7e15cm^{-3}, 13μm	[116]
4H	DMP		1250	Tbd	2002		[129]
4H	JBS		1500	Tbd	2002	6.4e15cm^{-3}, 10.5μm	[130]
4H	JBS		3000	Tbd	2002	1.5~3.0e15cm^{-3}, 30μm	[131]

The structures of these various structures are plotted in figure 15.

The common idea behind the JBS, MPS, DMTS and TMBS structures is to protect the Schottky barrier from high electric field when the device is blocking reverse voltage. Both the image force lowering and electron tunneling effects mentioned above are caused by an increasingly high electric field on the Schottky contact as reverse bias voltage increases. As can be seen in figure 15, JBS and MPS basically have the same structure

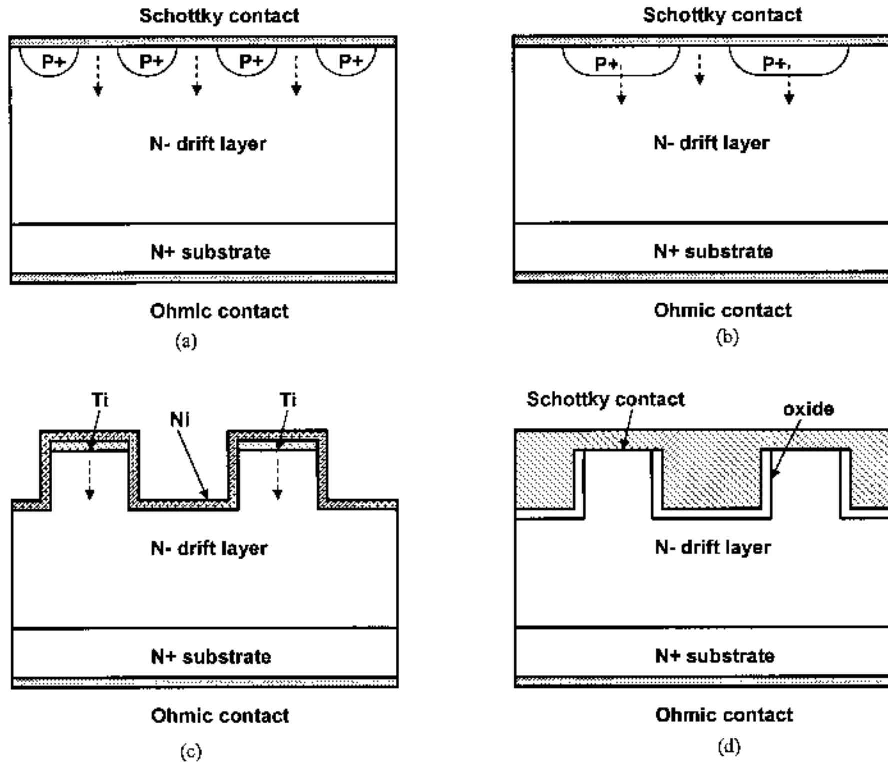


Fig. 15 Hybrid diode structures based on Schottky contact, (a), Junction Barrier Schottky (JBS) diode, (b), Merged P-i-N Schottky (MPS) diode, (c), Dual Metal Trench Schottky (DMTS) diode and Trench MOS Barrier Schottky (TMBS) diode. All structure utilize the common principle of electric field shielding to reduce the field at the Schottky contacts.

except that the P^+ regions of these two devices are designed differently. In both structures, the P^+ regions are closely spaced so that when the device block reverse voltage, the depletion regions of two adjacent intruding P^+ regions overlap each other and shield the Schottky contact area between them from high electric field [79]. However, in the JBS, depth, width and spacing of the P^+ regions are designed such at the P^+-n junctions will not be forward biased in under normal operating conditions of the device. P^+ regions of the MPS, on the other hand, are designed differently so that when the device forward current density is high enough, the P^+-N junction can be forward biased, injecting minority carriers into the drift region and reduce the device forward conduction voltage drop. In order to forward bias the MPS P^--n junctions, the voltage difference across the junction, which is caused by lateral current flow under the P+ regions, need to be close to the junction build-in potential. Because of the significantly higher build-in potential of SiC P^+-n junction, it will take a higher current density than its silicon counterpart to turn these junctions on.

The principle of electric field shielding also applies to the DMTS and TMBS diodes. In the DMTS, closely located trenches are filled with metals with higher barrier heights while for TMBS, similar trenches are oxidized before they are filled with metals. In both

cases, the trenches play the role of protecting the Schottky contact in between from high electric field, and hence reducing diode reverse leakage current.

Similar principle was proposed for a lateral SiC Schottky based diode named Lateral Merged Double Schottky (LMDS) diode in [128].

On the other hand, the dual metal planar (DMP) structure works with a different principle [129]. It was suggested that reverse leakage current of a SiC SBD is mainly attributed by those at the edge of the device because of the higher electric field there caused by imperfect field termination. The DMP diode was therefore proposed whereby a second Schottky metal with higher SBH is deposited at the periphery of the min Schottky metal. Since the reverse leakage current of a Schottky contact depends exponentially on the SBH, the higher SBH of the second metal drastically reduces the reverse leakage current at the device edge where electric field are the highest. The majority of active device area are still covered by the main Schottky contact metal with a lower SBH, ensuring a low forward voltage drop. In contrast to the four other structure discussed above, the DMP diode structure remains planar and no region protrusion occurs.

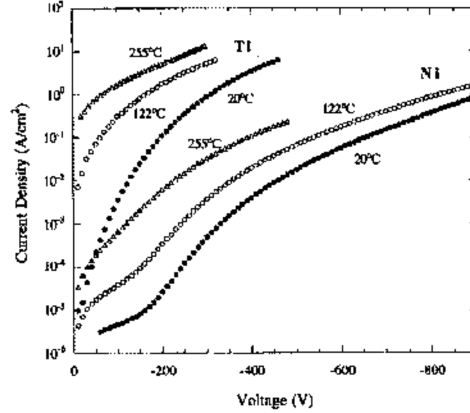


Fig. 16 Dependence of reverse leakage current density on temperature for Ti and Ni Schottky barrier diode on 1.6e16cm^{-3} doped 10μm thick n-type Si-face 4H-SiC [54]

3.3.3 Temperature dependence of reverse leakage current

The two major leakage current components representing the thermionic emission and tunneling currents are given by equations 6 and 7, respectively. It can be seen that both are highly sensitive to temperature. Figure 16 shows the reverse leakage currents density of Ti and Ni Schottky barrier diode on 1.6e16cm^{-3} doped 10μm thick n-type Si-face 4H-SiC at temperatures of 20°C, 122°C and 255°C. It is clear that the leakage current increases quickly with increasing temperature and decreasing Schottky barrier height, which agrees well with equations 6 and 7. The figure also shows a stronger dependence on temperature at lower voltage when compared to the higher voltage portion of the I-V curves.

3.4 Forward voltage drop

3.4.1 Forward voltage drop optimization

The forward voltage drop of a SiC diode with Schottky contact can be written as following.

$$V_F = \frac{\eta kT}{q}\ln\left(\frac{J_F}{A^*T^2}\right) + \eta\phi_B + R_{sp,on}J_F \tag{14}$$

$$V_F = V_{SB} + I_F(R_{sp,on} / A + R_{contact}) \quad (15)$$

While for n-type Schottky diode, the contact resistance can be generally neglected. An important parameter for a SBD is therefore its specific on-resistance. A lower specific on-resistance is desirable since a smaller chip size will be needed to handle a given amount of current. The specific on-resistance is normally calculated as the differential resistance of the SBD forward J-V curve and its components comprises the resistance of the electrodes, the back-side ohmic contact, the substrate and the drift region. For high voltage n-type SiC SBD, electrode, ohmic contact and substrate resistances are typically negligible and the drift region resistance is the dominating factor.

Optimizing the drift region resistance is therefore critical in minimizing the forward voltage drop of a high voltage SiC SBD. Two critical parameters, namely the doping and thickness of the drift layer, determine both the voltage blocking capability and the specific on-resistance of the device. There is a clear trade-off between these two targeting performance parameters. While high voltage blocking capability requires a thick and lightly doped drift layer, a low specific on-resistance demands exactly the opposite. Detailed analysis can be found in [79] on this trade-off. Usually, the targeted blocking voltage rating and the effectiveness of the edge termination employed determines the minimum thickness and the maximum doping used for the design of drift layer properties. The specific on-resistance of the drift layer used for an n-type SiC SBD can be written as:

$$R_{drift} = \frac{W_D}{q\mu_n N_D} \quad (16)$$

where W_D is the drift layer thickness, N_D is the drift layer doping, q is the electronic charge and μ_n is the electron mobility which is itself dependent on N_D. A non-punch-through (NPT) design of the drift layer corresponds to the case where drift layer thickness is equal or larger than the parallel plane avalanche breakdown width. Similarly, a punch-through (PT) design corresponds to a drift layer thinner than the parallel plane avalanche breakdown width. Design rules on the doping and thickness of the drift layer for NPT structures have been explained in [79]. However, it has been demonstrated that an optimized PT design can give a minimum specific drift layer resistance for a given targeting breakdown voltage [94].

For a punch through structure, the drift region thickness can be derived as:

$$W_D = \frac{\varepsilon E_C}{qN_D} - \sqrt{\left[\frac{\varepsilon E_C}{qN_D}\right]^2 - \left[\frac{2\varepsilon V_B}{qN_D}\right]} \quad (17)$$

where V_B is the targeting breakdown voltage of the diode, ε is the dielectric constant of SiC and E_C is the critical electric field of the drift layer, which is dependent on drift layer doping (and is weakly dependent on drift layer thickness when the thickness is very low).

$$E_C = \frac{2.49 \times 10^6}{1 - \frac{1}{4}\log(N_D / 10^{16})} \quad (18)$$

With the equations above, the optimization of drift layer doping and thickness can be performed to achieve the lowest possible specific on-resistance of a unipolar device for a targeting breakdown voltage.

In figure 17, the drift layer thicknesses and specific on-resistances are plotted against the drift layer doping for a targeting voltage blocking capability of 1200V. In this figure, it is assumed that the SBD edge termination can obtain 80% of the ideal parallel breakdown voltage of the drift layer. The result shows that the optimum design is a punch-through (PT) structure with approximately 90% of the NPT doping and 87% of the drift layer thickness, giving 7% lower specific on-resistance than the NPT design.

As has been described in equation 12, the theoretical limit of the specific on-resistance of a SiC unipolar power device is around two to three orders of magnitude lower than that is silicon. In figure 18, experimentally reported SiC diodes with one of the lowest specific on-resistances are plotted versus the device breakdown voltage.

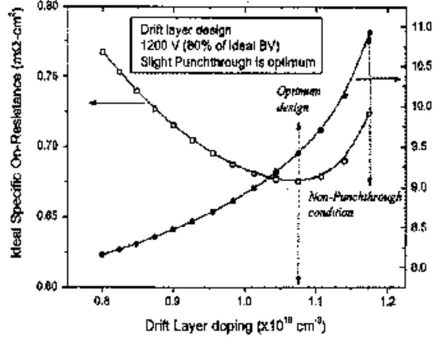


Fig. 17 Drift layer specific on-resistance and thickness versus doping for a breakdown of 1200V, assuming an 80% edge termination efficiency. The result shows that the optimum design can be achieved at approximately 90% of the NPT doping and 87% of the drift layer thickness [66].

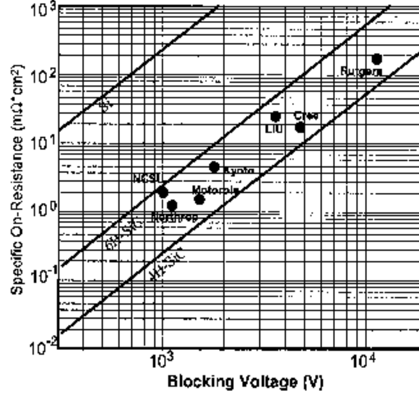


Fig. 18 Specific on-resistance versus breakdown voltage plot for Schottky barrier diodes

The forward voltage drops of the JBS, MPS, DMTS, TMBS structures described in the previous section can all be written as the sum of the Schottky barrier voltage (V_{SB}) and the voltage drop on the channel/grid resistance (R_{grid}) between field-shielding regions, the drift region resistance (R_{dr}), the substrate resistance (R_{sub}) and the backside ohmic contact resistance (R_{SB}).

$$V_F = V_{SB} + I_F(R_{grid} + R_{dr} + R_{sub} + R_{contact}) \tag{19}$$

For all four above structures, the forward conduction voltage will be somehow sacrificed because of the reduction in Schottky contact area through which current needs to flow. (The only exception is if the MPS diode has its P^+-n junction forward biased, injecting minority carriers and modulating the drift layer conductivity.) The amount of increase in forward voltage drop is a function of relative area of the P^+ regions to the total active device area [124 116]. The smaller the relative area of the P^+ regions, the less penalty on the forward voltage drop will incur. For devices with high blocking voltage, the drift region resistance component in equation 16 normally dominates. The increase of forward voltage, which arises from R_{grid}, will only be a small percentage of the total forward voltage drop [124, 116].

3.4.2 Temperature coefficient of the forward voltage drop

The variation of the forward drop of a SBD (or JBS, MPS) at different temperature can be determined by its three components given in equation 14. For a given current density within the range of practical interest, the first term in the equation is negative and is proportional to $T\ln(T)$. There fore, it decreases with increasing temperature. This is also evident from figure 16 where the reverse leakage currents are shown for different temperatures. The second term in equation 11, i.e., the barrier height, also decreases with increasing temperature, as have been discussed in section 2.2. The third term in the forward drop equation accounts for the contributions of resistances of drift region, substrate region and the ohmic contact region. For SBD with a low substrate resistance and a good ohmic contact on the cathode (anode for p-type SBD), the resistance is dominated by that of the drift region resistance, which increases substantially because of mobility degradation as temperature increases.

As a result, the temperature coefficient of the total SBD forward voltage drop depends on the relative magnitude of the three terms in equation 11 against temperature. When the current density is low, the first two components in the equation dominate against the resistive component and the temperature coefficient of V_F is negative. For the range of current density of practical interest (e.g., 1~500A/cm^2), because of the exponential dependence of current on the voltage for the first two components, they remain relatively constant. On the other hand, the resistive component will increase linearly and start to dominate. The temperature coefficient of the total device forward voltage will therefore change from negative to positive as the current density increases above certain level. Figure 19 shows the forward voltage drop of a SBD with relatively low voltage blocking capability (1.2~1.4e16cm^{-3}, 4μm) against temperature for different current densities. It can be seen that at around 300A/cm^2, the temperature coefficient of V_F becomes positive. For a SiC SBD with thicker and more lightly doped drift region, hence a higher blocking voltage, the contribution of the resistive term will be more significant and the V_F temperature coefficient will be positive at a lower current density.

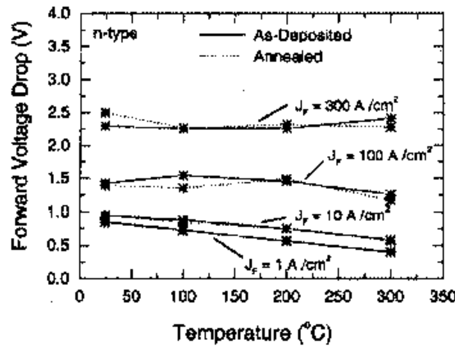


Fig. 19 Forward voltage drops of a Schottky barrier diode as a function of temperature for different current densities [92].

4. Applications in Power Electronics Circuits

4.1 Importance of power diodes and Silicon limitation

A major application of SiC Schottky barrier diodes is in power electronics systems. Performance of a power electronics system is largely determined by those of the power semiconductor devices, namely, the power switches and the fast diodes. During recent years, there have been substantial improvements on the development of Si power

semiconductor three terminal switches. These include the commercialization and optimization of the Insulated Gate Bipolar Transistor (IGBT) in the last 10 to 15 years. IGBTs now dominate the power semiconductor device market in the range of 600V to 3.3kV for most power electronics applications. Fast IGBTs have a switching speed of less than 100ns while still having conductivity modulation. The commercialization of CoolMOS^{TM} [142] device offers 600V to 800V rated power MOSFETs with specific on-resistance ($R_{sp,on}$) 5 times lower than the best traditional power MOSFETs and that break the theoretical $R_{sp,on}$ limit of Si unipolar devices. Unipolar devices like CoolMOSs can be switched with a switching speed of less than 10ns.

The improvements on the Si fast power diodes have been limited. In the range of 600V to 1.5kV, which represents the most commercially lucrative market portion, Si Schottky diodes are known as unsuitable for practical use because of their excessive on-state resistances and high leakage currents. Si P-i-N diodes are therefore invariably used. When conducting forward current, a P-i-N power diode structure features strong minority carrier injection which modulates the conductivity of the device drift region and hence drastically reducing its resistance. The injected carriers have to be removed from the drift region of the P-i-N diode when the diode enters reverse blocking mode. This charge-removal procedure significantly slows down the transition of the diode from forward conduction mode to reverse blocking mode when compared to that of a Schottky diode which is a unipolar device. The fastest Si power diodes available in the range of 600V to 1200V have reverse recovery times of around 50ns to 100ns. The slow recovery time of the diode results in a substantial amount of switching losses in both the power switch and the diode itself. The speed of the diode is slower than most power switches used in the circuit and has become the limiting factor preventing further improvements in many power electronics systems [143].

As mentioned in previous sections, a two to three orders of magnitude advantage in specific on-resistance is expected for Schottky-based diodes in SiC over those in Si. It is therefore possible to develop SiC Schottky-based unipolar diodes for voltages up to 2-3kV with a reasonably low on-state resistance. Unipolar diodes in the range of 600V to 3kV, when available, are very attractive for power electronics applications.

As described in sections 2 and 3, substantial efforts have invested on developing high voltage SiC SBDs for power electronics applications. While high voltage (~1000V) SiC Schottky-based diodes have been made as early as 1993, most diodes reported in early to mid-90's are of small device sizes and therefore are unable to conduct sufficient amount of current to be practically useful in a power electronics circuit. As the defect density of high quality SiC wafers decreases, SiC Schottky barrier diodes able to conduct significant amount of current (>a few amperes) where first reported in 1998 [101] and later in 2001 [102, 135]. It was followed quickly by the successful commercialization of SiC SBDs by power semiconductor device companies including Infineon AG, Microsemi Inc. and Cree Inc. Currently, Silicon Carbide SBDs from Infineon are available for voltage ratings of 300V and 600V with currant capability of 20A and 12A, respectively. SiC SBDs from Microsemi are available in 100V, 200V, 400V and 600V with a current capability of up to 4A. Cree currently offers SiC SBDs of 300V, 600V and 1200V with current capability of up to 20A. The commercial availability of these SiC SBDs provide a new opportunity of development for power electronics applications including high frequency switch mode power supply, power factor correction as well as low to medium power motor drive applications.

There have also been reports in the literature studying the circuit performances of commercial SiC SBDs as well as those fabricated in research labs, which demonstrated largely consistent results [131, 144-154]. In this section, performances of the SiC Schottky barrier diodes (or large area hybrid Schottky diodes) will be compared to silicon power diodes. The advantage and disadvantage of the SiC diodes will be discussed.

4.2 Semiconductor device losses in a power electronics circuit

In a power electronics circuit, power semiconductor devices (diodes and switches) largely dominate the whole circuit performance. A majority part of the circuit arises from the losses of these semiconductor devices. These include the losses of the power diodes and the switches:

$$\begin{aligned} P &= P_{Diode} + P_{Switch} \\ &= P_{D_CON} + E_{D_rr} f_{sw} + P_{S_CON} + (E_{S_on} + E_{S_off}) f_{sw} \end{aligned} \quad (20)$$

where P_{D_CON} is the diode conduction loss, E_{D_rr} is the diode reverse recovery energy, P_{S_CON} is the switch conduction loss, E_{S_on} is the switch turn-on energy, E_{S_off} is the switch turn-off energy and f_{sw} is the switching frequency. Losses caused by the leakage current of both the diodes and the switches can normally be neglected unless the devices are operating at the upper limit of their temperature capability (~175°C for Si and >300°C for SiC).

Switching frequency of a power electronics circuit is an important parameter which dominates the value as well as physical size and weight of energy-storage passive components, namely, power inductors and capacitors. The size and weight of these passive components, which dominate the size and weight of the system, are known to be *inversely proportional to the device switching frequency. While a higher switching* frequency is therefore desirable, a trade-off exists between the switching frequency and the switching losses (second and fourth terms in equation 20) which need to be kept below a certain level for system efficiency and thermal management considerations. Switches and diodes with low switching losses are therefore the key for size and weight reduction of power electronics systems.

4.3 Static characteristics comparison of commercial SiC and Si diodes

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In this section, the static characteristics of some commercial SiC power diodes are compared to those of silicon power diodes with similar voltage and current ratings. The commercial SiC diodes measured include SDT10S30 (300V, 10A) and SDT06S60 (600V, 6A) from Infineon and CSD20060 (600V, 10A) and CSD1020 (1200V, 5A) from Cree. Silicon devices used for comparison are some of the best fast recovery diodes available in the market: DSEP8-03 (300V, 10A) and DSEP30-12A (1200V, 30A) from IXYS [150].

The forward voltage drop of the diode accounts for the diode conduction loss, the first term in equation 16. The forward I-V characteristics of the Infineon SDT10S30 and IXYS DSP8-03 are plotted in figure 20 for different temperatures. Both devices, rated at 300V and 10A, are measured at 25°C, 100°C and 200°C up to 10A. As 300V silicon Schottky diodes are not commercially available for their excessive specific resistance, the IXYS device chosen is a P-i-N device.

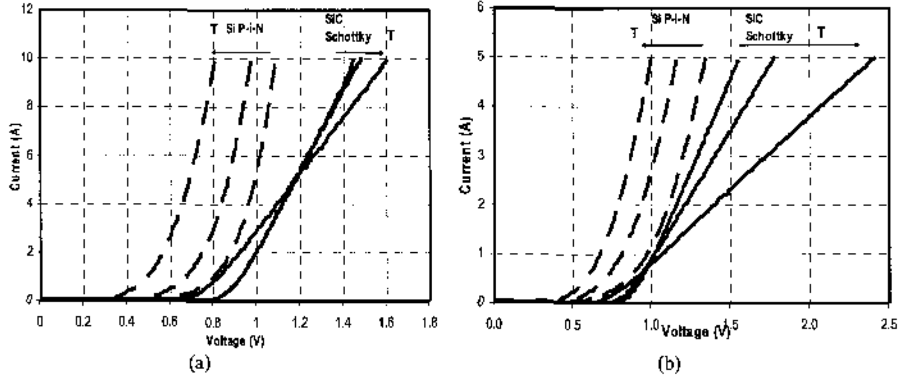

Fig. 20 Comparison of forward I-V characteristic at 25°C, 100°C and 200°C for SiC Schottky diode and Si P-i-N diode, (a), Infineon SDT10S30 and IXYS DSEP8-03, both rated at 300V, (b), Cree CSD1020 and IXYS DSEP20-12, both rated 1200V. Solid lines: SiC SBD. Dashed lines: silicon diode. Direction of the arrows indicates the increase of temperature

It can be seen that at room temperature, the SiC devices has a forward drop of approximately 1.5V and the silicon device has 1.1V. A clear different can be seen in figure 20.a between the two devices. As a bipolar power diode with high-level minority carrier injection in the epi base region, forward voltage drop of device DSEP 8-03 decreases significantly with increasing temperature. On the other hand, forward voltage drop of the SiC Schottky diode demonstrates a negative temperature coefficient at currents below 5A and a positive temperature coefficient at currents above 5A. The mechanism behind the variations of forward drop temperature coefficient has been discussed and agrees well with the analysis in section 3.4.2.

Tthe silicon device has a lower on-state voltage drop for all operation current levels and temperatures. A lower voltage drop will give less power loss and therefore is advantageous in the circuit. However, the negative forward voltage temperature coefficient of the silicon power diode is undesirable for connecting multiple devices in parallel when handling large load current. It is understood that when devices are connected in parallel, such a negative coefficient will more likely result in uneven current sharing among different devices. When such unbalance reaches a certain level, the whole system can become thermally unstable. The SiC device has a positive forward voltage temperature coefficient for the current levels above 50% of the rating where the devices is most likely to be used. It will therefore be more stable in case of parallel connection.

A similar comparison can be found in figure 20.b where the forward I-V curves of CSD1020 (1200V, 5A SiC diode from Cree) and DSEP30-12A (1200V, 30A silicon diode from IXYS) are shown. Temperature coefficients of the forward voltage have shown similar trend for both devices with the silicon bipolar device demonstrating negative value and the SiC diode showing different polarity at different current levels.

It is worth noting that since the silicon devices is rated at a higher current, its forward voltage drop at its rated current level (30A) is slightly higher than that of the SiC device at room temperature. It can also be seen that for the SiC device, temperature coefficient for the forward voltage becomes positive at a lower current when compared to the 300V SiC device. The reason is explained as follows. While the knee voltage (first term in equation 15) remains the same for the 300V and 1200V SiC devices, the drift region resistance becomes more dominant for the device with a higher voltage rating

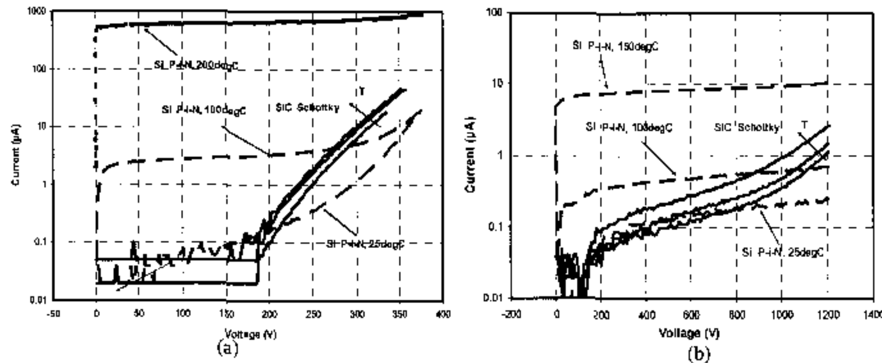

Fig. 21 Reverse I-V characteristic of SiC Schottky diode and Si P-i-N diode at different temperatures, (a), Infineon SDT10S30 and IXYS DSEP8-03, both devices are rated at 300V, and (b) Cree CSD1020 and IXYS DSEP20-12, both rated at 1200V. Solid lines: SiC SBD. Dashed lines: silicon diode. Direction of the arrows indicates the increase of temperature for the SiC SBD.

because of a thick and more lightly doped drift layer needed to block the required voltage. The temperature coefficient of the resistive component of the voltage drop will therefore also become more dominant. As explained in section 3.4.2, since the knee voltage decreases with increasing temperature and the drift layer resistance increases with temperature, the overall forward voltage temperature coefficient of the 1200V SiC diode is more positive than a 300V SiC diode.

While an increasing forward voltage is beneficial for device parallel connection, it does increase the conduction loss of the diode at high temperatures. The conduction losses of the SiC diodes are therefore generally higher than those of their silicon counter parts.

Another important static parameter of a diode is its reverse-blocking characteristics. In figures 21, variations of the reverse-blocking I-V curves at different temperatures are plotted for the 300V devices and 1200V devices, respectively.

The reverse leakage currents of the SiC Schottky devices are in sub-μA level for most part of reverse blocking characteristics. It can be seen that, for both 300V and 1200V comparisons, the SiC Schottky diodes have lower leakage current except when the voltage increases to a level close to or exceeding the voltage rating. In practical applications, devices are not normally stressed with such voltages. Both figures also show that the leakage currents of the silicon P-i-N diodes are orders of magnitude higher than their SiC counterparts at 200°C. The excessive amount of leakage current for the silicon devices prevents them from being reliable at this high temperature.

Comparisons of forward and reverse I-V curves of SiC SBDs from different manufacturers with similar voltage and current ratings show that differences are insignificant. The small differences can be accounted for by different manufacturing process and die sizes.

4.4 Dynamic characteristics comparison of commercial SiC and Si diodes

Dynamic characteristics of the diode are important for power electronics applications that require high frequency switching such as switch mode power supply, power factor correction, power inverter for induction heating and some motor drives. Low switching

energies (E_{D_rr}, E_{S_on} and E_{S_off} in equation 20) are the key for high frequency switching which will enable a small system size and high efficiency.

Typical building block of a power electronics system is shown in figure 22. This circuit is also known as the 'clamped inductive load switching circuit'.

When the switch turns on, the load current diverts from the diode (normally named a freewheeling diode) to the switch. During the transient of switch turning on, the diode changes from forward conduction to the reverse blocking status. Reverse recovery time of the diode is the most important parameter for this transition since it determines the peak currents of diode and switch as well as the amount of losses incur on these two devices during this transition (E_{D_rr}, E_{S_on} in equation 20) [151].

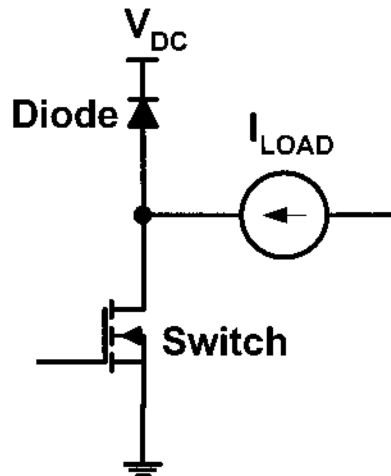

Fig. 22 Typical building block of a power electronics system comprises a switch, a free-wheeling diode.

Reverse recovery transients of the following three SiC diodes were evaluated at 25°C, 75°C and 150°C: UPSC200 (200V, 1A from Microsemi), SDT06S60 (600V, 6A from Infineon) and CSD10120 (1200V, 5A from Cree) [150].

The reverse recovery current waveforms are shown figures 23, 24 and 26. To leave some margin for safety, the DC voltage used in for these groups of measurements are 126V, 400V and 1000V, respectively.

In figure 23, the silicon device used is a 150V, 5A Schottky diode and both devices are tested at 1A forward current. It is clear that both reverse recovery time and peak current for the Si diode increases considerably with increasing temperature. On the other hand, reverse recovery time and peak current of the SiC Schottky diode showed no noticeable change as the temperature was increased from 25C to 150C, as seen by the reverse recovery curves lying on top of each other. Also, the reverse recovery current of the SiC Schottky diode is considerably lower than that of the Si Schottky diode.

The silicon diode used in to compare with SDT06S60 was DSEI8-06A (600V, 8A) from IXYS. Both devices were tested at 400V and 3A. It can be seen that the peak reverse recovery current of this silicon device increases from 4A at room temperature to over 8A at 150°C. It reverse recovery time also increase substantially. The reverse recovery current waveforms of the SiC SBD remain almost unchanged for the different temperatures with a peak reverse current well below 2A. Similar comparison can be seen in figure 25 where the 1200V SiC diode was compared to a 1200V ultra-fast silicon diode (DSEP30-12A from IXYS).

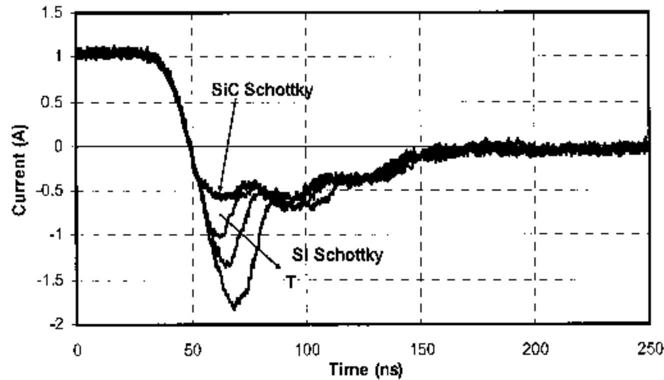

Fig. 23 Reverse recovery current waveforms at 25°C, 75°C and 150°C for the IR 10CTQ150 (150V/5A) Si Schottky diode and the Microsemi UPSC200 (200V/1A) SiC Schottky diode with V_{DC}=126V. Direction of the arrow indicates the increase of temperature.

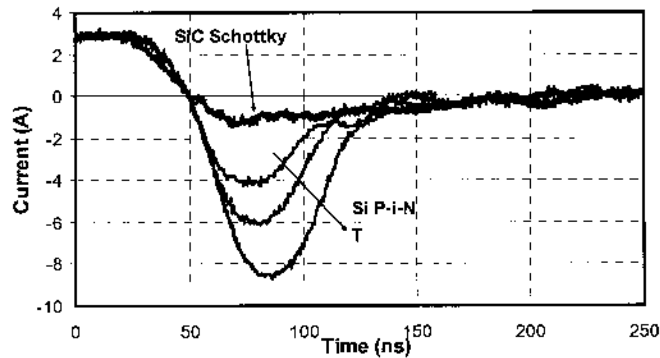

Fig. 24 Reverse recovery current waveforms at 25°C, 75°C and 150°C for Infineon SDT06S60 (600V/6A) SiC Schottky diode and the IXYS DSEI 8-06A (600V/8A) ultra fast Si diode with V_{DC}=400V. Direction of the arrow indicates the increase of temperature.

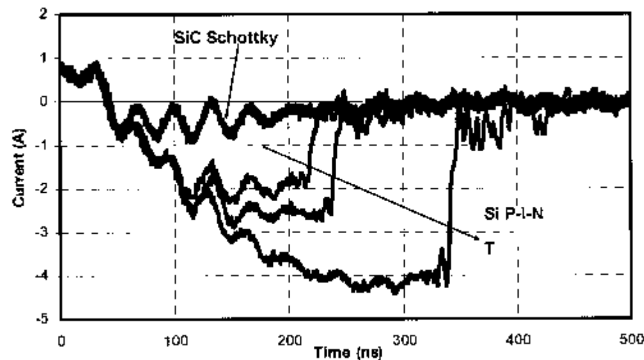

Fig. 25 Reverse recovery current waveforms at 25°C, 75°C and 150°C for Cree CSD10120 (1200V/5A) SiC Schottky diode and the IXYS DSEP30-12A (1200V/30A) ultra-fast silicon diode with V_{DC}=1000V. Direction of the arrow indicates the increase of temperature.

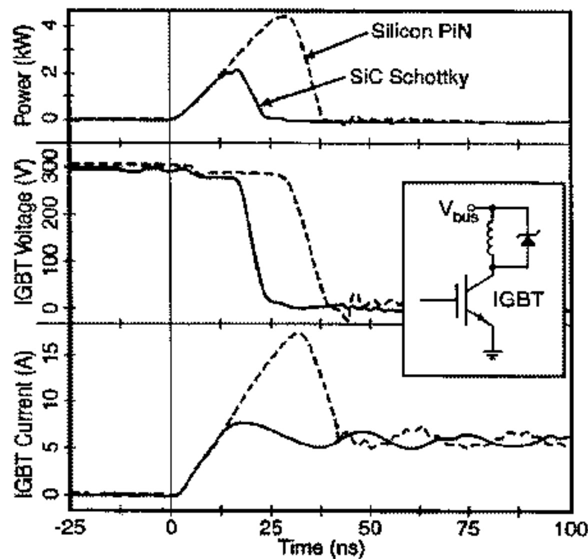

Fig. 26 Turn-on waveforms of a clamped inductive load circuit, comparing a SiC SBD with a commercial silicon P-i-N (RHR660) diode. From top to bottom, power, voltage and current waveforms of the switch [145].

It is noticeable that for SiC SBDs with these three blocking voltage, the reverse recovery current waveforms do not increase with increasing temperature. Similar findings have been reported in [145, 149, 152, 153]. This is due to the fact that as a unipolar, the reverse recovery currents are mainly caused by internal device junction capacitance and, to a certain extend, some packaging capacitances. In contrast, there is a substantial increase of reverse recovery time and peak current at higher temperature in the silicon devices. This can be explained by the increased minority carrier injection and hence storage charge at higher temperatures. The storage charge of a silicon power diode also increases with device voltage rating because of a thicker charge storage layer. This can be used to explain the difference between the SiC SBD and silicon diode is also found to be dramatic for devices with higher voltage rating.

The drastically reduced reverse recovery current and charge virtually eliminated the dynamic losses of the diode. In addition, the close-to-zero recovery time of the SiC SBDs can also reduce the turn-on energy (E_{S_on} in equation 20) of the corresponding switch substantially. Because the turn-on energy of the switch is typically larger than the dynamic loss of the diode itself, more loss reduction can actually be obtained on the switch than on the diode itself. Figure 26 shows the voltage, current and power waveforms of such a switch during turn-on with a SiC SBD and a normal silicon power diode. The SiC device used was a 1200V, 6A Schottky diode. It is evident that the fast speed of the SiC diode resulted in significant reduction in turn-on energy. It was reported that the turn-on energy of the switch can be reduced by a factor 2-6 [145, 149].

Many high frequency power electronics circuit uses power MOSFETs as the switch. In these circuits, when silicon P-i-N diodes are used, switching speed is typically limited by that of the diodes. By replacing the bipolar silicon P-i-N diode with a unipolar SiC diode, the whole power electronics comprises of only unipolar semiconductor devices and

the switching speed can be substantially increased. Power factor correction circuit using a combination of SiC Schottky diode and superior 600V CoolMOS has been reported to operate at close 400kHz without significant amount of switching losses [154], as shown in figure 27. From the figure, it is reasonable to project that such combination can switch at frequencies above 1MHz. SiC SBDs as the zero-recovery diode will have great impacts on high frequency power electronics applications.

The unique high temperature capability of the SiC diode also offers potential application for power electronics in high temperature environments. However, because of the lack of commercially available SiC three terminal switches, the high temperature capability of the commercial SiC diodes has so far not been fully taken advantage of.

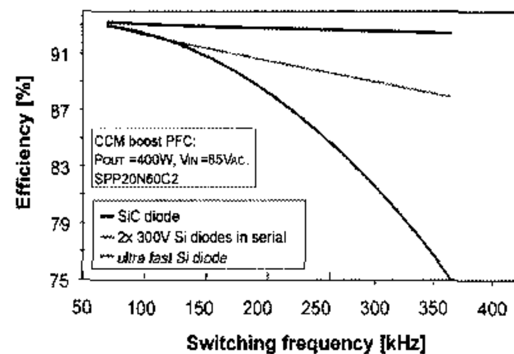

Fig. 27 Efficiency comparison of a power factor correction circuit with a 600V MOSFET and SiC diode or silicon diodes. With superior unipolar switch and SiC diode, the switching losses are kept low and efficiency remains almost unchanged for frequencies up to 400kHz. [154]

5. Other Application of SiC SBD

In addition to their application in high frequency power electronics applications, SiC Schottky barrier diode structure can also be used in other applications such as gas sensors, microwave circuits and UV detectors. In this section, these applications of SiC SBDs will be briefly introduced.

5.1 SiC SBD as gas sensor

Increasing regulations on the release of gases or other chemicals into the environment have led to the increased attention on development of advanced sensors. There is a strong interest in SiC-based gas sensors for applications including fuel leak detection in automobiles and aircraft, fire detectors, exhaust diagnosis and emissions from industrial processes. Because of its wide bandgap, SiC is capable of operating and remain stable at much higher temperatures than many of the conventional semiconductors such as Si. Simple Schottky diode or field-effect transistor structures fabricated in SiC are sensitive to a number of gases, including hydrogen, hydrocarbons and oxygen [155-168]. Gas sensitive SiC SBDs with palladium gates were reported in 1992 [169]. Operation of SiC SBDs as a gas sensor has been reported at above 550°C.

Hydrogen atoms can be dissociated from hydrogen molecules and diffuse through the thin metal layer and form a polarized layer on the metal-semiconductor interface. This polarized layer changes the barrier height of the Schottky contact and shifts the I-V curve of the diode, typically toward lower voltage. A typical response in the I-V curve to the ambient gas is shown in figure 28. A significant shift in the I-V curve can be seen, which can be easily detected by an electronics circuit. Such SiC SBD gas sensors can also be used to sense carbon monoxide (CO). The response time of the sensor is in the order of milliseconds [157].

One additional attractive attribute of SiC is the fact that gas sensors based on this material could be integrated with high temperature electronic devices on the same chip.

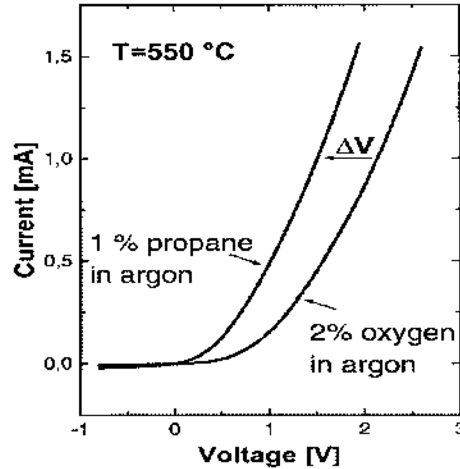

Fig. 28 Typical I–V curve for a Schottky diode at 550°C. The sensor response is indicated by an arrow. Composition of the device: Pt (150 nm); TaSix (15 nm); 6H SiC. [157]

5.2 SiC SBD in microwave applications

The application of SiC SBD in microwave are mainly related to those require high voltage or high power, for example in limiters and high level mixers. There have been some limited works reported for such applications of SiC SBDs [170-173].

The cut-off frequency of the SiC SBD used as a varistor in a mixer circuit can be defined as:

$$f_C = \frac{1}{2\pi C_{j0} R_S} \tag{21}$$

where C_{j0} is the junction capacitance at zero bias and R_S is the series resistance of the device. The cut-off frequency is regarded as the figure-of-merit for such applications. For similar reasons as have been mentioned in equation 12 of section 3, when a relatively high voltage is needed, SiC SBDs can offer significant advantage over conventional materials such as Si and GaAs.

A theoretical calculation based on physical parameters of 4H-SiC gave an optimization curve set for circle-shaped 4H-SiC SBDs, as shown in figure 29.

The first SiC SBD mixer was published in [170] on a 0.4μm, 4e17cm^{-3} doped 4H-

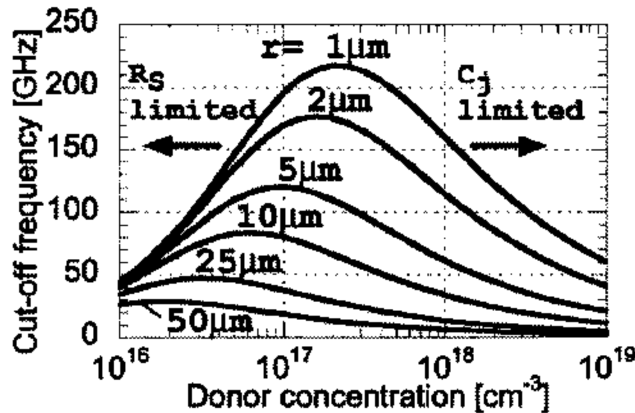

Fig. 29 Cut-off frequency versus drift layer doping of a circular 4H-SiC SBD diode for microwave mixer application. Results for different radius are plotted. [173]

SiC. The device uses Au/Ti as Schottky contact metal and has an area of 40*40μm^2. The same group reported a similar SiC SBD on a 0.38μm, 2.8e17cm^{-3} drift layer, a 0.5μm, 8e18cm^{-3} buffer and a 340μm, 1.1e19cm^{-3} substrate [173]. Limited by large ohmic contact resistance and designed for relatively low frequency application, these fabricated diodes has the lowest conversion loss of 5.2dB at a frequency of 800MHz.

5.3 SiC SBD as UV detector

SiC SBDs have also been used as detectors for radiations such as UV light [174-177], neutrons [178] and others [179-183].

The accurate measurement of UV radiation exposure has become increasingly important as a result of increasing environmental pollution. The main problem with UV silicon detectors occurs as a result of the supplementary radiation filtering required in order to eliminate the visible and infra-red part of the light, which blinds the detector. The 3.3eV bandgap of 4H-SiC means a SiC detector respond to light only in the 210-380nm UV range. The longer wavelength from visible and infra-red radiation can not bridge the wide bandgap, and hence the SiC detector is insensitive to these wavelengths and consequently does not necessitate supplementary radiation filtering. This is a great advantage in detecting UV in the presence of the substantial visible and infra-red background which generally is the case. Furthermore, as a wide bandgap material, SBDs made on SiC can have extremely low leakage current, substantially enhancing the sensitivity of the device.

Silicon Carbide UV detectors were fabricated on Schottky barrier structures by depositing a semitransparent (75Å) layer of Pt on top of a 3.7μm N- 4H-SiC epi layer (3e14~3e15cm-3) [177]. Schottky photodiodes with the device area of 0.25mm×0.50 mm, 2mm×2mm, 5mm×5mm, and 1cm×1cm were fabricated. The photodiodes demonstrated extremely low leakage current. The leakage current of a 5mm×5mm device is less than 1.2e-14A at a voltage bias of -1V. The quantum efficiency of the SiC Schottky photodiodes is shown in figure 30 for the spectra between 200nm and 400nm. Unlike GaN, 4H-SiC is indirect semiconductor, and does not have a sharp cutoff edge at the band edge. The absorption coefficient increases slowly from 385 nm as the wavelength decreases. As a result, the quantum efficiency of 4H-SiC Shcottky diodes increases gradually from less than 0.1% at 380 nm to 37% at 300 nm. The maximum quantum efficiency is around 37% and nearly constant from 240 to 300 nm.

The sensitivity of the SiC SBD UV detector was also evaluated. For a detector at zero bias, the noise of the detector is dominated by the Johnson noise. D^* is one of the most frequently used figure of merits to evaluate the sensitivity of photodetectors and is defined as [177]

$$f_C = \frac{q\eta}{hv}\left[\frac{R_0 A}{4k_B T}\right]^{1/2}$$

when the Johnson noise dominates, where is the quantum efficiency, h is the Planck constant, v is the radiation frequency, R_0 is the dynamic resistance at zero bias, and A is the detector area.

The of 4H-SiC Schottky photodiodes is calculated based on the directly measured results of our 5 mm 5 mm photodiodes and compared with other common photo detectors in figure 31. The maximum sensitivity of 4H-SiC Schottky is 3.6×10^{15}cmHz^{½}/W at

300nm and the sensitivity is above 10^{15}cmHz$^{1/2}$/W from 210 to 350nm. This sensitivity is two orders of magnitude higher than that of Si photodiodes and three orders of magnitude higher than the of Si CCD.

Sensitivity of the SiC SBD is limited by many different types of defects on the surface of the material [184] that will cause inhomogeneous barrier height across the device. The effective SBH of the device fabricated is expected to be significantly lower than the theoretical value of 2.0eV for Pt/4H-SiC. Therefore, as the defect density decreases and material quality improves, the leakage current of the SBD can be further reduced and the sensitivity further improved.

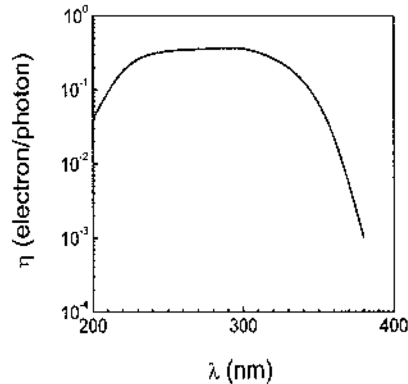

Fig. 30 Photo response spectra in quantum efficiency of Pt/4H-SiC Schottky photodiodes [177]

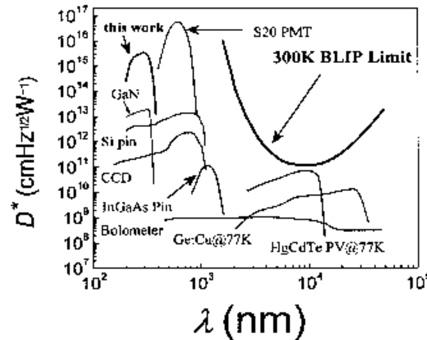

Fig. 31 Sensitivity comparison between SiC Schottky 5mm*5mm photodiodes and some common detectors. The 300K blackbody radiation limited D*, 300K BLIP limit, is also inset as a reference [177].

More details on the application of SiC SBDs as detector for other particles such as neutrons [178] and others [179-183] can be found in the literature.

5. Summary and Future Challenges

5.1 Summary

In summary, basic physics of metal to SiC Schottky contact that determines the Schottky barrier height (SBH) and the carrier transport mechanisms have been explained. Barrier height of a SiC Schottky contact is dependent on factors such as metallization choice, SiC poly-type, face polarity, surface treatment, post deposition annealing and SiC material doping. With increasing metal workfunction, the SBH of an n-type contact increases while that of a p-type contact decreases. The rate of change in SBH with metal workfunction (interface slope parameter, S) is found to be value between 0 and 1, depending on the density of interface states. Different interface state density could result from different surface treatments and conditions. Unpinning of the SiC Fermi level by a drastic reduction in interface state density has been reported with special surface treatment techniques. The interface slope parameters are also found to be dependent on the SiC poly-type with 0.6 for 6H-SiC -type and 0.9 for 4H-SiC n-type contacts. Overall, a range of 0.3eV to 2.0eV has been obtained for SiC n-type SBH. Although less investigation on p-type SiC Schottky contact has taken place because of its less practical

usefulness resulted from the lower mobility of holes in SiC, studies have reported p-type SBH between 1.3eV to 2.0eV.

Because of its wider bandgap, contacts on the 4H poly-type has shown a SBH 0.2~0.4eV higher than that of those on 6H poly-type. For both 6H and 4H poly-types, Schottky contacts on carbon-terminating SiC materials have shown higher barrier heights than those on silicon-terminating SiC materials. Since metal-semiconductor interface chemistry is critical for a SiC Schottky contact, pre-deposition SiC surface treatment, metal deposition conditions and post-deposition annealing conditions have all found to influence the resultant SBH significantly. For instance, the Pt-SiC SBH can increase significantly with post-deposition annealing because of the formation of silicide. The substrate temperature during metal deposition has also been reported to affect the resultant SBH because of different chemical reactions taking place.

The SBH of a SiC Schottky contact has also been found to decrease as the semiconductor doping increases above 3e17cm^{-3} level. The reduction can be explained by the combined effects of image force lowering and charge distribution across the contact interface. At temperatures above room temperature, SBH of n-type SiC Schottky contact has been reported to decrease with increasing temperature while the p-type SBH shows an increase. The SBH sensitivity to temperature was linked to the electronegativity of the metal used. The sensitivity was found to be low for metals with a low electronegativity.

Extensive efforts in the development of SiC Schottky barrier diodes for high power application in the last ten years or so have resulted in substantial improvements in both the voltage and current capability of this device. While most studies have been done on 6H-SiC before 1995, the efforts have been largely shifted to 4H-SiC after 1995 when high quality 4H-SiC material became widely available. 4H-SiC SBDs with a breakdown voltage of 10.8kV was reported with a specific on-resistance of 187Ωcm^2 [2] and single dies with an area of 1cm^2, able to handle >200A, have been fabricated with low leakage current. In achieving a good voltage blocking capability, various edge-termination techniques have been used. Techniques such as floating metal rings, P$^+$ region rings, p-epi guard rings, inert gas implantation and metal field-plating have been proven to be effective at low to medium voltage ranges (<2000V). Muti-step junction termination extension (MJTE) technique was demonstrated to be effective at voltages above 10kV.

A higher SBH will give lower diode reverse leakage while sacrificing forward conduction voltage. The reverse leakage current of a SiC SBD has however been reported to be significantly higher than predicted by single-barrier thermionic emission theory. Material inhomogeneous has been suggested as possible causes. The leakage current also increases quickly with increasing reverse bias voltage due to the effects of electric field induced barrier lowering and tunneling. To reduce the electric field at the Schottky contact area and hence the diode reverse leakage current, many structures utilizing the electric field shielding effect of high-barrier-junction depletion regions have been proposed. These include JBS, MPS, DMTS, DMP, TMBS and LMDS. With different processes and approaches, these variants aimed at the achieving a low leakage current with the same electric field shielding principle. Leakage currents orders-of-magnitude lower than the corresponding SBDs were reported with minor sacrifice on the forward conduction voltage. JBS diodes with large current carrying capability were successfully used in power electronics applications [SiC motor drive paper, Zhao].

The developments of SiC SBDs have enabled successful their commercialization for power electronics market. More than five manufactures have already offered SiC SBDs

with different voltage and current ranges. SiC SBDs are now commercially available with voltage up to 1200V and current up to 20A.

Comparisons on the performances of these SiC SBDs were made to existing silicon parts with comparable ratings. While the SiC SBDs do show higher forward conduction voltages than their silicon counterparts at the 300V rating, their forward voltage become comparable to that of the silicon device for the 1200V class. The SiC SBDs are found to offer significant advantages in all other aspects of the required performances. SiC SBDs have clear positive temperature coefficient on their forward voltage drop, enabling easy and reliable parallel connection of multiple chips for higher current application. They also demonstrated orders of magnitude lower leakage current, especially at temperatures higher than 150°C. This shows clearly their capability of operation at a temperature well above 150°C, which is widely expected due to the wide bandgap nature of the material.

The greatest advantage of SiC SBDs in a power electronics application is its close-to-ideal dynamic performance. During the crucial reverse recovery transient when the diode changes from a forward conduction mode to a reverse blocking mode, it demonstrated virtually zero recovery time, which remains unchanged over the full range of operating temperatures. This is mainly due to that fact that SiC SBD is a unipolar device without minority carrier injection and hence free of storage charge. The only charge involved in the recovery transient is the junction depletion charge which has been found to be more than one order of magnitude lower than the recovery charge of a similar silicon device. The advantage is especially drastic for devices with higher blocking voltage and/or at higher temperatures. This represents a breakthrough in power electronics device development and solves a major bottleneck in high frequency power electronics application where the speed of the diode seriously limits the whole circuit performance. Applications of the commercial SiC SBDs in high frequency switch mode power supplies, power factor corrections and some motor drive applications have been reported. Combined with the best available power MOSFETs, hard-switching frequencies up to 400kHz have bee demonstrated and a frequency of above 1MHz can be easily expected. This is substantially higher than the typical 100kHz frequency used for devices at this high voltage level (>600V).

In addition to their application in power electronics systems, SiC SBDs can also be used in other applications such as gas sensing, microwave applications and ultra-violet light detection. Their wide bandgap and exceptional stability at temperatures as high as 500°C give SiC SBDs their unique advantages for these applications.

5.2 Future trends and challenges in SiC SBD development

The development of SiC SBDs has been exciting in the last a few years with devices able to handle >10kV or >100A being reported by research labs. Commercially available SiC SBDs have already demonstrated exceptional performance advantage over existing silicon fast-recovery diodes for high end power electronics applications. Commercial devices are currently limited to 1.2kV and 20A in their ratings.

It is expected that SiC SBDs with higher voltage and current handling capabilities will continue to be pursued by both research labs and commercial companies. Commercial devices capable of handling up to 3-5kV will be able to provide significant system advantage for relatively high power electronics applications.

In order to achieve SiC SBDs with 3-5kV breakdown voltage for commercial production, one of the challenges ahead is a reliable edge termination technique that gives

high reproducibility, high yield, simple fabrication procedure and low leakage current. While various termination techniques have been used to obtain a high blocking voltage, as mentioned in previous sections, most of those involves an ion implantation step which generally results in increased leakage and reduced reliability. Issues associated with ion implantation caused crystal damages will need to be address or an implantation-free method will be needed for a termination technique that will satisfy criteria mentioned above. In addition, an appropriate passivation process for the edge termination region is also critical in achieving a high-voltage-blocking device with a reliable and low leakage current.

Another important challenge for continuous development of SiC SBDs will be the SiC wafer substrate and epitaxial quality, which is also the basis for continuous and success development of all SiC devices. While great improvements have been obtained in recent years on SiC substrate wafer and epitaxial layer quality, ultra-high quality SiC wafers with lower defect densities and larger sizes are needed. A breakthrough in ultra-high quality SiC substrate growth has been recently reported [185] by using a repeated a-face (RAF) growth process, demonstrating 2" SiC substrates with zero micro-pipe density and an etch pit density two to three orders of magnitude lower than the best existing materials available. This is an important development in single crystalline SiC material growth. Extending this method to wafers with larger diameter (3", 4" and beyond) will promise an encouraging future in future SiC device development.

While SiC SBDs have been able to successful compete with existing Si devices in high end power electronics applications such as server and telecom power supplies, significantly higher product cost have been the major obstacle that has so far prevented their penetration into the mass consumer market (e.g., PC power supplies). The SiC device cost is mainly dominated by the orders-of-magnitude higher base material cost when compared to silicon. Per-device cost can be reduced by reducing the wafer cost as well as increasing wafer diameter. Currently, commercial SiC substrates are available with 3" diameter which gives significant cost advantage over the widely-used 2" wafers. This results from both the increased device yield and more alternatives in processing equipment when compared to 2" wafers. Many relatively modern and automated 4" production facilities used for silicon device can be modified for the 3" SiC wafers, giving high reproducibility, low fabrication defect density and better device reliability. Good device yield and performance uniformity have been reported [186]. With larger SiC wafers, devices with higher current capability can also be fabricated with better yield. Power modules capable of handling hundreds of amps with SiC SBDs will be expected in the reasonably near future.

A unique market for SiC SBDs is the high temperature electronics market because of their capability of reliable operation at high voltage and high temperature. While there the SiC SBDs are able to handle well beyond 200°C, the development in realizing the potential of these devices for high temperature (>200°C) application has been limit by available packaging approaches. Commercially available SiC SBDs are therefore currently only rated for 175°C. Identifying a viable packaging technology that can remain reliable at temperature well above 200°C becomes the main challenge in applying SiC SBDs for high temperature high power applications.

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