# Validity of Using a Fixed Analog Input for Evaluating the SEU Sensitivity of a Flash Analog-to-Digital Converter

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Abstract-- The SEU rate in a flash ADC (AD9058) on board a space experiment varied by more than an order of magnitude, depending on the input. A pulsed laser aided in elucidating the reasons, which were found to be the result of the unique design of the AD9058.

### I. INTRODUCTION

Analog-to-DIGITAL Converters (ADCs) are widely used in space systems, raising the concern that in the presence of ionizing particle radiation their performance will be degraded by single-event upsets (SEUs). SEUs appear as deviations from the expected digital output values. Those deviations may be large or small and may last for one conversion cycle or for many, depending on the type of ADC.[1,2]

Before being included in a spacecraft's electrical system, ADCs must be tested for their SEU sensitivity using heavy ions and protons. Planning for the test involves making a decision on how to electrically configure the ADC, i.e., whether to use a static or dynamic input. Most SEU tests of ADCs have been performed with a fixed, or static, input voltage. The first reported SEU test of an ADC was for the AD42691 feed-forward, series-parallel converter with integral track-and-hold amplifiers, a device with a fairly complicated architecture.[1] SEUs appeared as both small and large deviations from the expected digital output value. The distribution of small deviations around the expected digital output value had a Gaussian shape, whereas large deviations (termed "offset" SEUs) appeared at multiples of the expected value. Because measurements were performed with a single analog input voltage, no information was obtained on whether the SEU distribution and cross-section depended on input voltage. A more recent publication details the testing of a

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high-speed (1.5 GSPS) flash ADC using a number of different static input voltages.[2] Of significance was the fact that the SEUs lasted for many conversion cycles and that the maximum deviation depended on ion LET. No significant dependence of SEU rate on analog input voltage was noted. The literature contains one report on SEU characterization of ADCs with a dynamic input.[3]

To improve our understanding of SEUs in ADCs, we selected an 8-bit flash ADC (AD9058) for inclusion in a space experiment – the Microelectronics and Photonics Testbed (MPTB). The goal of the space experiment was to measure SEU rates in space and compare them with calculated rates based on models of radiation response and the results of ground testing. Some initial results have previously been published.[4]

During the five years MPTB has been in orbit, five different analog input values were used. A dynamic input was avoided because of the increased complexity in designing the board and also in understanding the results. Ground testing involved measuring SEU cross-sections as a function of ion LET and proton energy. Because of limited time and resources, ground testing was done for only a single analog input voltage, the same voltage as used in one of the configurations in space. The results were used to calculate SEU rates in space for all input voltages and the calculated rates were compared with the actual SEU rates. The environment was continuously monitored using a proton telescope and heavy-ion spectrometers so that short-term variations in the environment could be taken into account when making the comparisons.

The results of our calculations, based on ground data, show remarkably good agreement with the observed SEU rates in space for four out of the five analog input voltages. However, for one input voltage, the measured SEU rate was smaller than the expected rate by over an order of magnitude. A pulsed laser was used to probe the SEU-sensitive areas of the chip to identify the origins of this anomaly. It revealed that for four of the input values the cross-section varied by about 20%. However, for the input value used when the observed SEU rate in space was unexpectedly low, the total SEU sensitive area measured with the laser was found to be much smaller. A circuit model of the unique structure of the ADC was used to explain this behavior. These results show conclusively that testing ADCs for their SEU sensitivity using

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a series of fixed analog input voltages is not a valid approach. A more accurate method would be to use a dynamic input.

### II. DESCRIPTION OF PART AND EXPERIMENT

The AD9058 is a dual 8-bit flash ADC that operates at 50 MSPS and has been described in a previous publication.[4] It consists of 128 comparators, interpolating latches, decoding logic and output registers. Normally, an 8-bit flash ADC requires 256 comparators. However, the AD9058 uses only half the number of comparators because its design uses a patented approach involving interpolating latches. Figure 1 shows a photomicrograph of one of the analog-to-digital converters on half of the chip. Although the manufacturer would not provide circuit diagrams and layouts, we were able to identify some of the functional parts on the chip. The comparators are visible as 32 identical structures in four parallel rows. The output registers, consisting of 8 identical structures, are clearly visible at the left end of the chip. Between the output registers and the banks of comparators is the ROM decoding circuitry. The encoding read-only memory is located between the rows of comparators.



Figure 1. Photomicrograph of one half of the AD9058 showing a single ADC. Each of the four horizontal structures contains 32 comparators. The eight output registers are at the left end of the chip.

Three AD9058 parts were included on the MPTB flight board. Together they provided six digital outputs. An identical board was used for ground testing. To ensure that there were no differences that might affect the measured SEU rates, the flight and ground software were identical. Different analog input voltages were applied to the ADC inputs by connecting them to a reference voltage through one of sixteen different resistors. During the time MPTB has been in orbit, five of sixteen possible input values were selected. In order to minimize the amount of data storage, a command in software set a window around the expected output, and as long as the output remained within the window, no data were recorded. The width of the window was set sufficiently wide to bracket the noise around the digital output. SEUs were flagged and recorded when their values were outside the window. The SEUs in the ADCs on board MPTB were stored and then sent via a downlink to a ground station for analysis. Proton and heavy-ion fluxes in space were constantly measured and downloaded together with the SEU data so that changes in the SEU rates could be compared with changes in the radiation environment.

The results of the ground testing were discussed in a previous publication.[4] The functional dependence of crosssection on heavy ion LET together with the cross-sections measured at two different proton energies were used to calculate the SEU rates. We note that the digital output during all heavy-ion and proton testing was set to 118 and the window was between 114 and 124. For ground testing, one of the ADCs was removed from the board and inserted in a socket attached to the side of the board. The socket was sufficiently far away from all the other components on the board that only the ADC in the socket was irradiated with protons or heavy ions.

A pulsed-laser was used to identify the SEU sensitive areas.[4] To do this, a focused beam of light (diameter of 1.5 microns, wavelength of 590 nm, pulse width of 1 ps and repetition rate of 1 KHz) was scanned across the surface of the chip while the output was being monitored for SEUs. The same input analog voltages and digital output windows used in space were used for pulsed laser testing. The total SEU sensitive area, as measured with the pulsed laser, should correspond to the saturated SEU cross-section measured with heavy ions.

### III. RESULTS

As previously mentioned, during the time MPTB has been in orbit five different analog voltage inputs have been used. Table I shows the nominal digital output values (in HEX and decimal) and the lower and upper values of the windows around the digital outputs. Table I also includes the date on which the configuration was set. The last data were collected on 12/14/02.

TABLE I NOMINAL DIGITAL OUTPUTS AND LOWER AND UPPER LIMITS OF WINDOW IN HEXADECIMAL AND DECIMAL

Start Date	Digital Output	Lower Limit	Upper Limit
11/27/97	0x11(17)	0xOF(15)	0x15(21)
6/13/98	0x45(69)	0x42(66)	0x4A(74)
11/8/98	0x75(117)	0x72(114)	0x7C(124)
4/6/99	0x84(132)	0x7F(127)	0x89(137)
1/13/00	0x63(99)	0x60(96)	0x6A(106)

A comparison of calculated and measured SEU rates in space was reported in a previous publication.[5] Comparisons were made both during the solar particle event of  $5^{th}$  November 2001, known as the Guy Fawkes Day Event, and during the "quiet" time prior to the event. At the time the digital output value for all the ADCs was set to 100 with a window bracketing the output from 96 to 106. (Clearly, SEUs that caused deviations in the three least significant bits were not recorded.) Those values are not the same as used during the heavy-ion and proton testing, yet the agreement between

To be presented at the European Conference on Radiation and its Effects on Components and Systems (RADECS), Grand Hotel Huis ter Duin, Noordwijk, Netherlands, September 15-19, 2003. the predicted SEU rate using the ground data and the actual SEU rate measured on board MPTB were remarkably close. This suggests that the LET thresholds and the saturated cross-sections for these two configurations are close.

A significant drop in the SEU rate was noticed after  $6^{th}$  April 1999 when the configuration was changed so that the output was 0x84(132) and the window extended from 0x7F(127) to 0x89(137). Table II shows the data for a threemonth period when the board was operating continually and there were no solar events. The SEUs are listed in bold. Whenever an SEU was detected, all six ADC outputs were recorded. For example, on 8/22/99 the SEU had a value of 0x43, whereas all the other undisturbed ADCs had values between 0x82 and 0x86, a range well within the window bracketing the digital output. The data also show that the undisturbed outputs vary little from one event to the next.

 TABLE II

 ADC OUTPUT READINGS WHEN SEUS (IN BOLD) WERE DETECTED ON MPTB.

Date	Out1	Out2	Out3	Out4	Out5	Out6
8/22/99	84	43	83	82	84	85
8/08/99	83	83	82	82	85	E5
8/06/99	8D	83	83	84	84	85
7/28/99	83	83	8E	82	85	86
7/25/99	84	83	82	82	8D	85
6/17/99	84	84	84	85	86	B5
6/14/99	84	84	84	82	8B	86

MPTB is in a highly elliptical orbit whose apogee (1,200 km) is below the radiation belts and whose perigee (39,200 km) is near geostationary orbit. MPTB's orbit inclination is 63°. The spacecraft completes two orbits in almost exactly one day (24 hours). Fig. 2 is a plot of the proton flux (energies greater than 38 MeV) during part of an orbit on 7/28/99. The plot also shows where the SEU occurred. The peaks in the proton flux occur when MPTB passes through the proton belts. That information is used to establish that the SEU occurred outside the radiation belts and is, therefore, due to a cosmic ray. Fig. 3 shows a similar plot for 8/22/99 and in this case the SEU occurs in the heart of the proton radiation belt.

A previous publication reported that the SEU rate measured for the AD9058 during "quiet time" before and after the solar particle event that occurred on  $5^{th} - 6^{th}$  November 2001 was 0.29 SEUs per device per day, or about 1 SEU per day for the whole board, which contains three devices. Those same calculations indicate that one third of the SEUs are due to cosmic rays and the remaining two thirds are due to tapped protons.

During the three-month period for which the digital output was 0x84, the solar activity was considerably lower than during the "quiet time" just prior to the Guy Fawkes Event. Associated with the lower solar activity was a doubling of the trapped proton flux as measured by CREDO as well as an increase in the cosmic ray flux. As a result, the SEU rate should increase to about 2 per day, so that over the threemonth period (June through August) the total number of SEUs should be about 180, a number significantly larger than the 7 actually observed.

One explanation for this disagreement is a reduction in the SEU sensitivity as a result of the new analog input voltage. Retesting the device with protons and heavy ions was not an option, so we opted to use a pulsed laser, which has the advantage of providing spatial information on SEUs.

An ADC was probed with the pulsed laser under conditions identical to those on board MPTB, i.e., the same digital outputs and window widths. Figs. 4, 5, 6, 7 and 8 show which



UT(Day from 1 January 1997)

Fig. 2. Proton Flux for an orbit for day 938 and location of SEU near geosynchronous orbit.



UT (Day from 1 January 1997)

Fig. 3. Proton flux showing that the SEU occurs in the proton radiation belt.

of the 128 comparators were SEU-sensitive for each configuration. The figures also give the values of the SEUs.

Careful measurements with the laser revealed that the energies needed to produce SEUs were the same for all comparators. From this result one can conclude that each comparator had the same LET thresholds for ion-induced SEUs. Therefore, the overall SEU cross-section is just the sum of all the contributions from the various comparators. This suggests that the variation in SEU sensitivity for different input voltages must be due to different numbers of sensitive comparators for the different input configurations.

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The data show that, in four of the five configurations, most of the comparators are sensitive to SEUs. The data also show that the digital values of the SEUs depend on which comparator is probed and on the magnitude of the analog input voltage. The number of insensitive comparator cells is different for each of the four input conditions, varying from 5 to 25. This should be reflected in the SEU cross-section, which should vary by about 20%. Such relatively small changes in the SEU cross-section are unlikely to be measurable, given the variability in the environment.

# E0 E1 E5 E1 E5 E1 E1 E3 E5 D1 D2 D3 D1 D3 <tdD3</td> D1 D3 D1</

Fig. 4. Digital outputs for SEUs in comparator cells for digital output of 0x11 and window (0x0f - 0x15). There are 5 unresponsive cells.

87	85	83	80	ø	86	86	87	80	8c	8a	89	87	85	83	81	81	84	8b	87	87	83	80	81	87	87	84	80	8e	8c	8c	87
80	85	87	80	æ	3	81	89	86	3	81	80	8	85	87	86	8	Be	8	81	83	85	87	81	83	85	87	89	8b	80	æ	87
4	40	40			40	41	40		ŧ	41	4	¥	40		L.		40	41	4	40	4		4	40	40	00				41	40
_		T	40	44	ă۵.	41			40					<b>—</b> —	40	-	-	41					4	44	4	4	40	41	41	41	

Fig. 5. Digital outputs for SEUs in each comparator cell for digital output 0x42 and window (0x42 - 0x4A). There are 25 unresponsive cells.

99	98	99	98	99	98	96	94	94	8C	8C	8D	8F	81	80	81	80	BC	BD	BD	8C	B1	BO	BO	81	B0	Að	A8	AB	A5	A5	A5
80	80	8t	8C	6C	8C	8	a	96	95	94	8	98	96	8	A4	AŞ	A\$	M	A9	A8	A8	AB	B1	80		BC	BD	물	BC	80	B1
70	70	70	7C	71		70	70	Γ.	66			00	00		59	58	3	58	55	54	54	54	Ð	¥	₽	ŧ	<del>\$</del>	Ŧ	40	41	40
70					68		70		71	70		7D	7D	7C		40	40	40	41	4C	40	₽	4F	2	55	55	5	58	58	58	58

Fig. 6. Digital outputs for SEUs in each comparator cell for digital output 0x63 and window (0x60 - 0x6A). There are 14 unresponsive cells.

ſ	87	86	86	83	80	BF	60	66	8F	ac	BA	84	86	86	83	80	BE	BF		BA	89	B7	85	83	<b>B</b> 7	89	BC		85	83		BF
t	83	85	86	69	8A	BC.	BF	89	84	ac	8F	80	83	85	86	BA	BC	BO	BF	80	83	B6	86	BO	83	85	86	89	BA	BC	BF	89
ľ	7F	_	00	00	73	73	80		1	<u> </u>	73	70	7E	7F			47	46	43	40	<b>4</b> F	4C	48	49	<b>4</b> F	40	4	8	46	45	0	40
ľ	_		_	7F	70	73	<b>—</b>		70	73					71	40	40	43	45	46	40	48	4D	4	40	40	40	40	43	43	46	æ

Fig. 7. Digital outputs for SEUs in each comparator cell for digital output 0x75 and window (0x72 - 0x7C). There are 18 unresponsive cells.

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Fig. 8. Digital outputs for SEUs in each comparator cell for digital output 0x84 and window (0x7F - 0x89). There are 128 unresponsive cells.

There is, however, one unique condition that confirms that the reduced SEU sensitivity of the ADCs when the input is 0x84 is due to all the comparators being SEU insensitive. Fig. 8 shows that for an input of 0x84 and a window from 0x7F to 0x89, none of the comparator cells is sensitive to SEUs. This lack of sensitivity was confirmed by testing the other ADC on the same chip. An attempt was made to see whether SEUs could be observed by reducing the size of the window. It was possible to reduce the window only slightly to cover the range from 0x80 to 0x88, but no SEUs in any of the comparator cells were detected. The window could not be reduced any further because of system noise.

The pulsed laser was used to scan for SEUs for other analog input voltages. The number of comparators insensitive to SEUs varied from one input configuration to another. One particular case, where the output value was 0x24 and the window extended from 0x1E to 0x27, is worth mentioning. Thirty out of the thirty-two cells in a single row were insensitive to SEUs.

Fig. 1 shows two vertical structures at the left end of the chip. The structure on the extreme left is believed to contain the eight output registers. The second vertical structure is believed to be the decoding circuit for converting from the Gray scale to binary. By probing all eight registers with the pulsed laser, we were able to establish that the five registers containing the five most significant bits were SEU sensitive for all configurations. The remaining three registers containing the three least significant output bits were not SEU sensitive because the window around the output masks any upsets produced in them. The decoding circuits feeding into those five output registers were also SEU sensitive.

Fig. 9 shows the values of the SEUs when the output registers and decoding circuits were probed with pulsed laser light. Comparison of the SEU values in figure 9 with those in Table II show that all the upsets that occurred in space were due to upsets in the output registers and decoding circuits. The only difference is for the case where the SEU in space had a value of 0x45 and in the laboratory a value of 0x43. That difference is due to noise in the system that affects the least significant bit.

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
45	E5	B5	9D	8D			

Fig. 9. Values of SEUs when the output registers were probed with the pulsed laser light. The blank entries indicate no SEUs when those bits were probed.

The values of the SEUs in the output registers are consistent with upsets generated in the various bits of the expected digital output (0x85). The binary representation of 0x85 is 10000101. Fig. 10 shows the expected value (in binary) in the first row and, in subsequent rows, the values obtained when different registers were irradiated with laser light. No SEUs were produced when the top three output registers were probed with laser light. When the fourth register from the top was irradiated, the "0" changed to a "1" and the value of the SEU was 0x8D. Irradiating the fifth register from the top caused upsets in bit #3 and bit #4, causing 10000101 to become 10011101 or 0x9D. Irradiating the bottom register caused SEUs in the two most significant bits and the digital output switched from 10000101 to 01000101 or 0x45. Inspection of the last column in the figure shows the hexadecimal values of the SEUs. They are the same as those observed in the data obtained from MPTB. This means that, in some case, the incident ion produced an SEU that caused more than one of the bits in the output to flip.

MSB	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB	HEX
1	0	0	0	0	1	0	1	85
1	0	0	0	1	1	0	1	8D
1	0	0	1	1	1	0	1	9D
1	0	1	1	0	1	0	1	B5
1	1	1	0	0	1	0	1	E5

0	1	0	0	0	1	0	1	45
							_	

Fig. 10. The top row shows the binary bits for the expected digital output of 0x85. The next row down shows a value of 0x8D, which was due to a single SEU in the third bit (bolded). Subsequent rows are for SEUs in other bits.

## IV. DISCUSSION

To understand why one value is far less sensitive than the rest, we needed to understand the operation of the device. Although the manufacturer was unwilling to provide us with any information, were obtained considerable information from patents obtained by the manufacturer. Using the information in those patents we were able to construct a model that we believe is fairly accurate of how the device operates.

We assumed that the "thermometer" encoding ROM stores values in Gray codes. Gray codes are a form of binary code where only one bit changes between any two consecutive numbers. The advantage of Gray codes is that the logical combination of two consecutive codes is typically much closer to the original values than the logical combination of two binary codes. The Gray codes are translated to ordinary binary values just before they reach the output registers. An XOR circuit was used to select the appropriate output word from the ROM.

Each comparator has two outputs that are inverted with respect to each other. Each output is used as input for two different interpolating latches. Thus, it is possible for an upset occurring in a comparator to affect two or three interpolating latches. Figure 11 is a simplified block diagram of the model used to analyze upsets in the AD9058 decoding circuitry.

Under normal circumstances, all of the outputs of the interpolating latches below a certain point would be one, and all those above the point would be zero. The result of this would be a single XOR gate turned on, which would select a single word from the ROM. When an error occurs in a comparator, there is the possibility of having multiple XOR gates turned on, and thus multiple output words from the ROM selected. The ROM output would be a logical combination of the selected words.



Fig. 11. Simplified schematic diagram of the ADC model, showing the comparators with differential outputs feeding into interpolating latches, followed by XOR gates, a ROM and decoding circuitry for converting from Gray code to binary.

To model errors in the decoding circuitry, we began by placing an expected thermometer code corresponding to an input code on the XOR inputs. We then toggled the value of each XOR input and recorded the binary outputs. For multiple bit upsets, we toggled two consecutive bits and recorded the output. The process was repeated for all 256 different possible input codes. For comparison, we also performed the same operation with the ROM storing raw binary outputs instead of Gray codes and using a combinatorial logic-decoding scheme similar to the 4-bit method illustrated in ref. [4].





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Fig. 13. Comparison of the simulated output codes with the measured codes presented in Figures 4,5,6 and 7. Blank spaces mean no error was recorded.

Figure 12 displays the number of sensitive comparators for each input code when the ROM used a Gray encoding and two consecutive bit upsets were simulated. It can easily be seen that there is a region around 171 that yields no sensitive comparators. Nearly identical results were observed for single bit upsets.

Figure 13 is a comparison of the output values on each comparator for four of the tested input values. The measured data are the same as those presented in Figures 4,5,6 and 7. The simulated data were obtained under the same conditions as the data in Fig. 12. The trends and values of the simulated data are in relatively good agreement with the measured data.

From the results presented, it is likely that the AD9058 utilizes a decoding scheme similar to the one shown in Fig. 11. The reason the measurements find an input value of 132 to have no sensitive comparators and simulations show an insensitive value centered around 171 is most likely due to the use of a different Gray code in the AD9058. The Gray code used in the simulation is not unique, and a variation of the code may have been implemented in the AD9058.

## V. CONCLUSIONS

From the results of this investigation comparing error rates in space with those calculated from limited ground based measurements one can draw a number of important conclusions.

First is that the LET threshold for SEUs in the AD9058 does not depend on input voltage as evidenced by same amount of energy required to upset each comparator.

Next, the spatial distribution and digital output values of the SEUs depend on the analog input voltage, as does the SEU cross-section, which can vary by more than an order of magnitude with analog input voltage.

Another important conclusion is that the pulsed laser can be used to measure the relative thresholds and SEU sensitive areas for the different inputs, thereby minimizing the amount of accelerator testing required. In fact, accelerator testing for a single analog input voltage is sufficient to characterize the SEU cross-section for all analog input voltages.

We caution that the results presented here are characteristic of the particular device tested and are not applicable to other implementations. However, unique effects that may affect the SEU sensitivity of other ADCs can also be unraveled using the pulsed laser.

Finally, when the SEU cross-section depends on input voltage, testing should be done with an agile input with sufficient SEUs to obtain statistically meaningful results.

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