The Space Technology 5 Avionics System

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Abstract— The Space Technology 5 (ST5) mission is a NASA New Millennium Program project that will validate new technologies for future space science missions and demonstrate the feasibility of building, launching and operating multiple, miniature spacecraft that can collect research-quality in-situ science measurements. The three satellites in the ST5 constellation will be launched into a sun-synchronous Earth orbit in early 2006. ST5 fits into the 25-kilogram and 24-watt class of very small but fully capable spacecraft. The new technologies and design concepts for a compact power and command and data handling (C&DH) avionics system are presented. [1,2]

The 2-card ST5 avionics design incorporates new technology components while being tightly constrained in mass, power and volume. In order to hold down the mass and volume, and qualify new technologies for future use in space, high efficiency triple-junction solar cells and a lithium-ion battery were baselined into the power system design. The flight computer is co-located with the power system electronics in an integral spacecraft structural enclosure called the card cage assembly. The flight computer has a full set of uplink, downlink and solid-state recording capabilities, and it implements a new CMOS Ultra-Low Power Radiation Tolerant logic technology.

There were a number of challenges imposed by the ST5 mission. Specifically, designing a micro-sat class spacecraft demanded that minimizing mass, volume and power dissipation would drive the overall design. The result is a very streamlined approach, while striving to maintain a high level of capability. The mission's radiation requirements, along with the low voltage DC power distribution, limited the selection of analog parts that can operate within these constraints.

The challenge of qualifying new technology components for the space environment within a short development schedule was another hurdle. The mission requirements also demanded magnetic cleanliness in order to reduce the effect of stray (spacecraft-generated) magnetic fields on the science-grade magnetometer.

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[2] IEEEAC paper #1514, Version 1, Updated October 21, 2004

1. INTRODUCTION

This paper describes the functions, interfaces, components, designs and new technologies for the Space Technology 5 (ST5) integrated avionics system. In order to put the avionics design into perspective, the paper starts with an overview of the ST5 mission and a review of the new spacecraft technologies that will be flight-validated by ST5. Following that, there is an introduction to the spacecraft's external geometry and location of internal components, with a discussion of the spacecraft's two-slot "card cage" assembly that houses the power system electronics (PSE) circuit board, and the command & data handling (C&DH) electronics circuit board. The physical locations of the various subsystems and the structural nature of the card cage assembly leads into a more in-depth presentation of how the mechanical and magnetic requirements drove the topology used for power distribution and electrical signal flow. The details of the power system design are then given in terms of the solar arrays, lithium-ion battery, power system electronics and architecture for regulation and switching. The details of the C&DH design are given in terms of its external signal interfaces for data acquisition and control, followed by the architecture for the processor, memory and gate arrays. The progress and current status of the flight hardware development, integration and testing effort are presented, with a look at how multiple flight units have been processed in parallel under very challenging schedule and manpower constraints. A discussion of the challenges met and lessons learned by the avionics team precedes the paper's conclusion, and a list of acronyms appears at the end for easy reference.

2. ST5 MISSION & TECHNOLOGY OVERVIEW

The Space Technology 5 mission is serving as a multi-functional stepping-stone for future missions. As a part of NASA's New Millennium Program (NMP), one key requirement for the ST5 mission is to validate new breakthrough technologies for exploring the space environment. Another important goal is the development of a small but fully capable spacecraft that can operate either as a stand-alone science probe or as part of a larger constellation to gather in-situ magnetospheric science data. The streamlined 25 kg spacecraft bus demonstrated by ST5 is an intermediate step towards a future nano-satellite goal of a full service scientific spacecraft weighing less than 10 kg. The three spacecraft in the ST5 constellation will be launched into polar elliptical Sun-synchronous orbits by a Pegasus XL launch vehicle from Vandenberg AFB. The "string of pearls" orbits will have a period of about 136 minutes, a perigee distance of about 300 kilometers and an apogee distance of about 4500 kilometers. After separation from the launch vehicle, the spacecraft spin rates will all be about 20 revolutions per minute. The nominal mission duration is three months.

ST5 mission requirements include the validation of several NMP technologies that are focused on the small and low-power theme. Among these are: a lithium-ion battery, a cold gas micro-thruster (CGMT), a miniature X-band transponder, two different variable emittance (thermal) controllers (VECs), and an ultra-low power, radiation-tolerant 1/2 volt CMOS logic technology. The validation plan for each new technology includes space qualification of the hardware followed by monitoring and analysis of the in-flight performance data. The technologies validated by ST5 will enable future NASA science missions and reduce the risk for those missions. Some other features on the ST5 spacecraft that are not formally considered to be NMP technologies are the triple junction photovoltaic solar cells, the low voltage (+7.2 V nominal) power bus, the very small but high-resolution magnetometer, the miniature sun sensor and the all-passive thermal control system.

Some of the biggest challenges imposed on the ST5 team were the constraints on the spacecraft mass (25 kg), volume and available power (24 watts). While these parameters are always major drivers behind the design decisions on any spacecraft, the level of the ST5 limits was so low that some features could not be included in the design. Some higher levels of performance had to be sacrificed in order to hold the mass, volume and power to a minimum. For example, where it would be typical to utilize a switching converter for optimum DC-to-DC power conversion efficiency, there would be a mass and volume penalty to incorporate the switching approach for every design. Instead, a very low drop-out regulator was used for the smaller power loads, while a switching converter was used for a larger load. Design tradeoffs like this one were applied throughout the early stages of the power system design and flight computer design in order to maintain a balance between the mix of nano-satellite requirements on the spacecraft avionics solution.

Originally, ST5 was to be launched into a highly elliptical geo-stationary transfer orbit. The predicted radiation environment was 100 kilorads total ionizing dose over an extended mission lifetime. This environment, in addition to the low supply voltage (+5V) for many of the components, limited the selection of electronic parts that could be used in the analog circuits. Although the radiation tolerance of the ST5 design is now higher than that necessary for the new lower altitude orbit, the design is robust enough to be used for future missions planning to operate from low voltage power busses in fairly high radiation environments.

3. ST5 Spacecraft Overview

Each of the three spacecraft (S/C) in the ST5 constellation will be identical. The basic shape of each S/C is roughly like an 8-sided flattened cylinder, approximately 20 inches (51 centimeters) in diameter and 11 inches (28 centimeters) tall. The total mass for each spin-stabilized vehicle is 25 kg, and the power budget for each is about 24 watts. The spacecraft spin axis is the axis of symmetry or axis of rotation of the 8-sided cylinder. The main science instrument is a small, low-power, high-resolution magnetometer (MAG) that will make in-situ measurements of the Earth's magnetic field throughout each orbit. The 3-element ST5 constellation is anticipated to be a proof-of-concept for later magnetospheric constellation missions where many miniature science probes will be able to take simultaneous measurements of a complex field that is both temporally and spatially dependent. A deployable MAG boom will position the magnetometer's sensor head about one meter away from the center of the S/C. This boom is stowed or "folded" during launch and ascent, and then deployed after the S/C is spun up to about 20 revolutions per minute (RPM) as it separates from the Pegasus launch vehicle.

Figure 1 gives an "in-space" view of the three ST5 satellites, showing the 8-sided flattened cylinder shape, the MAG sensor head out at the end of a deployed boom, and three of the eight solar array panels on each spacecraft.

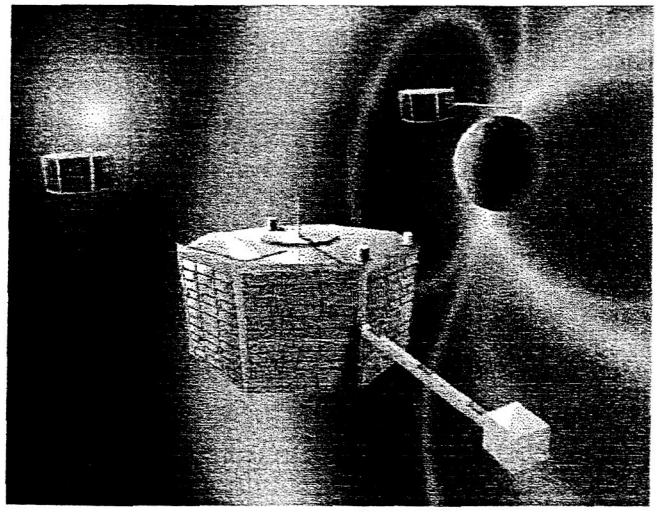

Figure 1: In-Space View of the ST5 Constellation

The flat top and bottom surfaces of the 8-sided cylinder, called the top and bottom "decks", are octagons. There are eight small solar panels covering the outsides of the eight side walls of the cylinder. A rectangular "brick-shaped" card cage assembly (CCA) mounts in between the top and bottom decks and joins the two decks together. The longest dimension of the card cage assembly is slightly less than the diameter of the S/C. Mounted inside the 8-sided flat cylinder's volume are a number of subsystems and components, including the battery, the cold gas micro-thruster, the cold gas propellant tank and the small electronics boxes for the NMP technologies, the magnetometer, the sun sensor, the thruster controls and the tank pressure transducer.

Figures 2 and 3 show two views of the physical geometry and location of components for each ST5 spacecraft. Figure 2 is a "top-down" view of the vehicle, looking down onto the octagonal top deck, with the MAG boom in the deployed position. This simplified diagram shows the approximate size and position of the various components and electronics boxes, but the length of the MAG boom is not to scale. Edge-on views of two of the eight solar panels are seen on the left and lower left sides of the octagonal deck.

The 2-slot CCA box encloses the command and data handling (C&DH) board and the power system electronics (PSE) board. The CCA serves as the major structural element connecting the top and bottom decks, and it splits the interior volume of the spacecraft into two halves. The card cage also serves as the main heat conduction path from the C&DH and PSE boards out to the two decks. Figure 3 is a "side" view of the vehicle, showing the top and bottom decks edge-on, with the card cage assembly between them.

4. Power and Signal I/O Topology

The magnetometer on board each of the ST5 spacecraft will be making precise 3-dimensional measurements of the vector field local to each spacecraft. The MAG data will also be used as part of a ground-based attitude determination algorithm. The magnetometer is very sensitive, and because the MAG sensor head is mounted on the end of a relatively short boom, it is possible that the MAG could sense the magnetic field generated by the spacecraft itself. In order to prevent this, or at least minimize the magnetic field generated by the spacecraft, a stringent magnetic field control plan was adopted.

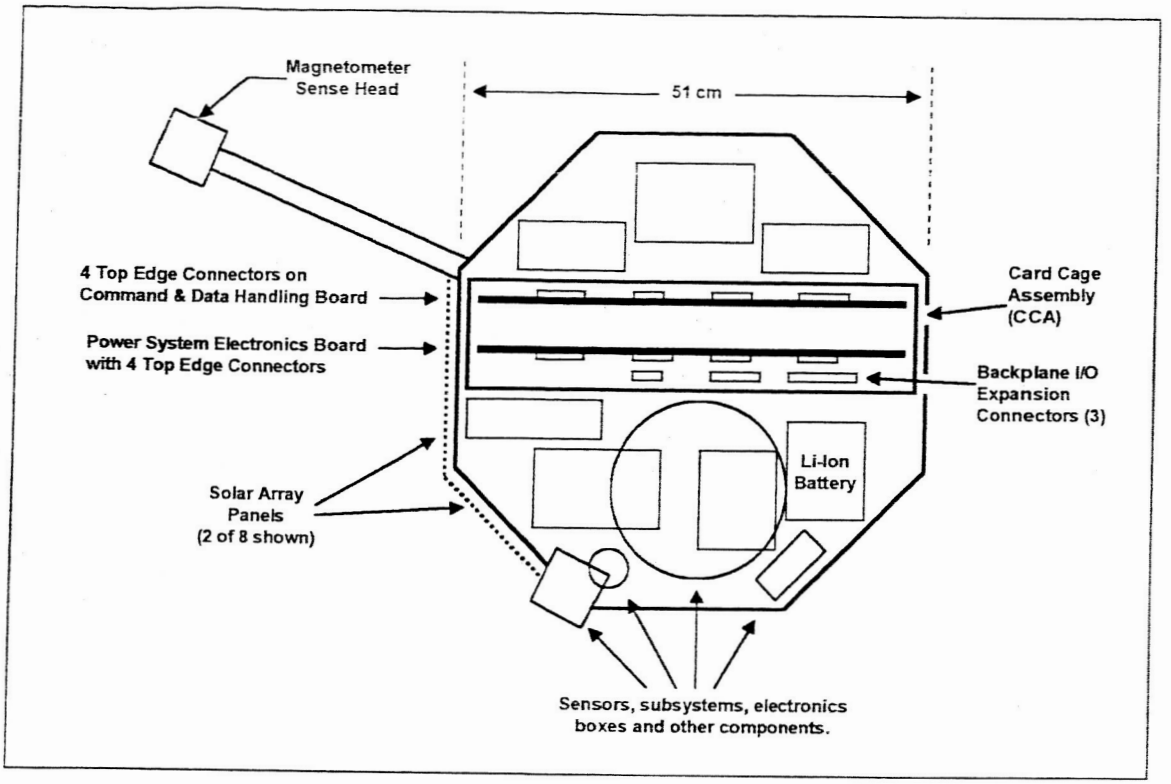

Figure 2: Top-Down View of ST5 Spacecraft Structure and Component Locations

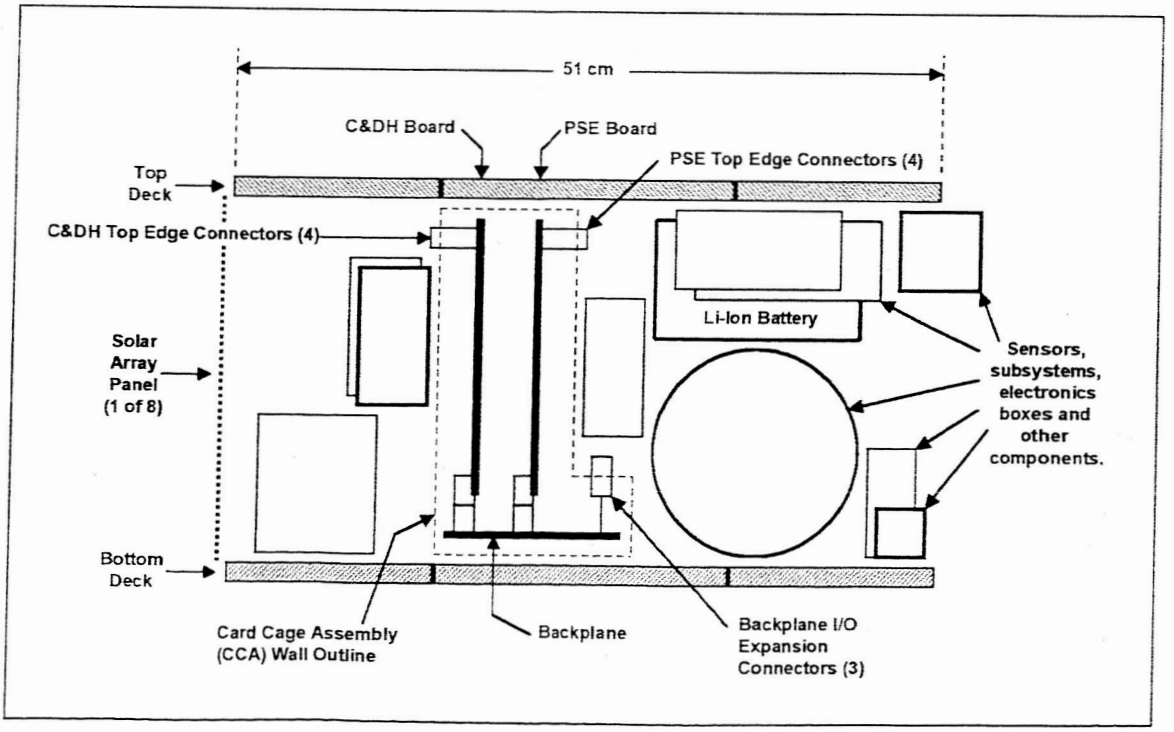

Figure 3: Side View of ST5 Spacecraft Structure and Component Locations

The ST5 "magnetic cleanliness" requirements dictated: 1) that the use of magnetic materials be severely restricted, 2) that packaging and power/signal routing decisions be made to reduce or eliminate the fields created by currents flowing in loops, and 3) that some capability be provided for doing magnetic field compensation (if required). To minimize any current loop areas, the lines for power distribution were twisted together and the solar arrays were wired to cancel magnetic fields.

To ease the overall power/signal routing task as much as possible, connectors were located along the top edge of the PSE board for the "PSE side" subsystems (like the battery). Likewise, for the "C&DH side" subsystems, there are connectors located along the top edge of the C&DH board. For inter-board communications between the PSE and C&DH there is a backplane mounted in the bottom of the CCA. For some interfaces between the CCA and subsystems on the "PSE side" of the spacecraft there are three backplane I/O expansion connectors. These are all shown in Figures 2 and 3.

The PSE provides the regulated +5.0V power to the C&DH through a backplane connector. The PSE also sends dedicated analog signals to C&DH (through the same backplane connector) that are used to measure bus and battery voltages and currents. In addition, there is a multiplexed analog output signal from PSE to C&DH that is used to monitor other power system health and status telemetry.

Figure 4 summarizes the I/O topology for the signal and power lines going to and from the CCA box. The large bold-lined rectangle represents the CCA box containing the C&DH board, the PSE board and the backplane. Power distribution from the PSE is indicated by solid-line arrows, while signal distribution to and from the C&DH is indicated by dashed-line arrows. This topology for power and signals provided for simplified point-to-point spacecraft harnessing (in many cases) and easier integration and testing.

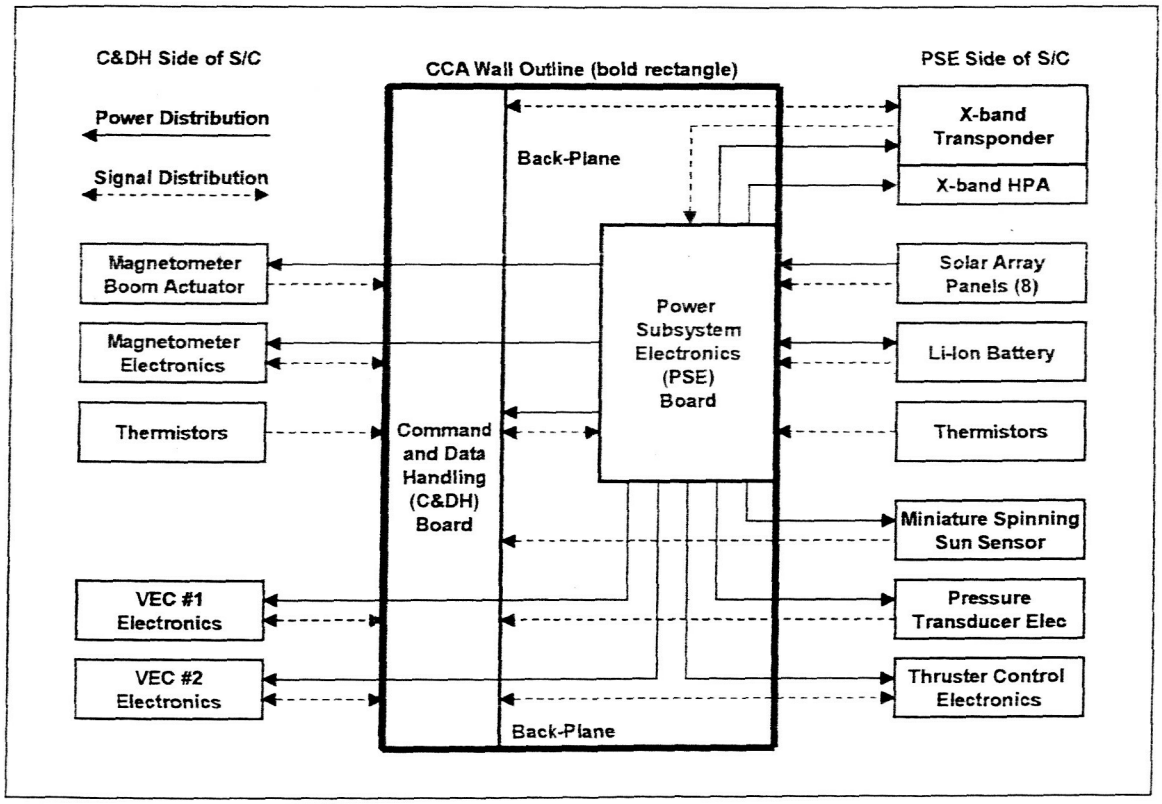

Figure 4: Power and Signal I/O Topology through the Backplane

5. POWER SYSTEM DESIGN & TECHNOLOGIES

The main functions of the power system are to collect energy from the eight solar array panels, store any excess solar energy in the lithium-ion battery, draw stored energy from the battery when needed, and provide switched power outputs (with on/off control) to the S/C subsystems. Key elements of the power system architecture are the low voltage busses (+5.25V regulated and +7.2 ± 1.2V unregulated) along with components that achieve very low power consumption and dissipation. A low voltage DC bus was selected in order to minimize conversion and regulation losses. Since most of the spacecraft electronics (about 90%) are digital and operate from an input voltage of around +5V, and since all of the components are in close proximity (less than 12 inches from any CCA wall), a +5.25 Volt power bus was chosen. A higher voltage bus (+7.2 V) was added for components that can improve their efficiency when operating from a higher voltage (e.g., the transponder's RF high power amplifier or HPA).

5.1 Solar Arrays and Battery

The solar array is comprised of eight body-mounted panels. The solar cells are triple-junction GaAs cells and have an average efficiency of 28%. At beginning of life, power generation by the solar array will be just over 26 watts. There are temperature sensors on two of the eight panels. A battery is needed to power the S/C during eclipses (if any), and due to growth in the load power demanded by the spacecraft and the limited solar panel area available around the sides of a small vehicle, the battery will be used to supplement the solar arrays during peak load conditions in sunlight. Periods of peak power demand are expected to be during X-band downlink passes when the HPA is on.

The 7.5 amp-hour lithium-ion battery is a new technology on the ST5 mission. It provides for an increase in energy density of 2-3 times over nickel cadmium batteries, thus helping our mass and volume allocations. Along with the increase in energy density, this battery technology allows for a simplification in battery charge management circuitry. Constant current charging is no longer required and the voltage and temperature management is greatly simplified. In addition, the selection of low amp-hour cells in the battery has allowed for further reduction of battery charge control circuitry compared to that required for larger lithium-ion cells. The smaller cell sizes do not really need individual cell balancing and cell level charge control electronics. For ST5, we are simply using battery level charge control measures. The reduction in the electronics area simplifies the design and testing and is consistent with our mass and volume constraints. The individual battery cells have an end-of-charge voltage of +4.2V each, with a capacity of about 1.25 amp-hours at a C/5 discharge rate, to a voltage of +6.0V. A total of twelve cells are wired with groups of six cells in parallel, and two groups wired in series to achieve a nominal +8.4V output. Figure 5 is a picture of the battery, with a one inch scale in the foreground.

Figure 5: Photograph of ST5 Lithium-Ion Battery

5.2 Power System Electronics

As described previously, the PSE maintains an un-regulated +7.2 ± 1.2V power bus and a regulated +5.25V power bus. These two low-voltage busses are shown in the simplified power system block diagram (Figure 6). Power distribution is accomplished with digitally command-able and reset-able solid-state power switches. Each power switch has a digital command and status interface as well as an over-current protection circuit integrated into a small package. The "circuit breaker" function is activated when an over-current condition is sensed. The current level for the over-current trip function is adjustable for each load and is fixed prior to launch. The default state of a switch (after initial start-up) can be either on or off. The design of this hybrid switch was done in-house at Goddard and has passed flight qualification testing.

As shown in Figure 6, there are five switch-able +7.2V un-regulated outputs. The +7.2V power to the transponder's X-band uplink receiver is not switch-able; it is always on when the spacecraft is on. A DC-to-DC converter provides regulated +5.0V power to the flight computer (C&DH board). The +5.0V power to the C&DH is always on, but it can be momentarily cycled on-off-on by a ground-to-transponder "special command" if necessary. At the bottom of the figure are the four switch-able +5.25V regulated outputs. All of the PSE board's solid-state power switches are controlled by the C&DH processor via read/write transactions over the backplane's local 16-bit parallel data bus.

In order to produce a miniature power system and improve its efficiency, the system's functions were combined and streamlined. The same circuitry that regulates the solar array voltage also operates as a battery charger. The dual role is performed by a pulse width modulated boost converter which regulates to a fixed voltage clamp. The voltage clamp is set for the optimum end-of-charge voltage of the lithium-ion battery and provides overcharge protection. Battery over-discharge protection is provided by the flight software resident in the spacecraft computer. Analog battery health and status signals are digitized and monitored by the flight software. If the battery falls below a pre-determined depth of discharge, a flight software load-shedding algorithm is initiated to reduce demand on the battery.

Note that the ST5 spacecraft is NOT powered on during launch and ascent. Upon separation from the launch vehicle, a power system enable switch will close and the spacecraft will turn on. For integration and test (I&T) purposes there is a battery off-line switch that prevents even small amounts of leakage from the battery when the S/C is powered off for extended periods of time. Also for I&T, the PSE has an externally accessible connector for supplying ground power, charging the battery, and directly measuring the power system's health and status signals.

The PSE board mass is approximately 2.1 kg, and its power consumption is about 0.9 watts. Figure 7 is a photograph of the A side of the PSE board assembly.

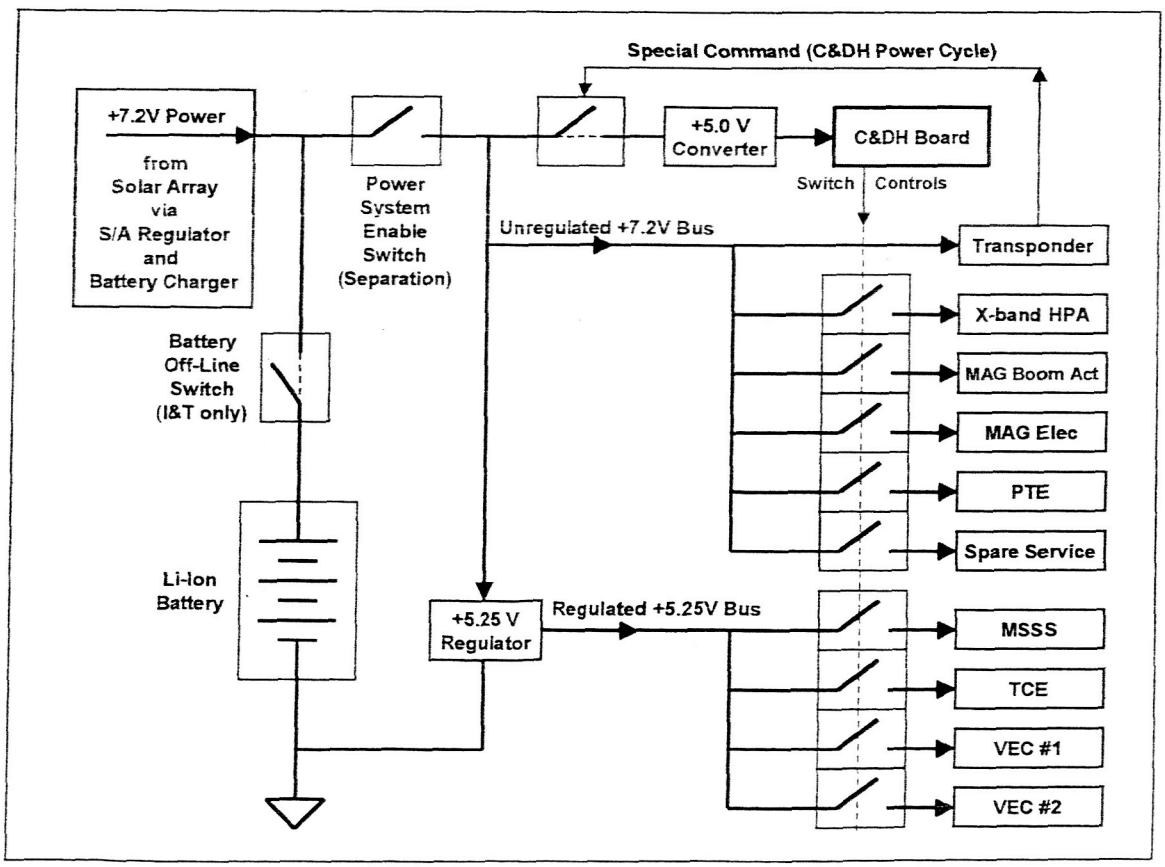

Figure 6: ST5 Power System Block Diagram

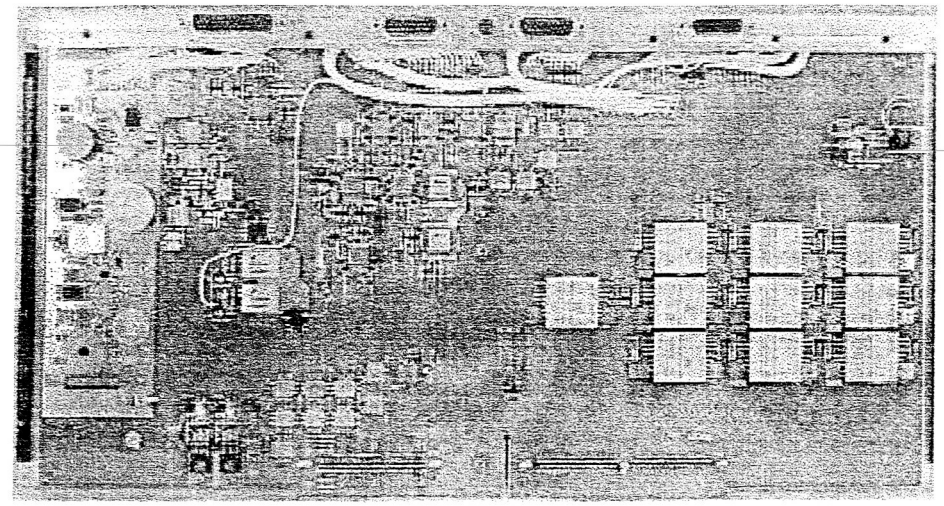

Figure 7: Photograph of PSE Board (side A)

6. C&DH DESIGN & TECHNOLOGIES

The C&DH board (flight computer) interfaces to all other spacecraft subsystems, and it performs all of the data collection and processing functions for on-board attitude control, science measurements and bulk data storage, NMP technology validation, housekeeping, and ground communications for command uplink and telemetry downlink. The NMP technology for CMOS ultra low-power radiation-tolerant (CULPRiT) logic will be validated in a Reed-Solomon encoder chip. The C&DH can select (and compare the results) between a conventional +5V Reed-Solomon encoder and the CULPRiT encoder in order to do forward error correction on the telemetry downlink. The 1/2 volt CULPRiT technology is latch-up immune and hardened for up to 100 kilorads of total ionization dose, with a single event upset LET threshold of approximately 20 MeV-cm^2/mg. The PSE provides regulated +5.0V power to the C&DH board, where linear regulators on the C&DH are used to derive the required +3.3V and +2.5 volt supplies. The CULPRiT chip requires a +0.5V logic supply.

6.1 External Interfaces & Functions

Referring back to Figure 4, there are dashed lines for all of the C&DH signal interfaces. The C&DH signals to and from the X-band transponder are for uplink and downlink, control and monitoring of the internal operation of the transponder, and sensing temperatures and other analog parameters inside the transponder. Uplink commands are sent to the C&DH over a serial interface at 1 kbps. Downlink telemetry goes to the transponder over a separate serial interface that can run at either 1 kbps or 100 kbps. The C&DH has another pair of 1 kbps serial data links to allow for transponder configuration control and allow digital status readout from inside the transponder. A hardware-decoded "special command reset" signal goes from the transponder to the PSE in order to cycle the C&DH power on-off-on and reset the spacecraft processor.

When the sun passes through the field-of-view of the sun sensor, the C&DH will sample the time and the sun elevation angle bits from the sensor. The C&DH can also monitor the MSSS electronics temperature.

For the "cold gas" propulsion system, the C&DH will collect telemetry for tank temperature, tank pressure, CGMT temperature and TCE temperature. For attitude control and validation of the NMP micro-thruster technology, the thruster on-off control pulses can be synchronized to either the S/C rotation or an on-board 2 Hz clock. For adjusting the orientation of the spin axis the pulses are phased with respect to the S/C rotation. For delta-V maneuvers the pulses are phased with respect to the 2 Hz clock.

The C&DH can sense the temperatures of the MAG boom actuator, the MAG electronics and the MAG sensor head. From the MAG electronics, the C&DH receives science data on a 2 kbps serial interface, with samples of the magnetic vector field arriving continuously at 16 Hz. The C&DH also gets an analog telemetry signal for MAG total current.

For the two VEC technologies, there are digital control and status signals, as well as two temperatures for each VEC. The C&DH also collects information on sixteen different analog parameters from inside each VEC over a single time-multiplexed analog signal line.

Additional internal and external telemetry signals that are sampled and digitized by the C&DH include voltages and currents for the +5.0V supply, the +3.3V supply, the +2.5V supply and the +0.5V CULPRiT encoder supply. Also monitored are the temperatures for the C&DH processor and 24 MHz oscillator, CULPRiT encoder, spacecraft top and bottom decks, the two CCA side walls and the nutation damper.

All of the analog voltage, current and temperature telemetry signals that are collected from all over the spacecraft will funnel down through a network of analog multiplexers to an analog-to-digital converter on the C&DH board. An autonomous FPGA-based analog telemetry collection system will perform all of the low-level micro-operations associated with selecting each analog signal, converting it to digital form and storing the result in memory.

6.2 Processor and Memory Architecture

Figure 8 is a simplified block diagram of the ST5 processor and memory architecture. The board design is centered around a single Mongoose 5 radiation-hardened 32-bit processor. The C&DH design uses a variety of memory types, and has a full set of registers for data acquisition and control functions. There are 2 megabytes of electrically erasable programmable read-only memory (EEPROM) for non-volatile program storage. There are 32 megabytes of dynamic random access memory (DRAM) that are divided up between processor code and data storage, and space for solid-state recording of spacecraft telemetry between downlink passes. For faster program execution, the code in EEPROM will be copied into DRAM after processor start-up. To compensate for single event upsets, the processor and DRAM utilize an error detection and correction (EDAC) algorithm that can correct any single bit errors and detect multi-bit errors. The hardware design also has a small static random access memory (SRAM) for automated collection of magnetometer science data and analog housekeeping telemetry.

Many of the C&DH logic functions are incorporated into three Actel RT54SX32S Field Programmable Gate Arrays (FPGA). The Processor FPGA handles top-level address decoding, DRAM refresh and various timer functions. The Transponder FPGA will perform all of the operations associated with decoding uplink commands and encoding downlink telemetry. Buffering of downlink data packets will be done by a first-in-first-out (FIFO) memory that can be block-filled by flight software while the data simultaneously trickles out through the transponder FPGA.

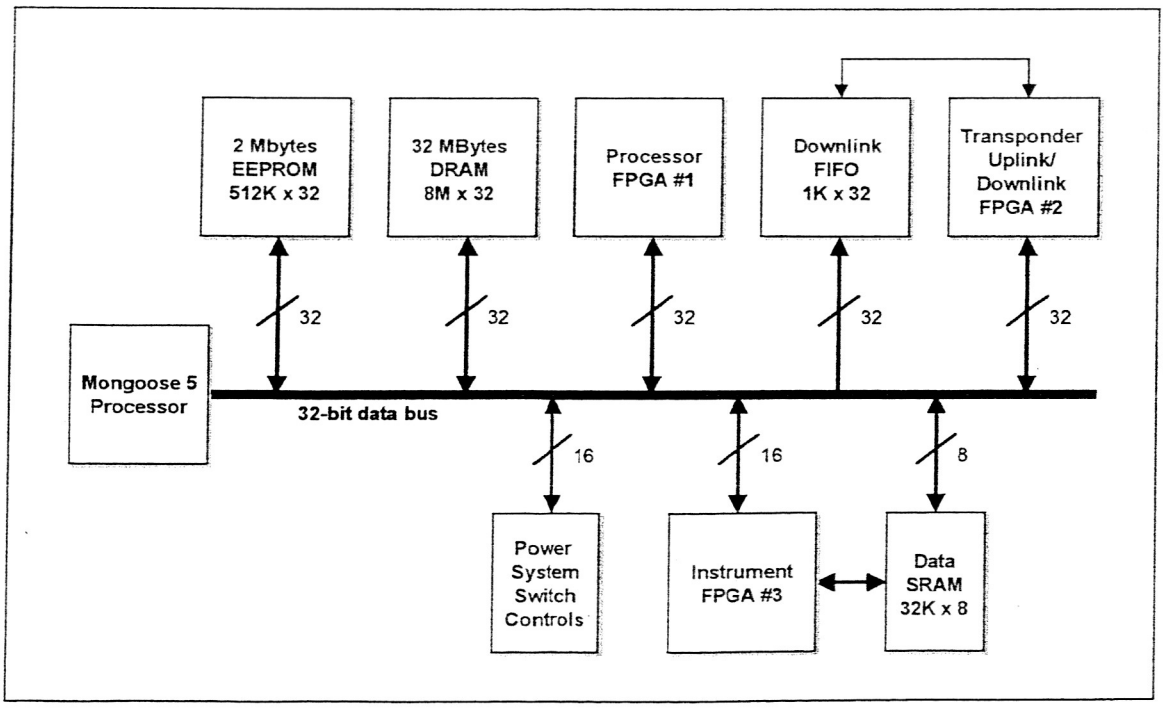

Figure 8: Block Diagram of C&DH Processor and Memory Architecture

The Instrument FPGA is responsible for the data acquisition and control interfaces with the sun sensor, micro-thruster, magnetometer and VEC technologies, and the automated collection of analog telemetry data from all over the spacecraft.

The processor, EEPROM, FIFO, FPGAs and conventional Reed-Solomon encoder use the +5.0V supply directly. The DRAM uses the +3.3V supply and the FPGA cores need the +2.5V supply. There is an externally accessible C&DH direct access test connector for memory loading, hard-line (base band) serial uplink and downlink, built-in test and debug functions, etc.

A highly automated architecture and use of dense electronic components allowed for a single processor, single board C&DH solution with a total power consumption of only 3.6 watts and a mass of about 2.2 kg. Figure 9 is a photograph of the A side of the C&DH board.

The PSE and C&DH boards are designed to be single event latch-up immune, with radiation hardening for up to 40 kilorads of total ionization dose and a single event upset LET threshold of 35 MeV-cm^2/mg. The required electronics operating temperature range is –20°C to +50°C.

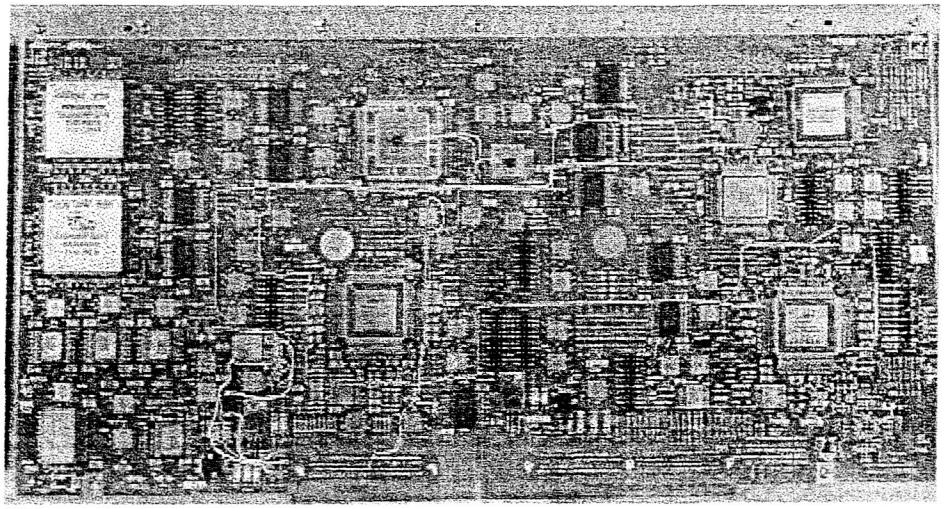

Figure 9: Picture of C&DH Board, Side A

7. INTEGRATION & TEST STATUS

Following board-level checkout and functional testing of the individual PSE and C&DH breadboard units, a short wiring harness version of the backplane was used to electrically integrate the two breadboard units together. Extensive hardware and software testing was then done using ground support equipment (GSE) electrical interface and data/signal simulators for all of the components and subsystems external to the CCA box. Thermal margin testing (under ambient pressure conditions) was also performed on the PSE and C&DH breadboards independently.

Four sets of PSE, backplane and C&DH flight units have been built in a time-staggered sequence, one set for each of the three ST5 spacecraft and one spare set. Each PSE and C&DH flight unit initially went through acceptance tests at the board-level, where a PSE breadboard was used to power a C&DH flight unit. For the final series of box-level qualification tests, the PSE and C&DH flight units were integrated into a flight CCA box with a flight backplane. Full functional tests were then performed at ambient temperature, at –30°C and at +60°C.

Flight CCA box #1 has been through thermal cycle testing, conducted electro-magnetic interference (EMI) testing and 3-axis vibration testing, and is currently in the very last stages of spacecraft-level integration with the first set of flight structures, components and subsystems. Flight CCA boxes #2 and #3 will undergo full qualification testing at box-level, including: conducted and radiated EMI testing, vibration testing and thermal-vacuum testing during late 2004 and early 2005. Integration and comprehensive performance testing of the three spacecraft will continue into 2005, with launch planned for March 2006.

8. Challenges and Lessons Learned

Two of the early avionics design challenges were to achieve very low power consumption and fit inside the allocated board area. The total power dissipation for the ST5 avionics (PSE and C&DH boards combined) is under 5 watts, well below the initial requirement of 8 watts. Both boards were able to meet the area requirements derived from the mechanical dimensions of a 2-slot card cage enclosure that also serves as an integral part of the spacecraft structure.

A significant amount of up-front systems engineering time was invested in working out the board/box packaging concept, evaluating various power and signal I/O topologies and preparing hardware-software interface documentation.

Instead of building engineering test units (ETU), there were high-fidelity breadboards with flight-like parts packages, flight-like board area constraints and external electrical connector interfaces that would be the same as flight. This approach allowed us to measure (rather than estimate) board area and power consumption, re-use GSE harnesses and debug some flight I&T procedures on the breadboards. Only one CCA connector (out of 14) was changed between the breadboards and the flight units.

A high quality set of loadable diagnostics software was crucial to rapidly trouble-shooting C&DH problems. It was also important to have basic memory and register I/O functions included in the early versions of flight software. With an uplink and downlink to and from the flight software, test procedures were much more automated.

The hardware and software test and debug processes were streamlined by liberal use of built-in design for testability, including on-board test headers and test pads for critical signals. Functional groups of signals were multiplexed out from the insides of an FPGA so that a number of key subsystem interfaces could be viewed (while operating) at a dedicated test connector.

A thorough inspection process at the board manufacturing site helped to resolve minor issues before the start of powered testing in the lab. Inspection of operating flight assemblies with a thermal infra-red camera is highly recommended for any space avionics development flow.

9. Conclusion & a Look to the Future

A compact, low-power single-box avionics design has been done at Goddard Space Flight Center to meet the requirements for the ST5 technology validation and nano-sat constellation trailblazer mission. Three identical 25 kg spacecraft are being developed, with integration and testing during calendar years 2004 and 2005, and a Pegasus XL launch into a polar sun-synchronous orbit in March of 2006. ST5 will show that multiple spacecraft can operate together as a single constellation, and that a very small spacecraft is capable of research-quality science measurements.

The ST5 satellite will use low-voltage DC power distribution, from either an unregulated +7.2V bus or a regulated +5.25V bus, with a total available power of about 24 watts. The thermal control system is all-passive. A single-processor, multi-function flight computer will implement direct digital and analog signal interfaces to all spacecraft subsystems and components. Flight software running on this processor will be responsible for the entire spectrum of real-time tasks associated with: power switching, attitude and orbit control, uplink and downlink, science data acquisition and storage, and housekeeping data collection and logging.

As part of NASA's New Millennium Program, the ST5 design is demonstrating a number of new technologies including: a lithium-ion battery, a miniature low power X-band transponder, a cold gas micro-thruster, two different variable emittance (thermal) controllers and a CMOS ultra low-power radiation-tolerant +0.5 volt logic chip. ST5 will also apply advanced components such as triple-junction solar cell arrays, a miniature spinning sun sensor and a science-grade magnetometer. The high sensitivity of the magnetometer was a significant design driver, because magnetic materials and electrical current flow topologies could generate magnetic fields at the nano-Tesla level. This is especially true for a very small S/C where the magnetometer's sensor head could not be placed at the end of a boom that was many meters long.

The ST5 team has made significant progress towards the goal of revolutionizing our ability to do multi-point in-situ scientific investigations as part of the roadmap for future Sun-Earth Connection nano-sats. On ST5 a single avionics box will perform the power conditioning and distribution, data acquisition and control, communications, processing and storage requirements that have traditionally required a larger network of separate circuit boards and/or avionics boxes. For these reasons the ST5 bus design has been baselined as the starting point for a low cost Magnetospheric Constellation – Dynamic Response And Coupling Observatory (MC-DRACO) mission, with approximately 30 satellites in the constellation.

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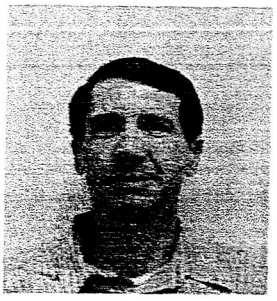
10. ACRONYM LIST

AFB	=	Air Force Base
CCA	=	Card Cage Assembly
CGMT	=	Cold Gas Micro-Thruster
C&DH	=	Command & Data Handling
cm	=	centimeters
CMOS	=	Complimentary Metal Oxide Semiconductor
CULPRiT	=	CMOS Ultra Low-Power Radiation-Tolerant (logic technology)
DC	=	Direct Current
DRAM	=	Dynamic Random Access Memory
EDAC	=	Error Detection and Correction
EEPROM	=	Electrically-Erasable Read-Only Memory
EMI	=	Electro-Magnetic Interference
ETU	=	Engineering Test Unit
FIFO	=	First In First Out (buffer memory)
FPGA	=	Field Programmable Gate Array
GaAs	=	Gallium Arsenide
GSE	=	Ground Support Equipment
GSFC	=	Goddard Space Flight Center
HPA	=	High Power Amplifier
Hz	=	Hertz
I/O	=	Input/Output
I&T	=	Integration and Test
JPL	=	Jet Propulsion Laboratory
kbps	=	kilobits per second
kg	=	kilogram
MAG	=	Magnetometer
MHz	=	MegaHertz
MSSS	=	Miniature Spinning Sun Sensor
NASA	=	National Aeronautics and Space Administration
NMP	=	New Millennium Program
PSE	=	Power System Electronics
PTE	=	Pressure Transducer Electronics
RF	=	Radio Frequency
RPM	=	Revolutions Per Minute
RS	=	Reed-Solomon
S/A	=	Solar Array
S/C	=	Spacecraft
SRAM	=	Static Random Access Memory
SSR	=	Solid State (data) Recorder
ST5	=	Space Technology 5
TCE	=	Thruster Control Electronics
VEC	=	Variable Emittance Controller

11. BIOGRAPHIES



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