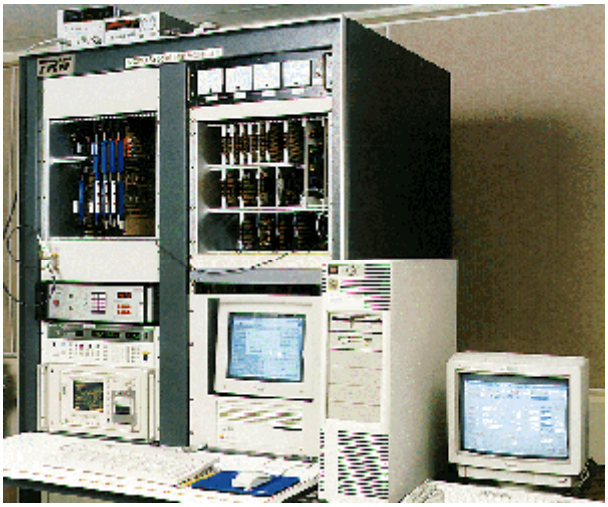
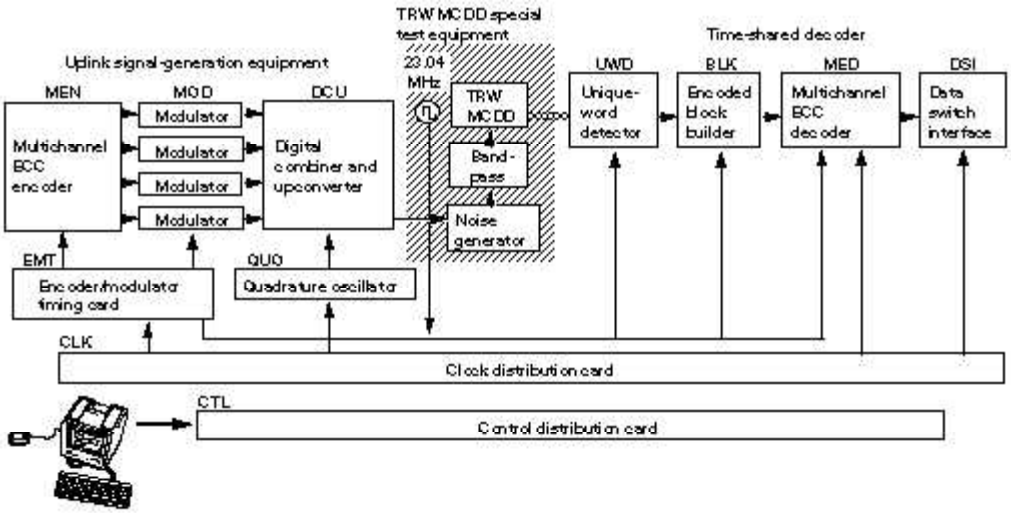
Multichannel Error Correction Code Decoder



Uplink signal-generation equipment and time-shared decoder.

NASA Lewis Research Center's Digital Systems Technology Branch has an ongoing program in modulation, coding, onboard processing, and switching. Recently, NASA completed a project to incorporate a time-shared decoder into the very-small-aperture terminal (VSAT) onboard-processing mesh architecture. The primary goal was to demonstrate a time-shared decoder for a regenerative satellite that uses asynchronous, frequency-division multiple access (FDMA) uplink channels, thereby identifying hardware and power requirements and fault-tolerant issues that would have to be addressed in a operational system. A secondary goal was to integrate and test, in a system environment, two NASA-sponsored, proof-of-concept hardware deliverables: the Harris Corp. high-speed Bose Chaudhuri-Hocquenghem (BCH) codec and the TRW multichannel demultiplexer/demodulator (MCDD). A beneficial byproduct of this project was the development of flexible, multichannel-uplink signal-generation equipment.

The multichannel ECC decoder (MED) system is a prototype of the uplink portion of a low-rate (64 kbps) FDMA satellite for a mesh VSAT processing satellite. As shown in the schematic, the MED consists of a bit-error-rate test set, uplink signal-generation equipment, the TRW MCDD (including radiofrequency and link-simulation equipment), and the time-shared decoder. The system can produce four uncoded or coded uplink channels at a channel transmission rate of 64 kbps. The codec uses a BCH block code in block sizes of 224 to 480 bits excluding a 32-bit unique word preamble that identifies the start of a block.



Schematic of uplink signal-generation equipment and time-shared decoder.

This time-shared decoder has a very good potential for being applied in an onboard-processing circuit-switch environment because individual blocks of data can be processed and routed as soon as a full data block is available. Thus, the amount of storage memory required onboard is reduced. For applications to a packet switch in an asynchronous FDMA environment, the time-shared decoder system would have to be modified to align packets. This procedure would be prohibitively memory intensive and is not recommended.

Testing was performed to characterize the information channels through the MCDD at various signal-to-noise levels. In addition, the MCDD's degraded guard channels can be used for transmission with inferior performance. Therefore, the guard channels were also characterized. Some parameters that were investigated include coding block length, data pattern, unique word value, and adjacent-channel interference. A final report of the complete testing and characterization of the system will be available by January 1996.

Bibliography

Wagner, P.K.; and Ivancic, W.D.: Multichannel Error Correction Code Decoder. AIAA Paper 94-1025 (NASA TM-106331), 1994.