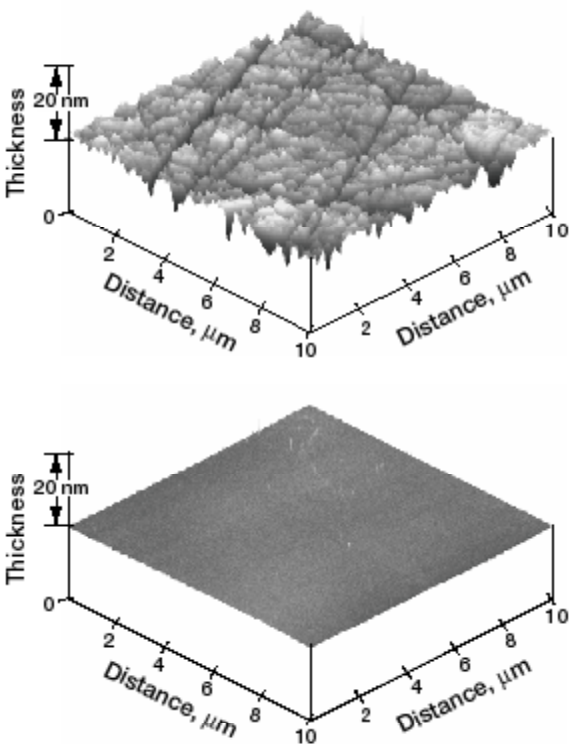
Chemical Mechanical Polishing of Silicon Carbide

The High Temperature Integrated Electronics and Sensors (HTIES) team at the NASA Lewis Research Center is developing silicon carbide (SiC) as an enabling electronic technology for many aerospace applications. The ability of SiC to function under high-temperature, high-power, and/or high-radiation conditions allows it to be used in applications where silicon, the semiconductor used in nearly all of today's electronics, is not practical. In jet engines, SiC power electronics could be used with electric actuators to replace pneumatic and hydraulic actuators, resulting in greatly enhanced performance and reliability. Also, SiC gas sensors could monitor high-temperature jet engine exhaust, leading to cleaner and more efficient operation. Other nonaerospace applications include improved high-voltage switching for energy savings in public electric power distribution and in electric cars.

The Lewis team is focusing on the chemical vapor deposition of the thin, single-crystal SiC films from which devices are fabricated. These films, which are deposited (i.e., epitaxially "grown") on commercial wafers, must consist of a single crystal with very few structural defects so that the derived devices perform satisfactorily and reliably. Using optical microscopy and atomic force microscopy in conjunction with transmission electron microscopy, we determined that subsurface damage in the wafers was a significant factor in many of the morphological features observed in the crystal films. Such subsurface damage can be caused by the cutting and polishing of wafers from the bulk crystals (boules), which are grown by a vendor.

Working in collaboration (NASA grant) with Professor Pirouz of Case Western Reserve University, we developed a chemical-mechanical polishing (CMP) technique for removing the subsurface polishing damage prior to epitaxial growth of the single-crystal SiC films. This technique uses a polishing procedure with an alkaline (pH > 10) slurry of colloidal silica at elevated temperatures (about 55 °C) to achieve SiC surfaces that are free of subsurface damage (as verified by high-resolution transmission electron microscopy). This development was somewhat of a surprise because SiC was believed to be impervious to chemical attack at such low temperatures. Surfaces of SiC wafers prepared with and without CMP are shown in the figure. Epitaxial films grown on SiC wafers prepared using CMP had significantly fewer morphological defects than films prepared on conventionally polished wafers. The CMP technique is still in an early state of development, and much work remains before a commercially viable process can be produced.



Atomic Force Microscope images of SiC wafers. Top: As-received wafer. Bottom: Wafer after CMP.

Bibliography

Zhou, L., et al.: Chemomechanical Polishing of Silicon Carbide. J. Electrochem. Soc., vol. 144, no. 6, June 1997, pp. L161-L163.

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