Reconfigurable Data Communications Packet-Switch Emulation Test Bed Demonstrated

The Communications Technology Division at the NASA Lewis Research Center has an ongoing program to develop advanced switching and routing technology concepts for future satellite onboard processing systems. Through a university grant as a part of this research, the Cleveland State University is using a flexible reconfigurable data communications packet switch emulation test bed to investigate packet switching techniques.

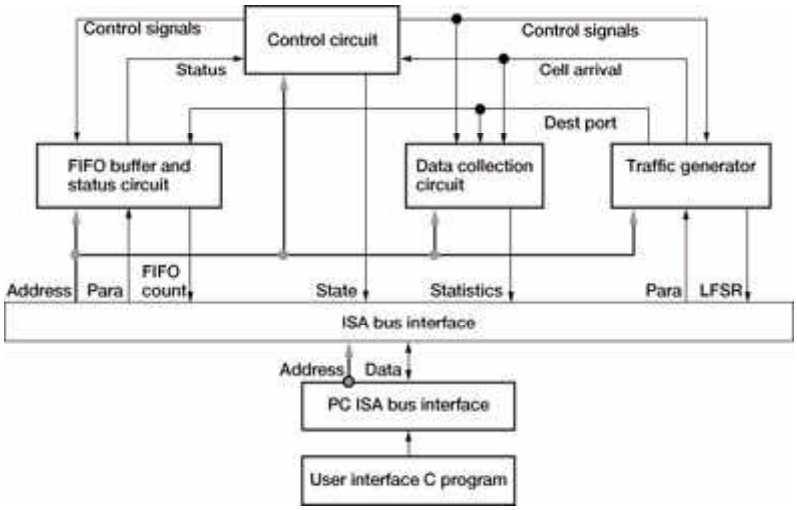
Because of the switching speed and protocol complexity, implementing a data communications network is a tremendous task. Various alternatives should be carefully studied and evaluated in the development stage so that the optimal system configuration can be obtained and implemented later. Therefore, it is desirable to predict the performance of the network before it is actually constructed. This is especially true in the case of satellite systems. In the past, theoretical analysis, software simulation, and prototyping were used to evaluate performance. However, each method has its drawback. There are basic tradeoffs among accuracy, cost, and required evaluation time. No method is completely satisfactory.

In addition to the theoretical analysis, software simulation, and prototype, there is one other possible alternative for performance evaluation--hardware emulation. Hardware emulation is similar to software simulation except that dedicated hardware modules replace software routines. The dedicated hardware can achieve much better performance and provide several orders of magnitude in increased speed over software simulation. When applied to network evaluation, it can be used to gather data for a realistic network configuration and to evaluate the performance of different schemes and protocols.

In the past, hardware emulation methods suffered the drawback of high cost and inflexibility and thus were rarely used. However, recent advances in field programmable gate array technology make it a feasible, and possibly superior, approach. The Cleveland State study investigated this approach and explored the feasibility of using hardware emulation to evaluate the performance of various asynchronous transfer mode (ATM) switch configurations and protocols. A reconfigurable test bed was developed utilizing static RAM-based (random access memory based) field programmable gate array technology. The flexible test bed, which was constructed to emulate an ATM switch, and consisted of an abstract ATM switch, a traffic generator, a data collection circuit, and a PC host interface (see the diagram). All the test bed hardware was described in industrial standard very high development language (VHDL). It was then synthesized and mapped into a field programmable gate array board. The construction and testing of the prototyping system was completed and used to evaluate several buffer management schemes. Results show that the hardware emulation was 10^2 to 10^5 times faster than

software simulation.

Para	Parameter	Control signal from the computer hardware
FIFO count	First in, first out count	Signal that keeps track of the number of generated data packets
Dest port	Destination port	Final destination of a generated data packet
LFSR	Linear Feedback Shift Register	Used as a uniform random number generator for generating data packets
ISA	Industry Standard Architecture	Standard hardware configuration used by 286 to 486 class IBM clone computers



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For more information, visit the Communications Technology Division at http://ctd.grc.nasa.gov/.

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