

HIGH QUALITY GAAS GROWTH BY MBE ON SI USING GESI BUFFERS AND PROSPECTS FOR SPACE PHOTOVOLTAICS¹

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ABSTRACT

III-V solar cells on Si substrates are of interest for space photovoltaics since this would combine high performance space cells with a strong, lightweight and inexpensive substrate. However, the primary obstacles blocking III-V/Si cells from achieving high performance to date have been fundamental materials incompatibilities, namely the 4% lattice mismatch between GaAs and Si, and the large mismatch in thermal expansion coefficient. In this paper, we report on the molecular beam epitaxial (MBE) growth and properties of GaAs layers and single junction GaAs cells on Si wafers which utilize compositionally graded GeSi intermediate buffers grown by ultra-high vacuum chemical vapor deposition (UHVCVD) to mitigate the large lattice mismatch between GaAs and Si. GaAs cell structures were found to incorporate a threading dislocation density of $0.9 - 1.5 \times 10^6 \text{ cm}^{-2}$, identical to the underlying relaxed Ge cap of the graded buffer, via a combination of transmission electron microscopy, electron beam induced current, and etch pit density measurements. AlGaAs/GaAs double heterostructures were grown on the GeSi/Si substrates for time-resolved photoluminescence measurements, which revealed a bulk GaAs minority carrier lifetime in excess of 10 ns, the highest lifetime ever reported for GaAs on Si. A series of growths were performed to assess the impact of a GaAs buffer layer that is typically grown on the Ge surface prior to growth of active device layers. We found that both the high lifetimes and low interface recombination velocities are maintained even after reducing the GaAs buffer to a thickness of only 0.1 μm . Secondary ion mass spectroscopy studies revealed that there is negligible cross diffusion of Ga, As and Ge at the III-V/Ge interface, identical to our earlier findings for GaAs grown on Ge wafers using MBE. This indicates that there is no need for a buffer to “bury” regions of high autodoping, and that either pn or np configuration cells are easily accommodated by these substrates. Preliminary diodes and single junction AlGaAs heteroface cells were grown and fabricated on the Ge/GeSi/Si substrates for the first time. Diodes fabricated on GaAs, Ge and Ge/GeSi/Si substrates show nearly identical I-V characteristics in both forward and reverse bias regions. External quantum efficiencies of AlGaAs/GaAs cell structures grown on Ge/GeSi/Si and Ge substrates demonstrated nearly identical photoresponse, which indicates that high lifetimes, diffusion lengths and efficient minority carrier collection is maintained after complete cell processing.

1. INTRODUCTION

The ability to achieve high efficiency and reliable space solar cells on lightweight, strong and inexpensive substrates is of great interest for virtually every satellite mission. For III-V space photovoltaics, this has led to the development of various types of III-V cells on Ge wafers, since Ge offers certain advantages in strength and cost over GaAs substrates while providing a lattice constant that closely matches that of GaAs. Nevertheless, from purely a substrate perspective, Ge is not ideal, especially when compared with Si, which is far cheaper, readily available in large areas, substantially stronger, and possesses a larger thermal conductivity. However, as is the

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case for many otherwise desirable combinations of substrates and epitaxial semiconductors, there exists a large mismatch in lattice constant (4% for GaAs/Si) that negates the advantage of the substrate by generating large densities of defects in the active device layers unless methods to control and reduce the density of mismatch-related defects are implemented. Numerous efforts have been made to deal with the mismatch during epitaxial growth, including thermally-cycled growth of the III-V intermediate layers, compositionally-graded III-V graded buffers, strained buffer layers, etc., and each has been successful in reducing the density of threading dislocations from $\sim 10^{10}$ cm⁻² for direct epitaxy of GaAs on Si, to $\sim 10^7$ cm⁻² for the various defect control approaches.[1-5] However, at this dislocation density minority carrier lifetimes in the range of ~ 1 -3 ns have been demonstrated, which are not high enough to generate efficient III-V solar cells. An alternative approach is to engineer the lattice constant of the Si substrate surface itself prior to III-V epitaxy, rather than dealing with the mismatch within the III-V regions alone. The Ge_xSi_{1-x} compositional alloy system is well-suited for this application since by slowly increasing the Ge content (x) during growth of a Ge_xSi_{1-x} epitaxial layer on Si, the lattice constant can be increased from that of Si to Ge, which provides a close lattice match for subsequent GaAs-based device growth. Of course this requires that the compositionally graded buffer layer is strain-relaxed so that the Ge surface lattice constant is matched to GaAs, and that the threading dislocations generated from relaxing the 4% misfit between Ge and Si are maintained to a minimum concentration in the Ge cap of this "virtual" Ge substrate. Recent work by Fitzgerald and co-workers has demonstrated that low threading dislocation densities (TDD) in relaxed Ge layers grown on compositionally-graded Ge_xSi_{1-x} buffers on Si are achievable.[6] Record-low TDD values of $\sim < 2 \times 10^6$ cm⁻² were achieved, as confirmed using plan-view and cross section transmission electron microscopy (TEM), electron beam induced current (EBIC) and etch pit density (EPD) measurements. As a result, these "virtual" Ge substrates are appealing for not only photovoltaic substrate applications, but also for integration of III-V optoelectronics with Si in general, since the residual TDD value in the substrate is already an order of magnitude lower than that observed for III-V layers grown on Si using III-V epitaxy-based dislocation control methods. At these TDD values, minority carrier lifetimes on the order of 10 ns can be expected, which can be translated into very respectable GaAs cell efficiencies. However, III-V epilayer growth and cell processing on Ge/Ge_xSi_{1-x}/Si wafers may not behave identically to III-V cell fabrication on Ge wafers, and issues such as the impact of residual dislocation density, thermal expansion mismatch, surface morphology, etc., on III-V overlayer quality all must be considered. In this paper, we present a growth, characterization and preliminary device study of GaAs and AlGaAs/GaAs layers and cell structures grown by molecular beam epitaxy (MBE) on graded Ge/Ge_xSi_{1-x}/Si substrate wafers. Note that for the remainder of the paper, the graded Ge_xSi_{1-x} buffer will be denoted by GeSi.

2. EXPERIMENTAL

III-V layers and AlGaAs/GaAs p on n single junction cell structures were grown by solid source MBE on Ge/GeSi/Si substrates. The Ge/GeSi growth was done by ultra high vacuum chemical vapor deposition. The composition of the GeSi buffer was increased during growth by step-grading from x = 0 (pure Si) to x = 1 (pure Ge) at an average rate of 10% Ge/μm. Details of the GeSi graded buffer growth have been described in previous work.[6] A combination of plan-view and cross sectional transmission electron microscopy (TEM), electron beam induced current (EBIC), and etch pit density (EPD) measurements were used to confirm an average TDD = $0.9 - 2 \times 10^6$ cm⁻² within the relaxed Ge cap layer for a number of growth runs. For all III-V growths, the MBE chamber background pressure was in the high 10⁻¹¹ torr range. Substrate temperatures were measured by infrared pyrometry except for temperatures below 450 °C for which substrate thermocouple readings are reported. In all cases, the substrates were (001) oriented with a 6° offcut toward the in-plane [110] direction. Substrate cleaning was found to be an important issue and here all substrates were cleaned in organic solvents, followed by a UV-ozone treatment before loading into the growth chamber.[7] Prior to MBE growth, surface oxides were removed by a 20 minute, 640 °C anneal, after which a thin Ge epitaxial layer was deposited onto the substrates, followed by GaAs epitaxy that was initiated using a 10 monolayer migration enhanced epitaxy (MEE) nucleation step. Two types of basic structures were grown, AlGaAs/GaAs/AlGaAs double heterostructures to facilitate minority carrier lifetime measurements by time resolved photoluminescence (TRPL), and p on n AlGaAs/GaAs heteroface cell structures. For either structure, we chose to vary the thickness of a GaAs buffer layer grown on top of the Ge prior to growth of the active III-V layers, from 0.1 μm - 1.0 μm, in order to assess the electronic quality of the III-V layers as a function of their proximity to the Ge/GeSi/Si surface. This is important from the viewpoint of reducing thermal expansion stress effects. The DH structure used for all minority carrier lifetime measurements is as follows: a GaAs layer doped at $n = 1.1 \times 10^{17}$ cm⁻³ of variable thickness (d = 0.5, 1.0, or 1.5 μm) sandwiched between Al_{0.3}.

Ga_{0.7}As layers of 50 nm and 20 nm thicknesses for the surface and buried barrier layers, respectively. Room temperature TRPL was used to measure the transient lifetime of the 870 nm GaAs band-to-band luminescence peak, the details of which have been described in earlier work.[8]. The bulk minority carrier lifetime (τ_p) and AlGaAs/GaAs interface recombination velocity (S) of each sample set was extracted from the net TRPL decay time (τ_{TRPL}) using

$$1/\tau_{TRPL} = 1/\tau_p + 2S/d \quad (1)$$

where d is the DH GaAs layer thickness. Cell structures were fully processed (without anti-reflection coatings), and were evaluated by dark and light I-V measurements, and by spectral response measurements. Identical cell and diode structures were grown on Ge/GeSi/Si, Ge and GaAs wafers to directly compare device characteristics as a function of substrate choice. To facilitate these measurements, Au-Cr and Au-Sb were used for front (p-type) and back (n-type) ohmic contacts, respectively. Finally, atomic diffusion of Ga, As and Ge across the heterovalent GaAs/Ge interfaces of DH and cell structures grown on the Ge/GeSi/Si substrates was investigated using secondary ion mass spectroscopy (SIMS).

3. RESULTS AND DISCUSSION

3.1. Structural Properties, Minority Carrier Lifetime and the Effect of GaAs Buffer Layer Thickness

Figure 1 shows a representative cross-sectional TEM image of an MBE-grown AlGaAs/GaAs heterostructure grown on a Ge/GeSi/Si substrate. At this scale, no threading dislocations are observable. Using a combination of lower magnification EBIC, plan-view TEM and EPD measurements, the III-V layers were found to contain a TDD = $0.9-1.5 \times 10^6 \text{ cm}^{-2}$, identical to the underlying Ge cap of the GeSi/Si substrate. This indicates that the GaAs/Ge interface is behaving as would be expected for an "ideal" low-mismatched interface (the misfit between GaAs and Ge is $\sim 0.17\%$) that generates only a very low density of new dislocations. Moreover, we did not detect any APB's or indication of APD disorder, consistent with our earlier results of an in-depth investigation of APD disorder in GaAs on Ge and its relation to GaAs growth nucleation conditions.[9] This is indicative of the successful transfer of our optimum GaAs growth and nucleation process on Ge wafers to Ge/GeSi/Si wafers. It is

interesting to note that while the compositionally graded GeSi buffer results in the well-known crosshatched surface morphology characteristic of low TDD, high quality graded buffers, this did not have an effect on the structural quality of the III-V overlayers.

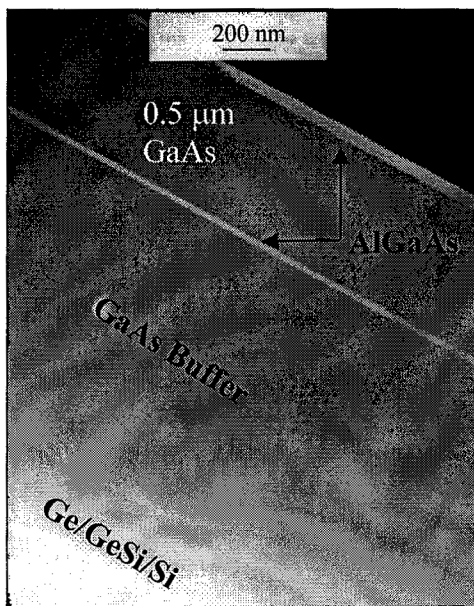


Figure 1. Cross section TEM micrograph of MBE-grown AlGaAs/GaAs/AlGaAs DH structure on Ge/GeSi/Si.

Note from figure 1 that a 1 μm thick GaAs buffer layer is present beneath the AlGaAs/GaAs/AlGaAs DH structure. For GaAs cells on Ge, a passive GaAs buffer layer grown on the Ge surface is often included to bury defects such as APB's emanating from the polar/nonpolar GaAs/Ge interface and to bury potential autodoping problems well below the active device regions. However, a critical aspect for successful, large area GaAs on Si device integration is the minimization of possible thermal stress-induced cracks resulting from thermal expansion coefficient mismatches. Thus it is imperative to reduce the thickness of GaAs (or Ge) buffer layers to a minimal amount. To investigate how the GaAs material quality varied with GaAs buffer layer thickness, a series of DH structures were grown on Ge/GeSi/Si substrates that incorporated a range of GaAs buffer layers from 0.1 – 1 μm in thickness. TRPL measurements indicated that there is no degradation of the minority carrier lifetime as a function of the GaAs buffer thickness. Indeed, figure 2 shows a comparison of the net TRPL decay curves for $d = 1.5 \mu\text{m}$ DH structures grown on Ge/GeSi/Si having GaAs buffers of

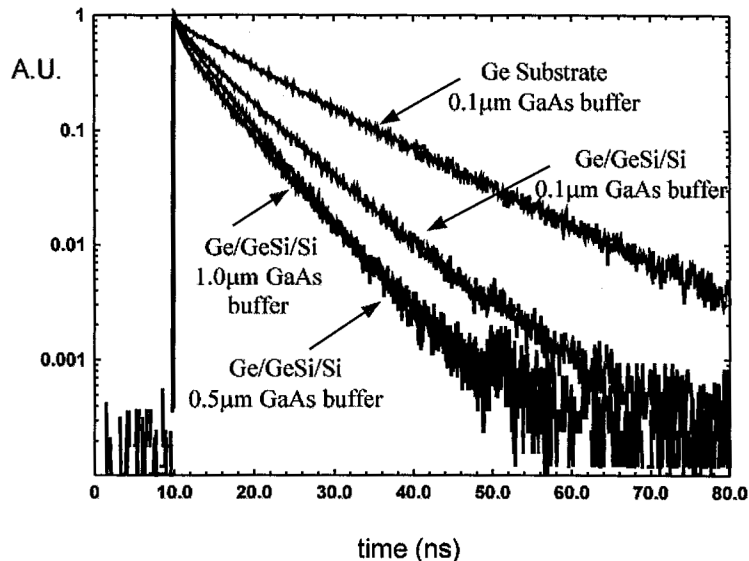


Figure 2. TRPL decay times for AlGaAs/GaAs/AlGaAs DH structures grown on Ge/GeSi as a function of GaAs buffer thickness as indicated. Measurements were done at 300 K.

encouraging as seen by the longer decay time in figure 2. The net PL decay time of 8.2 ns for this sample translates into a bulk minority carrier lifetime of 10.5 ns. This is calculated by using a value of 2,000 cm/s for S , which we consistently obtain independent of GaAs buffer thickness for all UV-ozone treated Ge/GeSi/Si surfaces (note from eq. 1 that a higher value for S will result in an even higher value for the minority carrier lifetime). These lifetime values are the highest bulk GaAs minority carrier lifetimes ever reported for GaAs grown on a Si substrate, and indicate that the GaAs buffer can safely be reduced to an almost negligible thickness of 0.1 μm with no degradation of either carrier lifetime or interface recombination velocity. The variations in our lifetimes from $\sim 8 - 10$ ns result from continued optimization of both the GaAs nucleation procedure and defect control in the Ge/GeSi/Si substrates. It should be noted that at these TDD values, the lifetime is a strong function of TDD, hence minor improvements in the TDD for the Ge/GeSi/Si substrates translates directly into higher lifetime values. This point is evident from figure 3 which shows a range of lifetime values measured on our samples as a function

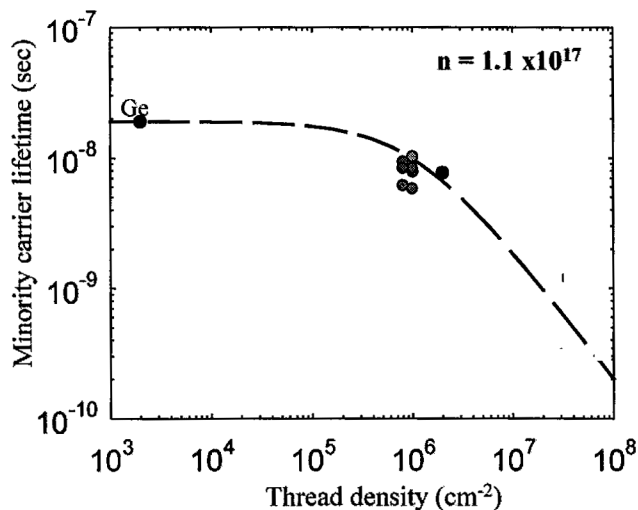


Figure 3. Bulk minority carrier lifetimes measured from a set of AlGaAs/GaAs/AlGaAs DH structures by TRPL plotted with the theoretically expected lifetime dependence on threading dislocation density. [after 2]

1.0, 0.5 and 0.1 μm in thickness. Also shown, for comparison, is the TRPL decay for the same DH structure grown on a Ge wafer. First looking at the 1.0 and 0.5 μm GaAs buffer results, we observe no change in the TRPL decay time. A full analysis of the former resulted in a bulk minority carrier lifetime for n-type GaAs of 7.7 ns and an interface recombination velocity (S) of 3,900 cm/s, by TRPL measurements applied to a range of DH GaAs thicknesses following eq. (1).[8] Note that for these particular structures, the Ge surface was chemically etched prior to III-V epitaxy. The recombination velocity was found to be very sensitive to substrate cleaning prior to III-V growth, and subsequent improvements (inclusion of UV-ozone exposure) resulted in a reduction in S to $\sim 1,800 - 2,200$ cm/s, independent of GaAs buffer thickness.

The TRPL results for the 0.1 μm thick GaAs buffer are even more encouraging as seen by the longer decay time in figure 2. The net PL decay time of 8.2 ns for this sample translates into a bulk minority carrier lifetime of 10.5 ns. This is calculated by using a value of 2,000 cm/s for S , which we consistently obtain independent of GaAs buffer thickness for all UV-ozone treated Ge/GeSi/Si surfaces (note from eq. 1 that a higher value for S will result in an even higher value for the minority carrier lifetime). These lifetime values are the highest bulk GaAs minority carrier lifetimes ever reported for GaAs grown on a Si substrate, and indicate that the GaAs buffer can safely be reduced to an almost negligible thickness of 0.1 μm with no degradation of either carrier lifetime or interface recombination velocity. The variations in our lifetimes from $\sim 8 - 10$ ns result from continued optimization of both the GaAs nucleation procedure and defect control in the Ge/GeSi/Si substrates. It should be noted that at these TDD values, the lifetime is a strong function of TDD, hence minor improvements in the TDD for the Ge/GeSi/Si substrates translates directly into higher lifetime values. This point is evident from figure 3 which shows a range of lifetime values measured on our samples as a function of TDD in the substrate, plotted along with the theoretical dependence of minority carrier lifetime on TDD as calculated by Yamaguchi.[2] As seen, our data correlates well with the calculated values. The small scatter observed in the data is most likely due to uncertainties in measuring TDD with high accuracy, since it is very difficult to count and separate individual threading dislocations at these low TDD values, which is further clouded by the presence of small dislocation pileups from which it is difficult to discern individual threads. In comparison to other reports, the highest previous lifetimes for GaAs on Si using other methods of defect control are on the order of $\sim 1-3$ ns.[1-5] From figure 3 it is clear that our current lifetime values are approaching the lifetime plateau below a TDD of \sim mid 10^5 cm^{-2} range, but even at 10 ns, high efficiency GaAs cells should be possible. Note that a lifetime value is also shown for GaAs grown on Ge as a point of reference, and that all TRPL data reported here were obtained from DH structures that were uniformly doped n-type to $1.1 \times 10^{17} \text{ cm}^{-3}$.

3.2. GaAs/Ge Interface Diffusion for MBE-Grown GaAs on Ge/GeSi/Si Substrates

While the electronic quality (i.e. lifetime and diffusion length) of the GaAs material grown on the Ge/GeSi/Si buffer is perhaps the most important aspect for photovoltaic performance, it is also necessary to determine whether the minimal 0.1 μm GaAs buffer discussed above is appropriate from the viewpoint of autodoping. This is an important issue for GaAs grown on a Ge terminated substrate since the high growth temperatures of conventional epitaxy (especially MOCVD) can cause cross diffusion of As, Ga and Ge at the GaAs/Ge interface, generating high background doping over many microns, and even type conversion. In previous work on GaAs growth on Ge wafers by MBE, we demonstrated the successful minimization of such diffusion to negligible levels using an optimum interface nucleation procedure, which includes a low temperature MEE nucleation step, that is maintained even after complete cell growth and processing under typical conditions.[9-11] Here, we repeat these experiments for GaAs grown on Ge/GeSi/Si substrates to investigate whether the residual TDD or the presence of the crosshatch morphology has an effect on atomic diffusion at the GaAs/Ge interface.

Figures 4a, 4b and 4c show the SIMS atomic concentration profiles obtained for Ge in GaAs, Ga in Ge, and As in Ge, for a 2 μm thick GaAs layer grown on the Ge/GeSi/Si substrates. For comparison, SIMS profiles are also shown for GaAs grown on Ge wafers under identical growth conditions. In all cases, GaAs growth was initiated by the MEE step and the 2.5 μm thick GaAs layer was grown at a substrate temperature of 620 C. As can be seen from figure 4, there is negligible diffusion across the interface

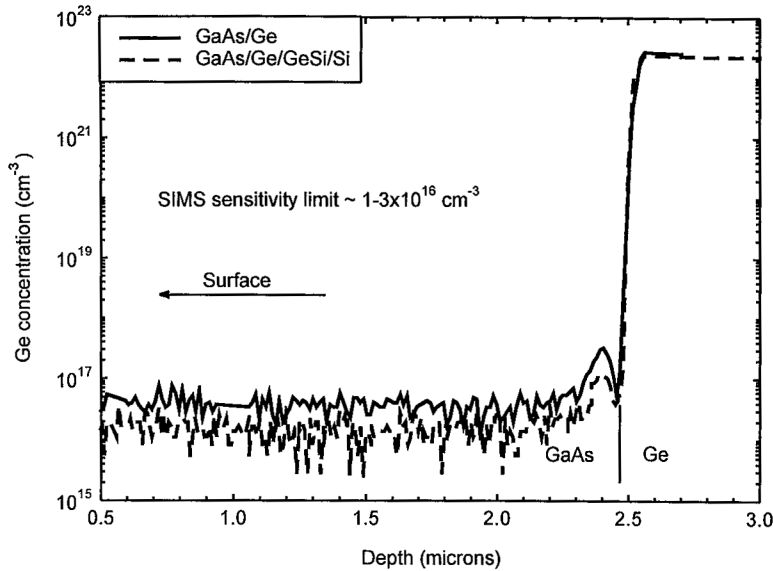


Figure 4(a). Ge SIMS profiles in GaAs grown on Ge/GeSi/Si and Ge substrates.

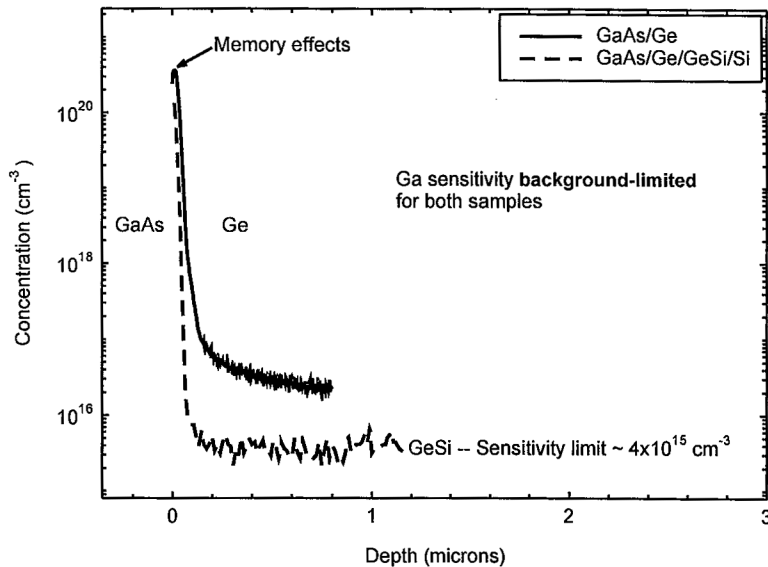


Figure 4(b). SIMS profiles showing negligible Ga penetration into the Ge/GeSi/Si and Ge substrates after 2.5 μm of GaAs MBE growth on each substrate.

boundary for all cases on either substrate. It is interesting to note that while the profiles for Ge in GaAs and Ga in Ge appear to be identical for either substrate (the only difference in figures 4a and 4b between the substrates is the lower detection limit for the SIMS measurements made on the GaAs/Ge/GeSi/Si structures), there is actually less As diffusion into the Ge cap of the GeSi/Si substrate than for the Ge wafer. The reason for this is not known and warrants additional investigation. These are very encouraging results since they confirm that the 0.1 μm GaAs buffer is more than sufficient to protect an overlying III-V cell from diffusion and autodoping effects. Moreover, the lack of detectable Ga or As diffusion into the Ge/GeSi/Si substrate indicates that complete control of the subsequent cell polarity (p on n versus n on p) is possible.

3.3. GaAs Diode and Preliminary Solar Cell Characteristics on Ge/GeSi/Si

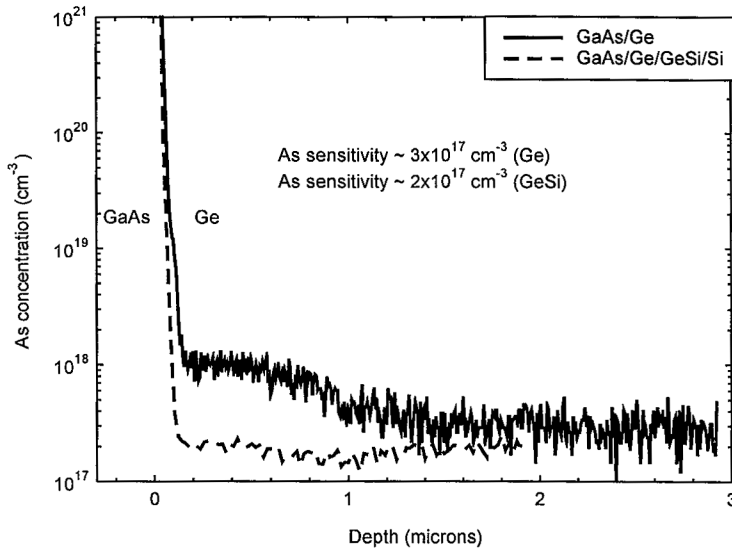


Figure 4(c). SIMS profiles showing minimal As penetration into the Ge/GeSi/Si and Ge substrates after 2.5 μm of GaAs MBE growth on each substrate.

P⁺n AlGaAs/GaAs heteroface cell structures were grown on the Ge/GeSi/Si substrates, and were fabricated into test diodes and solar cells for preliminary device analysis. All devices were grown using a 0.1 μm GaAs buffer as discussed above. Identical structures were also grown on both GaAs and Ge substrates in order to obtain a preliminary comparison of device characteristics as a function of substrate material and mismatch. Figure 5 shows forward and reverse bias dark I-V characteristics for 1 mm diameter diodes on each substrate. As seen, the I-V curves are almost identical, with turn-on voltages of ~ 1 V for all cases, and identical reverse leakage currents out to at least -2 volts. The most noticeable difference between the diodes is a slightly increased series resistance in forward bias for GaAs/Ge and GaAs/Ge/GeSi/Si

as compared to the GaAs/GaAs diode. We attribute this to a higher back contact resistance for our ohmic contact process to the group IV substrates. The identical turn-on voltages and reverse leakage currents are significant, since this is where any negative effect of the residual TDD for the Ge/GeSi/Si substrates would be expected to manifest itself in the form of a shunt path that would lower the diode turn on voltage and increase the reverse leakage current. The fact that with a TDD = $1 \times 10^6 \text{ cm}^{-2}$, the 1 mm diameter diode covers $\sim 7,800$ threading dislocations and yet these diodes yield very similar characteristics to the GaAs/GaAs diodes,

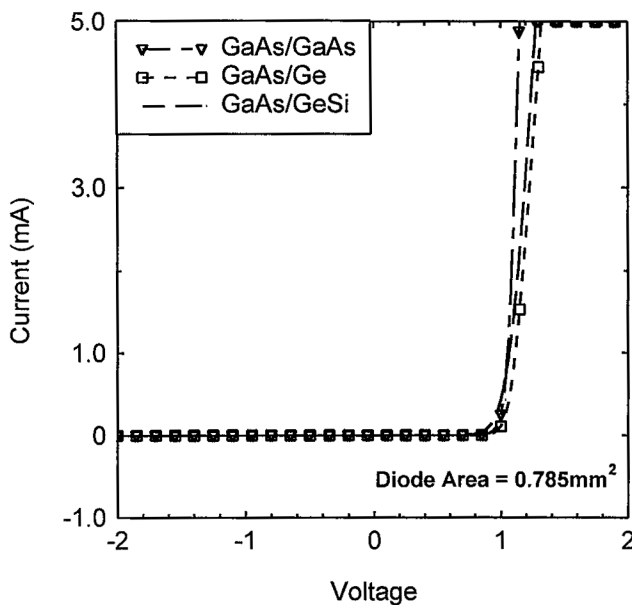


Figure 5. Comparison of dark I-V characteristics for AlGaAs/GaAs test diodes grown on GaAs, Ge and Ge/GeSi/Si substrates.

suggest that shunt currents in a completed, properly processed GaAs cell on Ge/GeSi/Si should not be significantly impacted by threading dislocations at our current threading dislocation density. We have recently begun to fabricate GaAs solar cells on Ge and Ge/GeSi/Si substrates. Figure 6 shows a comparison of the external quantum efficiency (EQE) responses of our first cells fabricated on Ge/GeSi/Si substrates, along with an EQE curve for a GaAs cell grown on a Ge wafer. At this time, no anti-reflection coatings were applied and the AlGaAs window layer (85% Al) was conservatively thick at 50 nm. The comparison indicates that the carrier collection efficiency is virtually identical for GaAs cells on either substrate. Hence, the high lifetime observed in the GaAs DH structures discussed earlier is replicated in the cell growth and maintained during the entire cell fabrication process. This is even more significant if one considers that only a 0.1 μm GaAs buffer was used between the cell layers and the substrate, demonstrating the robustness of our interface nucleation and MBE growth procedures. At this time, we have not yet completed a final cell with an optimum fabrication process. However, at the current

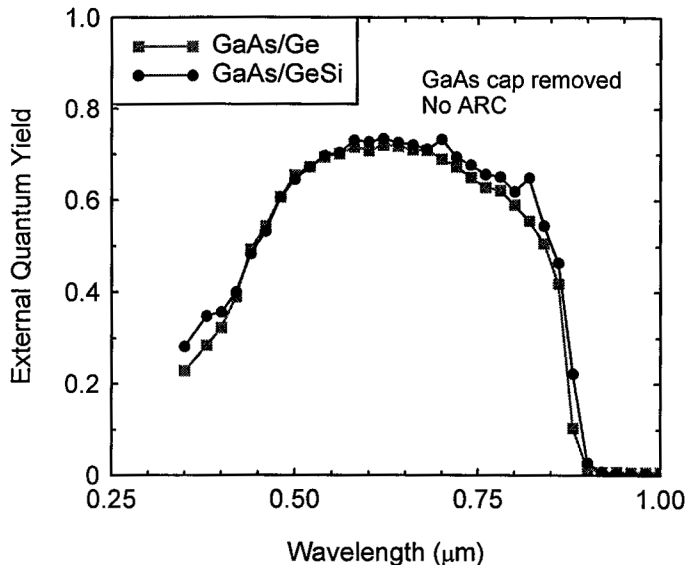


Figure 6. External quantum efficiency measurements for single junction GaAs cells grown on Ge and Ge/GeSi/Si substrates indicating the similar minority carrier collection efficiency for each.

detection limits on either side of the interface. The material results translated into excellent device characteristics, with nearly identical dark I-V characteristics being obtained for GaAs diodes grown on GaAs, Ge and Ge/GeSi/Si substrates in both forward and reverse bias regimes. Preliminary cell results are extremely promising, with virtually identical EQE responses for GaAs cells grown on Ge and Ge/GeSi/Si substrates that indicates long diffusion lengths and high collection efficiencies are maintained in the GaAs cell, even to within 0.1 μm of the Ge/GeSi/Si substrate. These results hold great promise for future demonstration of high efficiency III-V cells on Si via heteroepitaxy and group IV graded buffer technology.

5. References

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stage of processing our first cells, an AM0 $J_{sc} = 24.0 \text{ mA/cm}^2$ with a $V_{oc} = 0.95 \text{ V}$ has been achieved prior to the application of an anti-reflection coating. This compares favorably to a completed $\sim 20\%$ AM0 MBE-grown GaAs single junction cell on Ge, which at the same stage of processing, yielded a $J_{sc} = 24.5 \text{ mA/cm}^2$ and a $V_{oc} = 0.99 \text{ V}$.

4. Conclusions

The material and device properties of GaAs grown on low defect density Ge/GeSi/Si substrates were investigated for potential applications in space III-V solar cell technology. Record high minority carrier lifetimes in excess of 10 ns were demonstrated for GaAs on Si, which resulted from the combined use of high quality graded GeSi buffer layers coupled with careful GaAs/Ge interface nucleation. It was shown that the high material quality was maintained for GaAs buffer layer thickness as low as 0.1 μm . Moreover, the MBE nucleation conditions resulted in a negligibly small atomic interdiffusion at the GaAs/Ge interface that was at or below the SIMS