

ELECTRICAL CHARACTERIZATION OF DEFECTS IN SiC SCHOTTKY BARRIERS

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Abstract

We have been investigating the effects of screw dislocation and other structural defects on the electrical properties of SiC. SiC is a wide-bandgap semiconductor that is currently receiving much attention due to its favorable high temperature behavior and high electric field breakdown strength. Unfortunately, the current state-of-the-art crystal growth and device processing methods produce material with high defect densities, resulting in a limited commercial viability. In order to characterize these defects, we have been correlating the electrical behavior of Au on 6H-SiC Schottky barriers with other physical measurements. We have been able to related minority carrier recombination centers, identified by electron beam induced current (EBIC) measurements, to screw dislocations observed by synchrotron white-beam x-ray topography. These screw dislocations have also been correlated with growth pits on the SiC surface observed via the Nomarski imaging method and atomic force microscopy. We have characterized the electrical behavior of the Au on SiC Schottky barriers using current versus voltage and capacitance versus voltage measurements. The effects of the observed electronic defects on the electrical behavior of these devices will be discussed.

1. Introduction

The 6H-SiC polytype is a promising wide bandgap ($E_g = 3.0$ eV) semiconductor which is being developed for use in high-temperature, high-power, high-frequency, and high-radiation conditions.¹ The advantages of this material lie in its extremely large breakdown field strength, high thermal conductivity, good electron saturation drift velocity, and stable electrical performance at temperatures as high as 600 °C.² These properties have made SiC an ideal candidate for high-temperature electronics and high-power microwave devices. In addition, it has also generated interest in the space power community as a possible photovoltaic solar cell material for devices capable of operating within three solar radii of the sun.³

The processing techniques required to produce high-quality SiC wafers has undergone tremendous improvement since this material was first investigated for semiconductor applications. However, even the best SiC produced today still has a large density of crystallographic defects.⁴ The most prominent of these defects being screw-dislocations and their hollow-core counterparts, micropipes.⁵ These defects have been correlated with increased reverse leakage currents and soft reverse bias breakdown in SiC Schottky diodes.⁶

In order to better characterize these defects and understand their role in the electronic performance of SiC-based devices, Schottky barriers on 6H-SiC epilayers have been analyzed by a variety of electrical and structural characterization techniques. An effort has been made to correlate the structural defects, specifically screw dislocations, with electronic recombination centers.

The structural defects have been investigated using synchrotron white-beam X-ray topography. This technique produces a gray-scale image that identifies regions of stress within the crystalline lattice. Surface imperfections have also been examined using Nomarski microscopy and atomic force microscopy. Nomarski microscopy uses the interference of converging beams of light to be able to identify surface features and atomic step heights as small as 30 angstroms.⁷ Atomic force microscopy is an ultra-low force profilometer capable of measuring height differences on the atomic scale.

The electronic recombination centers have been identified using electron-beam induced current (EBIC) measurements. EBIC is performed in a scanning electron microscope (SEM). In this technique, as the electron beam in the SEM is rastered across the Schottky barrier surface, the current induced in the device by the creation of electron-hole pairs at or near the boundary depletion width is measured.⁸ The induced current is then plotted in gray-scale as a function of beam position. Areas in which there is significant carrier recombination and low induced current appear darker in the resulting image.

2. Experimental Details

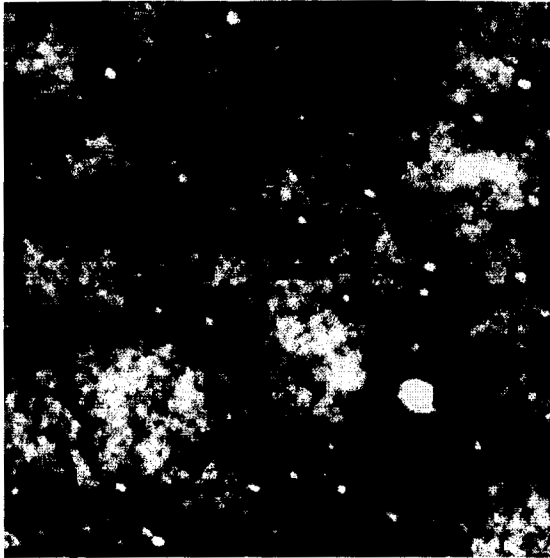
The 6H-SiC samples were made at the NASA Glenn Research Center by growing a 3.5 μm thick homoepilayer on 3.5° off-axis n-type SiC wafers obtained from Cree Research. The samples were nitrogen doped to approximately 10^{16} cm^{-3} during epilayer growth. Immediately following a surface clean-up using a buffered HF etch and rinse, 40 nm thick gold contacts were electron beam evaporated and patterned into 0.9 mm square pads using lift-off photolithography.

The structural defects in the 6H-SiC were analyzed using synchrotron white-beam X-ray topography (SWBXT) at NSLS at Brookhaven National Lab. Surface defects were imaged using Nomarski microscopy and a Digital Instruments Nanoscope III atomic force microscope (AFM). The electrical behavior of the Schottky diodes was analyzed using current versus voltage and capacitance versus voltage measurements using a computer controlled Keithley 236 Source/Measure Unit and a Keithley 590 CV Analyzer. Electronic defects in the diodes were imaged using electron-beam induced current (EBIC) measurements performed in a Hitachi S-800 Field-Emission Scanning Electron Microscope (SEM).

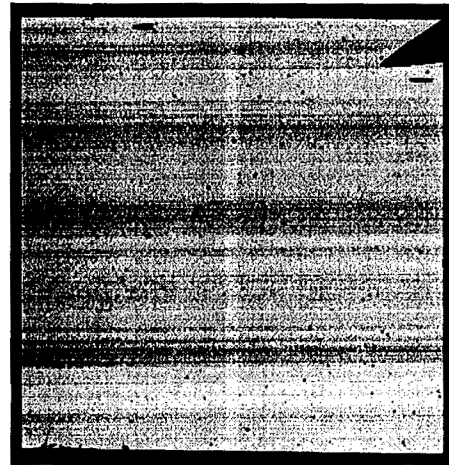
3. Results and Discussion

The contrast in the SWBXT image shown in Figure 1a represents areas of stress in the crystalline lattice. The image shown was digitally re-scaled to remove the asymmetric distortion associated with the SWBXT technique. The white spots appearing in the image are indicative of screw dislocations. EBIC was performed on the same area that is shown in Figure 1a, after it was coated with gold (see Figure 1b). Many dark areas corresponding to recombination centers or electronic defects at or near the metal semiconductor junction can be seen. A mask of the screw dislocations identified in the SWBXT image in Figure 1a was overlaid on the EBIC image shown in Figure 1b (see Figure 2). It is evident from this result that the screw dislocations act as electronic recombination centers.

A Nomarski microscope was used to look at the surface imperfections on the same sample discussed above. The area was divided into 12 smaller sections from which to obtain the high resolution Nomarski images. These images were then combined to produce the image of the entire area as shown in Figure 3a. Overlaying the same screw dislocation mask used in Figure 2 (generated using the SWBXT image) on the Nomarski image shows that screw dislocations also result in growth pits (see Figure 2b). Surface particulates were found at the locations in which screw dislocations were present and no growth pits were recorded. It is believed that the particulates may have obscured the growth pits in those areas. The growth pits that correspond to screw dislocations have a characteristic shape, as seen in the Nomarski images. Atomic force microscopy was used to investigate the topography of the screw dislocation growth pits (see Figure 4).



(a)



(b)

Figure 1. a) SWBXT image showing stress in the crystal lattice. The light colored dots are indicative of screw dislocations, where the stress is high. b) EBIC image representing collected current as a function of position. Dark spots indicate recombination centers in the epilayer.

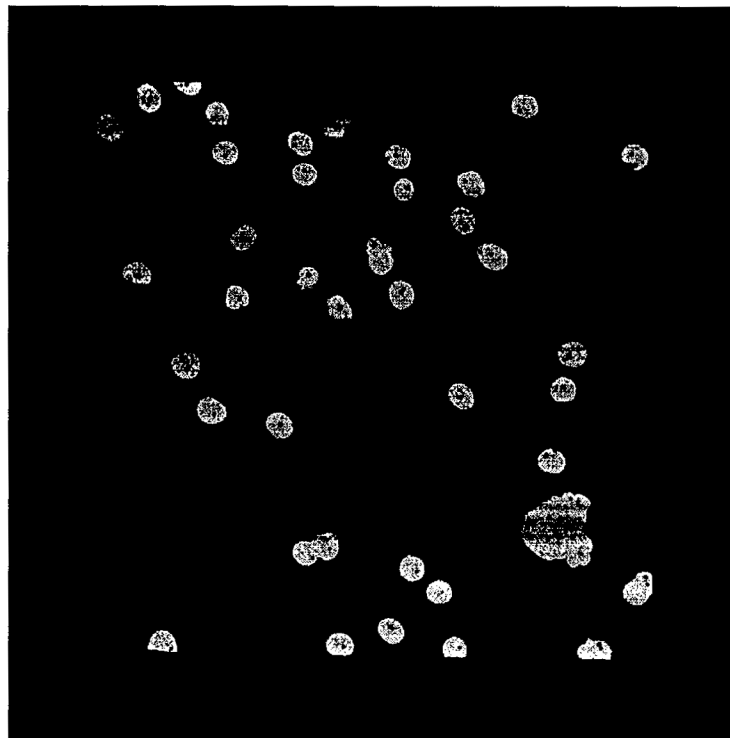


Figure 2. A Screw dislocation mask, from a SWBXT image, overlaid on an EBIC scan of a Au Schottky barrier placed on the same area. Dark spots in the EBIC scan correspond to electronic recombination centers and are found at each of the screw dislocations identified.

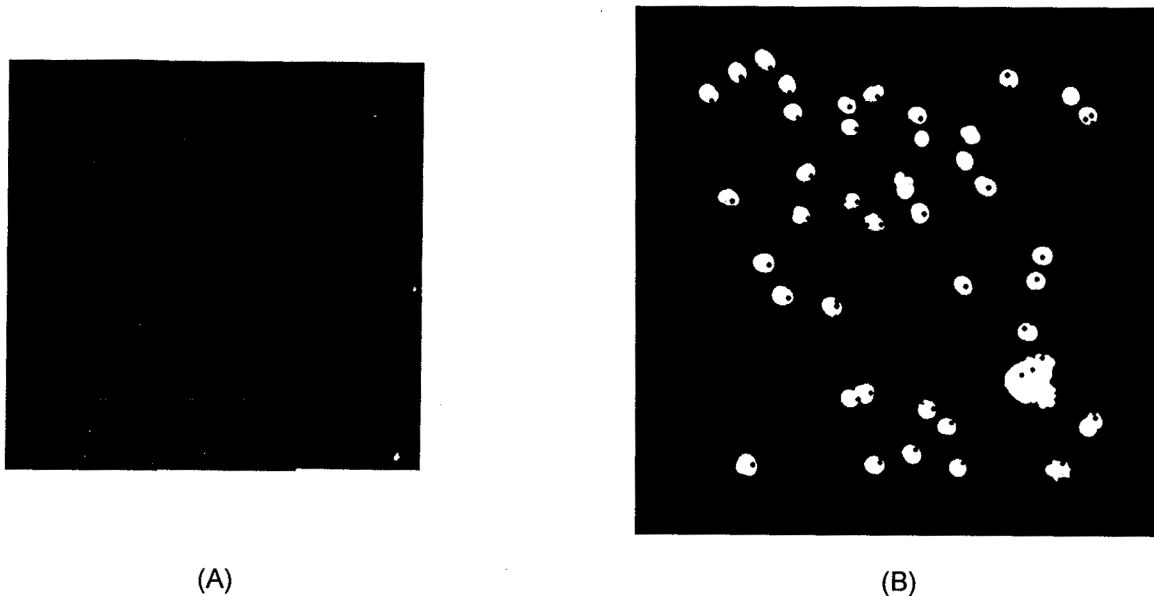


Figure 3. a) Nomarski image of a die with locations of growth pits marked. b) A mask of screw dislocations from Figure 1a is overlaid onto the Nomarski image in a) revealing that screw dislocations are correlated with growth pits.

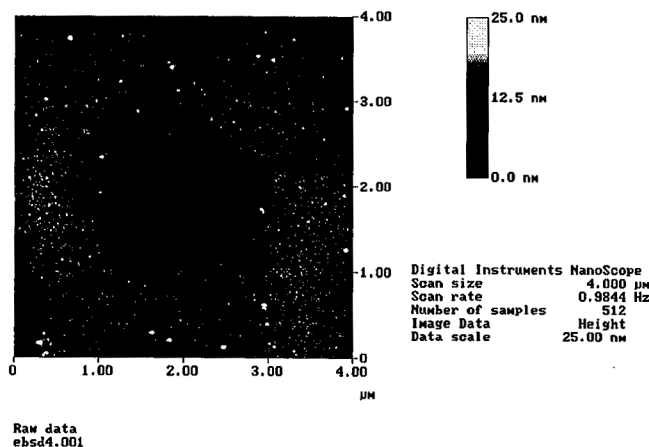


Figure 4. An AFM image of a growth pit that was identified as a screw dislocation in Figure 3b.

The current versus voltage scans of the Schottky barriers produced in this study showed good Shockley diode behavior (see Figure 5a). However, several of the diodes showed non-linear behavior in the Log current versus voltage forward bias scan (see Figure 5b). This behavior has previously been reported in SiC Schottky diodes by Defives et. al. and has been attributed to a dual barrier height model.⁹ It is believed that junction defects give barrier height inhomogeneities which cause the causing the device characteristics to resemble two barriers in parallel. This behavior did not correlate to the position of the die on the sample surface. This behavior also did not correlate with the number or type of electrical or structural defects identified in this study. The barrier heights obtained from the current versus voltage behavior of the various dies were between 0.85 and 1.08 eV. The ideality factors for all the diodes measured were between 1.1 and 1.5. The reverse-bias analysis of these Schottky diodes showed a wide variety of breakdown types and voltages. The types range from very soft to

extremely hard and the voltages ranged from approximately 40 V to nearly 140 V. However, only a slight correlation between screw dislocation and premature breakdown was apparent.

Capacitance versus voltage measurements were performed on all the Schottky barriers to determine dopant densities as a function of position on the sample surface. The results were analyzed using a simple parallel-plate capacitor model.¹⁰ These results were also used to investigate possible vertical dopant gradients within the epilayer. All of the dies showed excellent linearity in their inverse capacitance squared versus voltage behavior, indicating a homogenous vertical doping in the epilayer (see Figure 6). The carrier densities for 5 different dies spread out uniformly over the sample surface were all with a range of 1.12×10^{16} to $1.21 \times 10^{16} \text{ cm}^{-3}$. These values are in good agreement with the anticipated doping density. The dies from which these values were obtained were randomly distributed across the sample surface and therefore did not indicate any transverse doping gradients across the sample. The barrier heights were found to be between 1.18 and 1.29 eV.

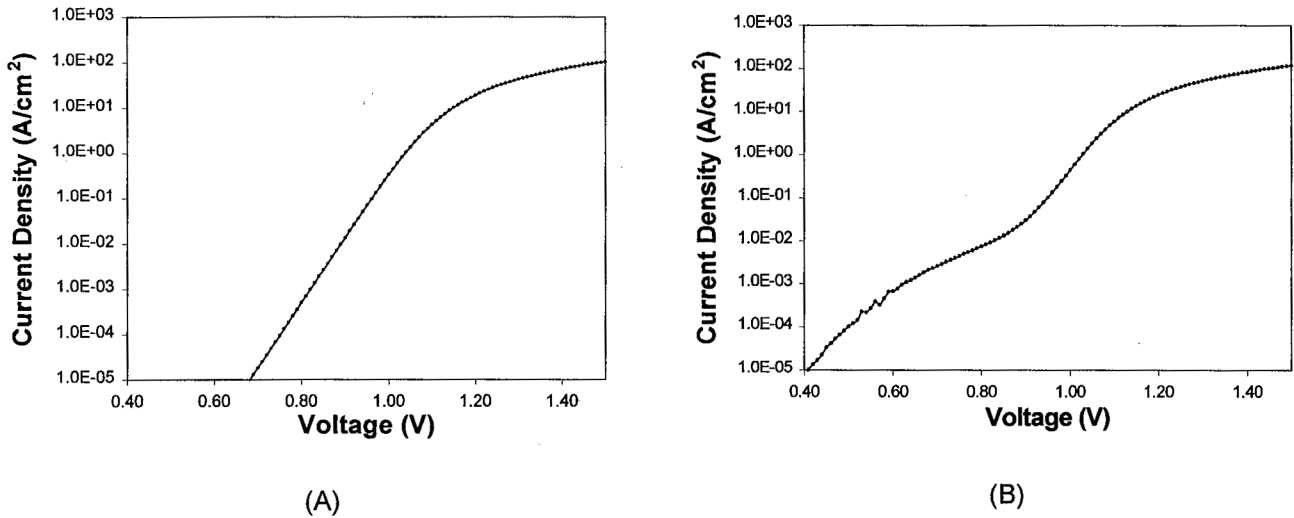


Figure 5. Current versus voltage characteristics of similar dies within the same area show both a) linear and b) non-linear characteristics.

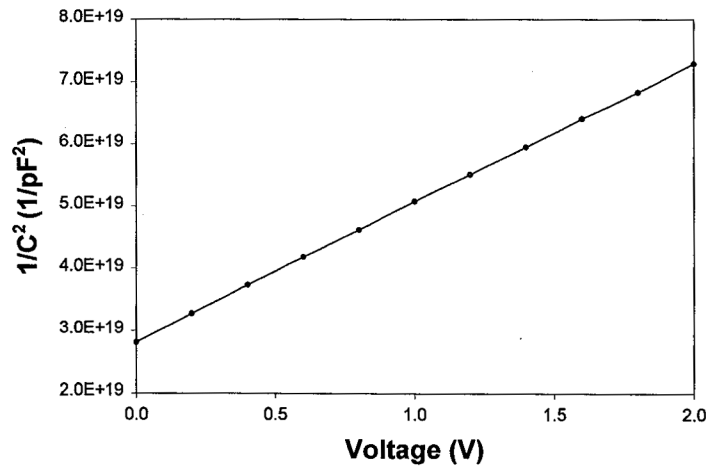


Figure 6. Capacitance versus voltage data reveals that the doping of the sample is $1.15 \times 10^{16} \text{ cm}^{-3}$.

4. Conclusions

A positive correlation has been shown between screw dislocations, identified by synchrotron white-beam x-ray topography, and electronic recombination centers, identified by electron-beam induced current measurements of gold on 6H-SiC Schottky barriers. Nomarski microscopy was used to show that the aforementioned screw dislocations also result in growth pits on the semiconductor surface. The growth pits associated with screw dislocations have a characteristic shape that can be imaged with atomic force microscopy. Although the Schottky barriers analyzed by EBIC were shown to have numerous electronic defects, current versus voltage characterization showed that they still exhibited reasonable diode characteristics. Capacitance versus voltage measurements were used to determine a carrier density in the SiC on the order of 10^{16} cm^{-3} . Some of the diodes measured here did exhibit non-linear logarithmic current versus voltage behavior, as previously identified in 6H-SiC Schottky diodes. However, no correlation was seen between this behavior and the density of screw dislocations.

References

- [1] P.G. Neudeck, *J. Electron. Mater.* **24**, 283 (1995).
- [2] M. Bhatnagar and B.J. Baliga, *IEEE Trans. on Electron Devices* **40**, 645 (1993).
- [3] D.A. Scheiman, G.A. Landis, and V.G. Weizer, *Space Technology and Applications International Forum*, AIP Proc. **453** (1999).
- [4] P.G. Neudeck, W. Huang, and M. Dudley, in *Power Semiconductor Materials and Devices*, edited by S.J. Pearton, R.J. Shul, E. Wolfgang, F. Ren, and S. Tenconi (Materials Research Society, Warrendale, PA 1998), Vol. 483, pp. 285-384.
- [5] P.G. Neudeck and J.A. Powell, *IEEE Electron Device Lett.* **15**, 63 (1994)
- [6] P.G. Neudeck, W. Huang, and M. Dudley, *IEEE Trans. Electron Devices* **46**, 478 (1999).
- [7] G. Nomarski, French Patents Nos. 1059124 and 1056361.
- [8] D.K. Schroder, *Semiconductor Material and Device Characterization* (John Wiley & Sons, New York, NY 1990), pp.391-394.
- [9] D. Defives, O. Noblanc, C. Dua, C. Brylinski, M. Barthula, V. Aubry-Fortuna, and F. Meyer, *IEEE Trans.on Electron Dev.* **46**, 449 (1999)
- [10] S.M. Sze, *Physics of Semiconductor devices* (John Wiley & sons, New York, NY 1981), 2nd edition, pp.248-249.