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SHORT COURSE

Single Event Transients in

Linear Integrated Circuits

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1.0 Introduction

On November 5, 2001, a processor reset occurred on board the Microwave Anisotropy Probe (MAP), a NASA mission to measure the anisotropy of the microwave radiation left over from the Big Bang. The reset caused the spacecraft to enter a safehold mode from which it took several days to recover. Were that to happen regularly, the entire mission would be compromised, so it was important to find the cause of the reset and, if possible, to mitigate it. NASA assembled a team of engineers that included experts in radiation effects to tackle the problem. The first clue was the observation that the processor reset occurred during a solar event characterized by large increases in the proton and heavy ion fluxes emitted by the sun. To the radiation effects engineers on the team, this strongly suggested that particle radiation might be the culprit, particularly when it was discovered that the reset circuit contained three voltage comparators (LM139). Previous testing revealed that large voltage transients, or "glitches" appeared at the output of the LM139 when it was exposed to a beam of heavy ions [NI96]. The function of the reset circuit was to monitor the supply voltage and to issue a reset command to the processor should the voltage fall below a reference of 2.5 V [PO02]. Eventually, the team of engineers concluded that ionizing particle radiation from the solar event produced a negative voltage transient on the output of one of the LM139s sufficiently large to reset the processor on MAP. Fortunately, as of the end of 2004, only two such resets have occurred.

The reset on MAP was not the first malfunction on a spacecraft attributed to a transient. That occurred shortly after the launch of NASA's TOPEX/Poseidon satellite in 1992. It was suspected, and later confirmed, that an anomaly in the Earth Sensor was caused by a transient in an operational amplifier (OP-15) [KO93]. Over the next few years, problems on TDRS, CASSINI, [PR02] SOHO [HA99,HA01] and TERRA were also attributed to transients. In some cases, such events produced resets by falsely triggering circuits designed to protect against over-voltage or over-current. On at least three occasions, transients caused satellites to switch into "safe mode" in which most of the systems on board the satellites were powered down for an extended period. By the time the satellites were reconfigured and returned to full operational state, much scientific data had been lost. Fortunately, no permanent damage occurred in any of the systems and they were all successfully re-activated.

In light of the serious consequences transients in linear circuits have had on recent space missions, now is an appropriate time to review our current level of understanding. To begin, it is necessary to define the term Single Event Transient (SET). An SET is any temporary voltage disturbance that occurs in an integrated circuit (IC) following the passage of an ionizing particle through the IC. SETs occur in both digital and analog ICs. (SETs in digital circuits are referred to as DSETs and those in analog circuits as ASETs.) SETs occur in devices manufactured with silicon CMOS, bipolar, or BiCMOS, or III-V technology. SETs are generated at internal circuit nodes, but whether they are detected depends on a number of factors. For example, if a DSET occurs in a memory, it must be sufficiently large to upset the contents of the memory in order to be detected. A DSET in a logic circuit is only detected after propagating through the combinational logic and being captured in a register, where it alters the existing information bit. Similarly, an ASET is only detected if it first propagates to the output of a linear circuit and then to a follow-on circuit where it alters the state of the circuit.

More than twenty papers have been published on the topic of ASETs in analog circuits during the last four years. In addition, a compendium of single-event-transient data was published that contains information on ASETs in more than fifty different analog devices [SA01]. These papers are testament to the advances made in our understanding of this phenomenon. The support provided to investigators at a number of different institutions by the Defense Threat Reduction Agency was the essential ingredient that led to this rapid progress. Some institutions concentrated on testing with broad ion beams (NAVSEA-Crane, NASA-GSFC). Others used focused ion

beams (Sandia National Laboratories), or pulsed laser light (Naval Research Laboratory). Another (Vanderbilt University) used computers for ASET simulation, and general technical expertise was provided by RLP Research. IXL Microelectronics Laboratory (University of Bordeaux, France), although not officially part of the group, nevertheless made valuable contributions with a pulsed laser system as did Sandia National Laboratory with their focused ion microprobe. Each group contributed its own special set of skills, but it was the synergy that was the key to success.

The aim of this Short Course is to review all aspects of ASETs, including generation, testing, modeling, hardness assurance, and mitigation. Emphasis will be placed on how the various analytical and experimental techniques worked in concert to provide the information necessary for understanding ASETs.

2.0 Background

A Short Course presented in 2001 at NSREC dealt exclusively with SETs in digital circuits [BU01a]. The course did not include ASETs because, at that time, there were relatively few published reports on the subject. The recognition that ASETs have been responsible for anomalies in a number of different space missions justifies a course devoted solely to them. Space systems contain many different types of linear circuits, including operational amplifiers, voltage comparators, voltage references, pulse-width modulators, voltage controlled oscillators, DC/DC converters, *etc.*, all of which are prone to ASETs. This monograph deals primarily with operational amplifiers and voltage comparators because they have been the object of most of the ASET studies to date.

In purely analog systems, ASETs may be considered a form of noise. For example, a meter for measuring electric current contains an amplifier whose gain is adjusted according to the magnitude of the current to be measured. The noise in the system manifests itself as a continuous series of small glitches such that the current reading oscillates about the expected or average value. Glitches caused by ASETs are indistinguishable from noise, except that some of them are a great deal larger and, therefore, more pernicious.

In a mixed-signal system, ASETs originating in the "analog" portion may become latched in a follow-on circuit. In the process, the ASET is converted into a SEU, so that what starts out as an ASET, ends up having characteristics akin to that of a digital upset. For example, the ASETs in the LM139 comparator that caused resets in the processor on board MAP were essentially large noise pulses that turned into digital SEUs in the follow-on circuit.

Not all ASETs that appear at the outputs of linear ICs will propagate through the follow-on circuits and cause failure. All the circuits together constitute a subsystem and the subsystem's bandwidth restricts propagation to ASETs whose amplitudes exceed some minimum value for a minimum time. Another condition is that the ASETs must be sufficiently large not just to reach a sensitive follow-on circuit, but to actually trigger a change of state. Those ASETs that do not meet these conditions will have no effect on the subsystem.

Comparators are usually used in applications where their outputs have digital character, which means that large ASETs are always a problem. In contrast, op-amps are used in a wide variety of applications, including power-supply circuits where their outputs are routinely filtered to remove noise. Those same filters are also effective at removing ASETs, so that no additional mitigation is necessary for power-supply circuits. However, in applications where the outputs of op-amps cannot be filtered, ASETs present a very real problem for the circuit designer.

Op-amps produce ASETs with a variety of shapes and sizes. **Fig. 1** shows examples of ASETs from a single device, the LM124 operational amplifier [BU04a], Some ASETs are positive, some are negative, and some are bipolar. Some are of very short duration while others

are much longer. Many factors affect ASET shapes including (a) ion strike location, (b) energy and nuclear charge of the incident ion, and (c) the device operating configuration (input voltage, output impedance, supply voltage, gain, *etc*). Because the operating configuration determines ASET shape and sensitivity, it is essential to test the device in precisely the same configuration as will be used in space. Measurements made for one operating configuration are not necessarily applicable to another. This has profound implications for testing, which must be performed for each unique operating configuration – an expensive and time-consuming proposition that will be addressed in a later section.
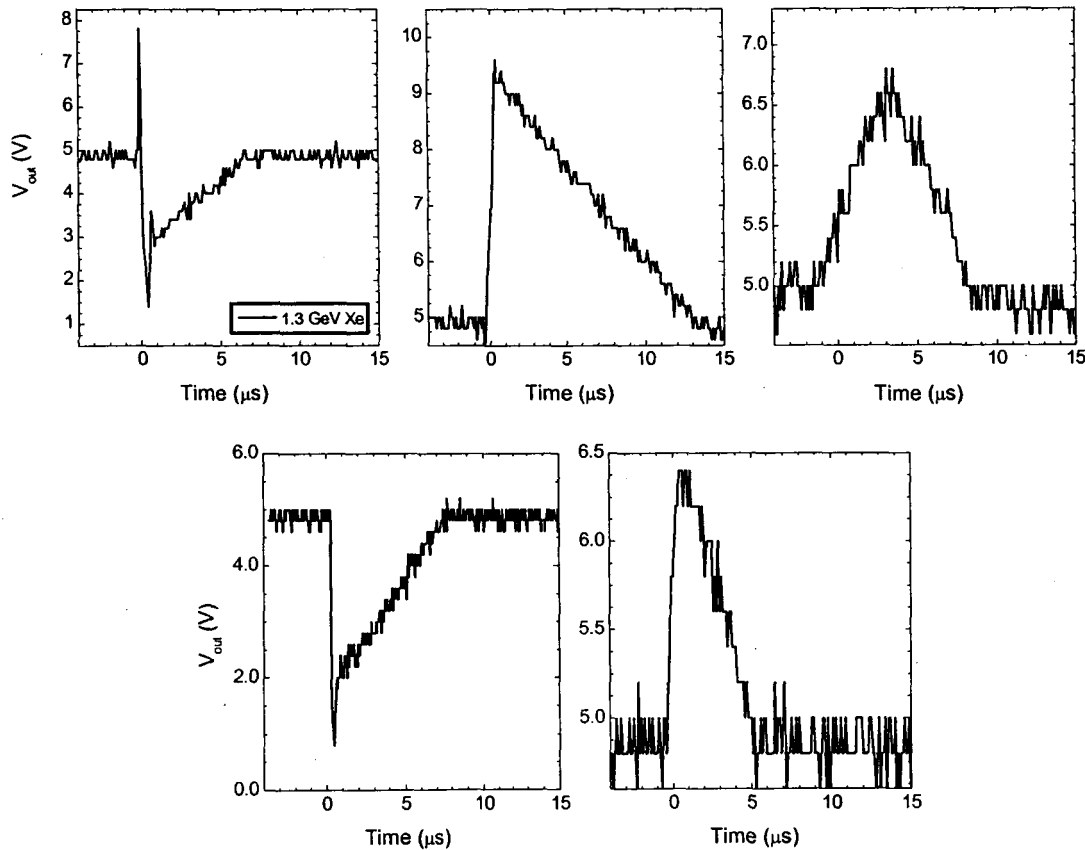

Fig. 1. Variety of ASETs produced in the LM124 operational amplifier by high-energy heavy-ion irradiation [BU04a]

The ASETs depicted in Fig. 1 are typical of the variety of shapes that occur in operational amplifiers. ASETs in voltage comparators are less complex as they are unipolar and vary only in amplitude and width. ASETs in voltage references are similar to those in voltage comparators. In contrast, ASET signatures are quite different in other types of linear circuits, such as pulse width modulators (PWMs) and voltage controlled oscillators (VCOs). **Fig. 2** shows an ASET caused by an interruption in the train of pulses at the output of a PWM [HO03]. Such interruptions may take the form of dropped pulses, shortened pulses, or phase shifts. **Fig. 3** shows that an ASET in a VCO causes a distortion in the output signal for a time that spans more than one clock period [CH03]. These temporary operational malfunctions qualify as ASETs because they are caused by voltage transients induced by ions passing through the circuits. In each case, the device returned to its normal mode of operation following the ASET.
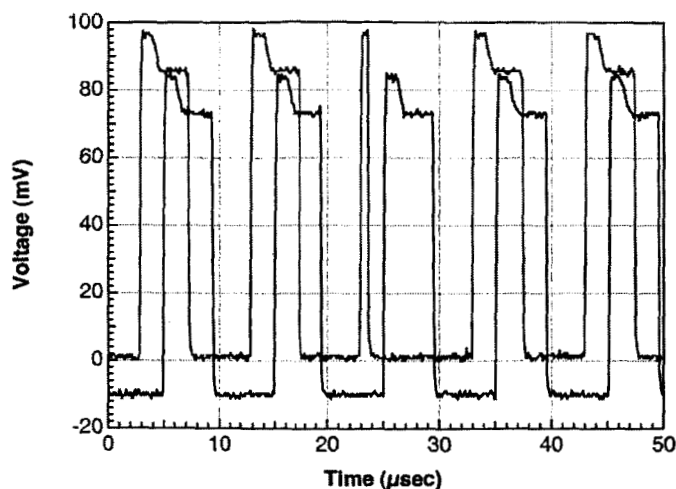
Fig. 2. Two pulse trains from a SG1525A pulse-width-modulator showing a shortened positive pulse in one of the trains [HO03].

ASETs are a threat to linear ICs operating in space for a number of reasons. One is the low linear energy transfer (LET; *see below*) threshold (~1 MeV·cm^2/mg) that prevails for some configurations resulting in large numbers of heavy ions in space being capable of producing ASETs. [KO93] Another is the combination of large amplitudes (rail-to-rail) and long durations (typically tens of microseconds, but some as long as milliseconds) that enhance the likelihood of an ASET propagating through a series of follow-on circuits before eventually becoming "latched". Finally, the low energy threshold (~30 MeV) measured for proton-induced ASETs in some devices means that a large number of protons in space will be able to generate ASETs. Since protons are by far the most abundant positive ion species, circuits sensitive to proton-induced ASETs will exhibit high rates in space [NI96].
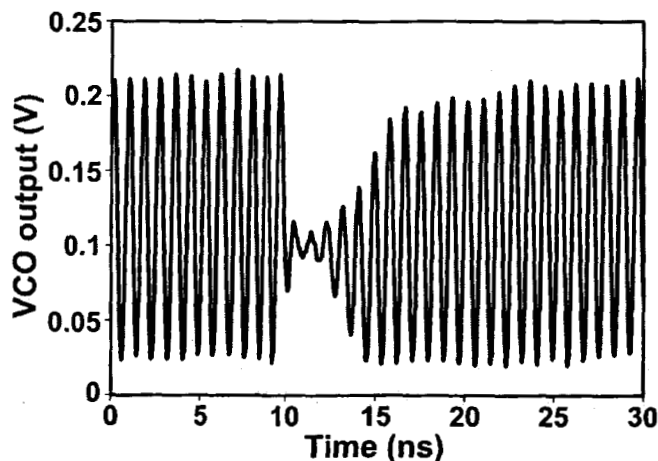

Fig. 3. Output voltage as a function of time for a voltage controlled oscillator. The ASET appears as a reduction in the amplitude that lasts for about 10 cycles [CH03].

3.0 ASET Generation

Integrated circuits on board spacecraft are exposed to energetic positive ions with masses that span the Periodic Table from Hydrogen to Uranium. Most of those ions are capable of producing ASETs in ICs. A detailed presentation of the many characteristics of the radiation environment relevant to ASET production is beyond the scope of this monograph. The reader is referred, instead, to an excellent short course presented in 1997 [BA97].

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This section discusses the physical mechanisms responsible for ASETs. Positive ions interact with the bound electrons and nuclei of the host atoms in the IC to produce ASETs. The process consists of three steps [XA92]. The first step involves energy deposition by an ionizing particle in or near a sensitive volume in a device. The second step involves charge separation and collection in the sensitive volume that encompasses the electric field of a p-n junction. The third step involves the circuit response, which includes the propagation of the ASET from its origin through the circuit to the output.

3.1 Energy Deposition

Charged particles traveling through matter, such as silicon, lose energy as they interact with the electrons and nuclei of the constituent atoms. The rate of energy loss is dominated by the Coulomb interaction between the nucleus of the incident ion and the bound electrons of the silicon atoms. In the process, the bound electrons absorb sufficient energy to break away from the silicon atoms, leaving behind mobile "holes".

The energy loss (dE) per unit distance (dx) via ionization depends on the charge (ze) and energy $(\frac{1}{2}m_o v^2)$ of the incoming particle, and may be calculated with Bethe's formula:

$$-\frac{dE}{dx} = \frac{4\pi e^4 z^2}{m_o v^2} N \cdot Z \cdot B(m_o, v, I) \tag{1}$$

In the formula, N is the number density and Z is the atomic number of the atoms in the absorbing matter. I is the average excitation potential, which is 3.6 eV for silicon. $B(m_o, v, I)$ is a slowly varying function of energy. The equation clearly shows that the energy lost by an ion traveling through material is greatest for highly charged particles (large z) with relatively low energy (small v). [KN90] The standard metric for energy loss is known as linear energy transfer (LET), defined as the energy transferred to the material, normalized to the density (ρ) of the material,

$$LET = \frac{1}{\rho} \cdot \frac{dE}{dx} \tag{2}$$

Fig. 4 is a plot of dE/dx versus energy for different ions in silicon. The figure shows that at low energies the LET increases with energy until it reaches a maximum, after which it decreases with increasing energy. The figure also shows that ions with larger nuclear charges have higher LETs.
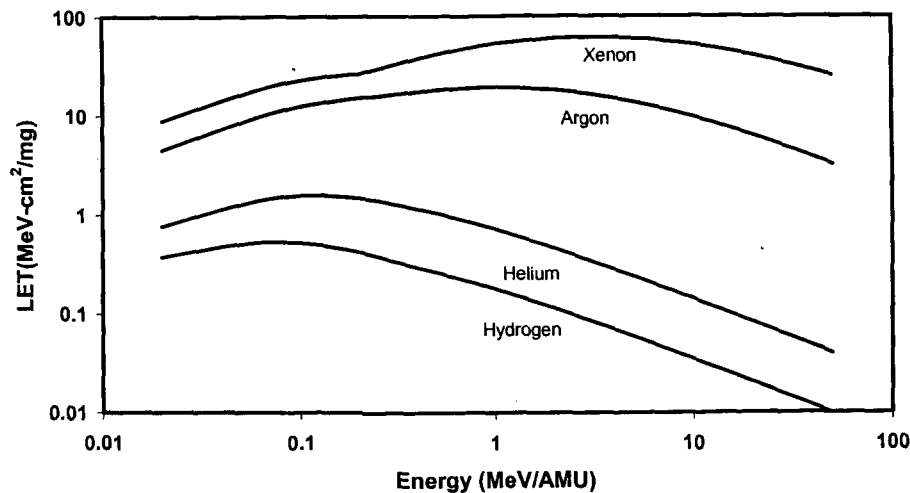

Fig. 4. LET as a function of ion energy (MeV/amu) for four different ions with very different masses.

Fig. 5, which is derived from Fig. 4, depicts the dependence of dE/dx on distance from the surface. When an incident ion with a large energy first enters a slab of silicon it has a relatively low LET because it has little time to interact with the bound electrons. As it continues on its path through the silicon, the particle loses energy and its LET gradually increases. Eventually, the LET saturates and additional energy loss leads to a decrease in the LET. The maximum energy loss occurs near the end of the path and is referred to as the Bragg peak. For a particle to trigger an ASET at a deep junction – on the order of 10 μm below the surface for typical bipolar devices – it must have sufficient range. Range is a parameter that should be considered carefully whenever testing with low-energy heavy ions at accelerators is planned. Data will be presented in a later section showing the effects of range on ASET cross-section. Ionizing particle radiation in space has a wide range of energies and, consequently, a wide range of LETs and ranges.
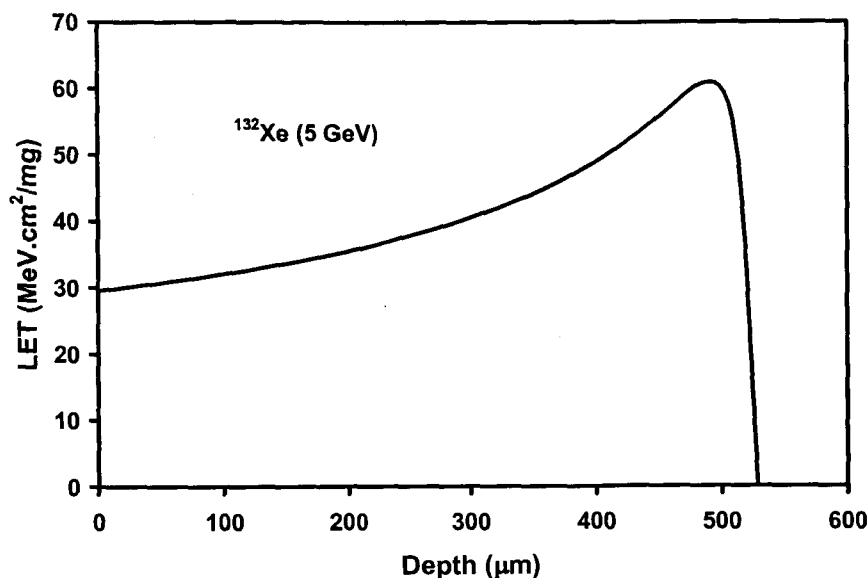

Fig. 5. LET as a function of depth in silicon for a ^{132}Xe ion with an energy of 5 GeV. The range is about 520 μm and the maximum is referred to as the Bragg peak.

The electrons initially liberated by the interaction are called delta rays. They have relatively high energies and move rapidly away from the point of generation. As they do so, they interact with the bound electrons in other atoms, giving up some of their energy in the process. The delta ray range is directly related to the ion energy, with higher energy ions yielding higher energy delta rays. Even for the highest energy ions, most of the secondary electrons are produced by the delta rays in less than a micron. The track of charge is generated in less than a picosecond, and its length is given by the range of the incident ion. For all practical purposes, the charge track's initial diameter may be assumed to be less than a micron.

Incident particles also lose energy through elastic and inelastic scattering with the nuclei in the host material. During elastic (Coulomb or nuclear) scattering, the incident particles and the constituent nuclei recoil and as they move through the lattice they lose energy by direct ionization. If the recoiling nuclei create sufficient charge in a localized sensitive volume, an ASET may be produced. In inelastic scattering, the incident ion collides with a nucleus, causing it to break apart. Hosts of smaller particles are emitted that also lose energy via direct ionization. Nuclear scattering occurs relatively infrequently ($\sim$ 1 incident particle in 10^5 collides with a nucleus) so indirect processes may be ignored for heavy ions. An interesting case is that of protons whose LETs are too low to produce ASETs via direct ionization, but whose flux in space is sufficiently large that the relatively rare nuclear collisions able to produce ASETs sometimes

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actually dominate all other sources. Examples of proton-induced ASETs will be given in a later section.

Following a nuclear interaction, a constituent atom is knocked out of its equilibrium lattice position, leaving behind a vacancy. The nucleus is now in an interstitial site. The presence of the vacancy and the interstitial destroy the local periodicity of the lattice. This form of energy loss is called "non-ionizing energy loss" (NIEL). Associated with the disrupted lattice are traps and recombination centers that limit minority carrier lifetime and degrade charge-carrier mobility, two parameters that determine bipolar transistor performance [MA99]. This monograph will largely ignore the effects of lattice damage except to note that high damage levels affect the ASET amplitude and width [BU01].

3.2 Charge Collection

All transistors contain p-n junctions. It is, therefore, instructive to consider first charge collection in an isolated diode. **Fig. 6** is a diagram of a simple p-n junction diode. There are two modes of operation for the diode – reverse bias and forward bias. With a negative voltage applied to the p-doped side, the diode is reverse-biased and a large potential barrier prevents current from flowing. A positive voltage greater than 0.6 V applied to the p-doped side forward biases the diode and reduces the potential barrier to such an extent that an electric current can flow, with electrons moving from the n-doped region to the p-doped region and holes move in the opposite direction.
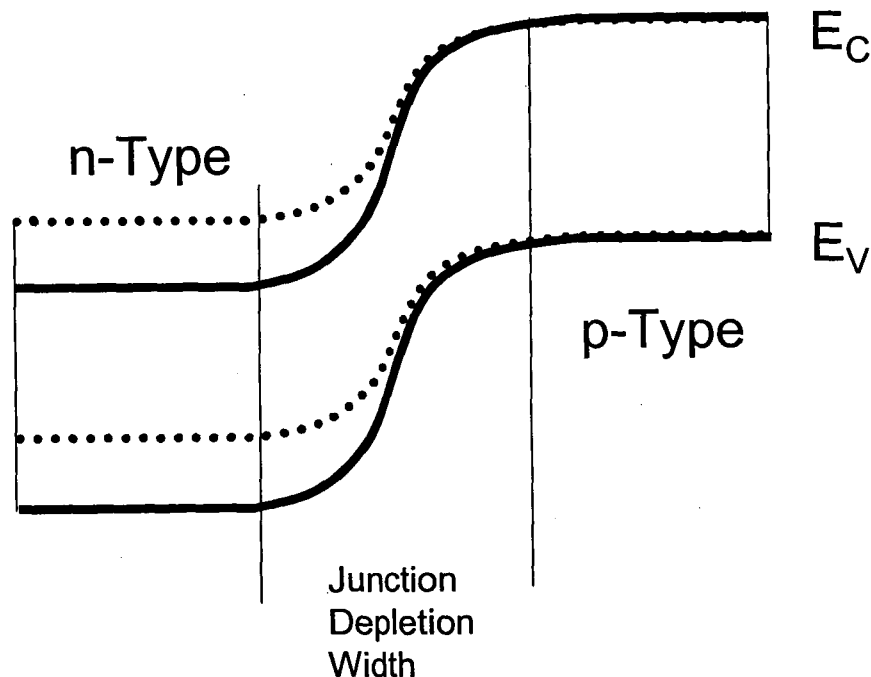

Fig. 6. Energy-band diagram for an unbiased p-n junction (solid line), showing the conduction (E_c) and valence (E_v) bands. The slope of the energy bands is related to the strength of the electric field in the depletion layer. If a positive bias is applied to the p-type region, the junction is forward biased, the slopes of the energy bands are reduced (dotted lines), indicating a smaller electric field, and the depletion width is reduced.

Ionization involves the creation of both electrons and holes. Electrons and holes created in the depletion region of a reverse-biased p-n junction will be separated by the junction's electric field. **Fig. 7** shows the flow of injected charge carriers in a reverse-biased p-n junction. The electrons will move to the n-type region and the holes to the p-type region. This process, known

as "drift", is efficient at collecting charge because the physical separation prevents most of the electrons and holes from recombining. The charge separation gives rise to an opposing electric field that partially cancels the existing junction electric field. The potential in the n-type region is lowered by the influx of electrons and the potential in the p-type region is increased by the influx of holes. It is the flow of charges across a junction that produces an ASET.
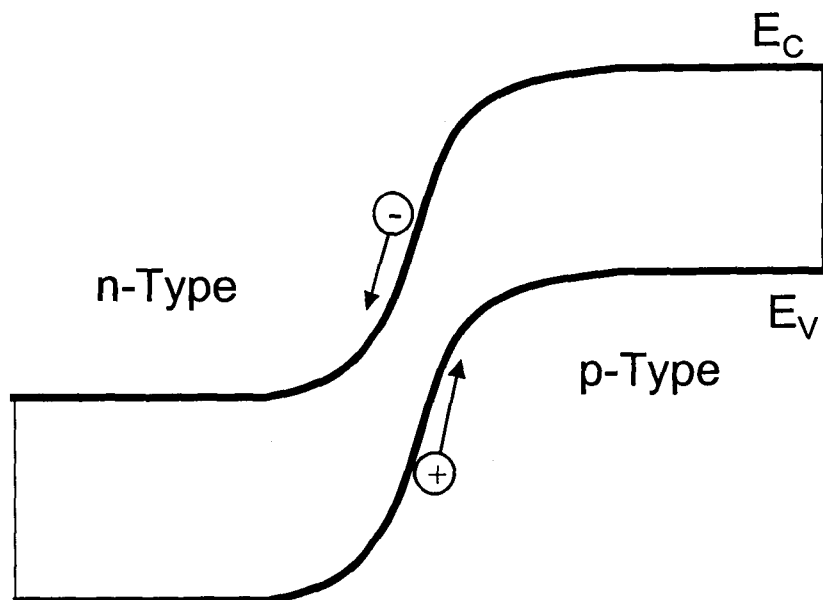

Fig. 7. Movement of charge carriers generated in the depletion region of a reverse-biased p-n junction. Under reverse bias both the electric field and the depletion width increase. The separation of the charge sets up an electric field opposite to the inherent field, thereby reducing its magnitude. The movement of charge changes the potential on the nodes.

Generally, the density of electrons and holes immediately following the formation of the charge track is so high that the junction electric field along the track is screened out. The effect is to distort the depletion layer so that it extends along the edge of the track [DU95]. The extended depletion region results in the collection of additional charge that increases the chances of an ASET occurring. Another effect caused by the initial high density of electrons and holes in the track is termed the "shunt" effect. It occurs where there are at least two junctions in close proximity. For example, if two n-type regions are separated by a thin p-type region, (as would be the case in a vertical n-p-n transistor) a charge track could electrically short the two n-type regions. The result is a large current flow and enhanced charge collection, i.e., more charge is collected than deposited. Computer simulation of an ion strike in a vertical n-p-n transistor suggests that the shunt effect occurs during the initial phases of charge collection [JO00].

When an energetic ion produces a long charge track that passes through or near a junction, some of the charge will be generated outside the junction. That charge may eventually be collected across the junction, but first the charge must move to the edge of the junction depletion region. The movement of charge in the absence of an electric field is driven by the gradient of the charge density, a process known as "diffusion". Diffusion is a much slower process than drift, and, because there is no electric field to separate the electrons and holes, recombination is more likely. Clearly, charge collection by diffusion is much less efficient than by drift. ASETs originating in bipolar transistors are typically the result of charge collection via both drift and diffusion, with the diffusion contribution depending on the device structure and material properties. In Section 6.4, the importance of charge collection via diffusion will be illustrated with experimental results for the LM111 voltage comparator, for which charge collection takes

place over a distance of about 100 μm, well beyond the depth of the deepest junction (~10 μm). For this case, the diffusion component dominates the drift component.
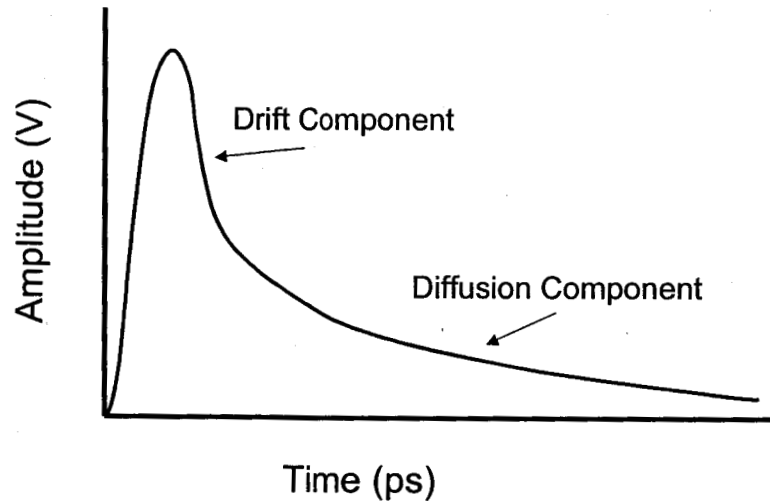

Fig. 8. Amplitude of the voltage disturbance as a function of time at a transistor junction. The figure shows both the fast component due to drift and the slow component due to diffusion.

The size of the voltage transient is, in part, a measure of the amount of charge injected by the ionizing particle. **Fig. 8** shows a voltage transient from a diode. The transient has a fast component consisting of a narrow peak followed by a slow decay. The narrow peak is due to charge collected by drift and the slow decay is due to charge generated outside the junction and collected via a combination of diffusion and drift.
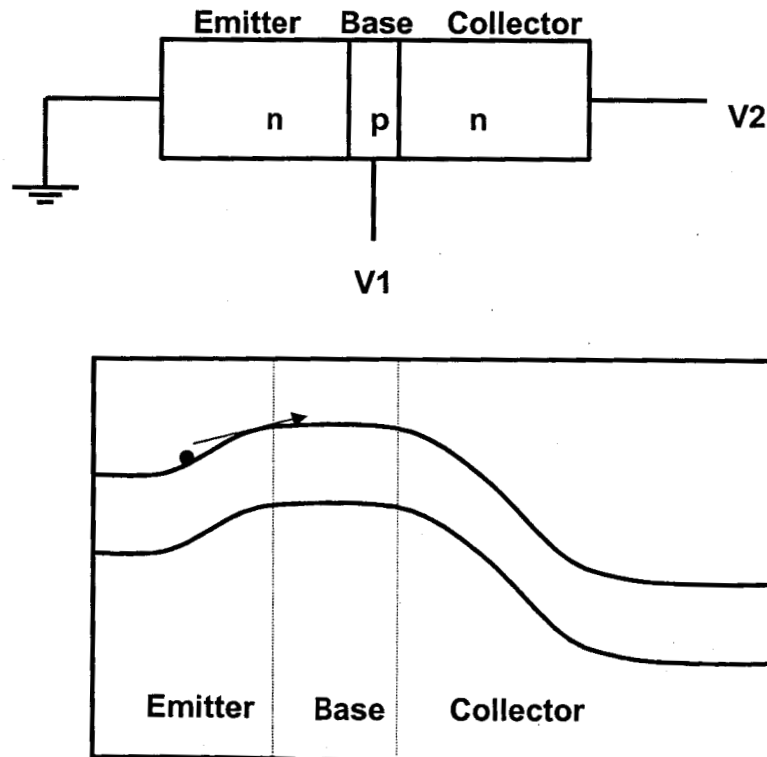

Fig. 9. (a) n-p-n transistor. (b) Energy-band diagram of the transistor operating in the forward-active mode in which the emitter/base junction is forward biased and the base/collector is reverse biased.

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Bipolar transistors in linear devices function as current-controlled amplifiers – the current flowing from the emitter to the collector is linearly proportional to the current injected into the base ($I_C = h \cdot I_E$) where h is the transistor gain. For reasons of brevity, only n-p-n transistors will be analyzed. **Fig. 9a** is a cartoon of an n-p-n transistor in which the emitter, base and collector are indicated. The transistor consists of two back-to-back p-n junctions, which act as barriers to the flow of current through the device, as previously described. Each junction may be independently forward-biased or reverse-biased. **Fig. 9b** shows the applicable energy-band diagram for the situation where the transistor is operating in the forward-active mode, i.e., the E/B junction is forward-biased and the C/B junction is reverse-biased. The application of a forward bias of at least 0.6 V across the E/B junction lowers the potential barrier sufficiently to allow current to flow from the emitter to the base. At the same time, current flows from the base contact through the base to the emitter. Transistor action (amplification) is possible because the base is intentionally made very thin to minimize recombination of carriers. That ensures that almost all the electrons injected from the emitter into the base will diffuse across the base to the edge of the C/B junction. The large electric field of the reverse-biased junction will rapidly sweep the electrons into the collector. For this mode, the electron current flowing from the emitter to the collector is amplified by the hole current injected into the base.

From the discussion in the previous section regarding charge collection in diodes, one can conclude that, to a first approximation, charge deposited in the reverse-biased C/B junction will be much more effective at producing ASETs than charge deposited in the forward-biased E/B junction. The electrons and holes that appear in the C/B junction are rapidly separated by the large electric field and those holes that arrive at the base raise its potential. The effect is to increase the forward bias across the E/B junction, which results in more current flowing through the device. A relatively small amount of charge injected into the base will cause a large increase in the current from the emitter to the collector due to amplification inherent in the device. Eventually, the excess holes in the base recombine, the forward bias is reduced, and the excess current abates. In reality, the charge collection processes leading to the formation of ASETs are more complicated because of the interactions of the charge carriers with the junctions. Calculations using a device simulator reveal the complicated nature of charge collection at very short times after the ion strike [JO00], [JO02]. To a first approximation, the complicated processes may be ignored because they occur over such short time intervals that their contributions to the total amount of collected charge are relatively small.

There is another mode for increased current flow through the transistor induced by heavy ions – the shunt effect. As described in the section on charge collection, the shunt effect occurs when a dense charge track induced by a heavy ion passes through two junctions, such as the E/B and C/B junctions. The dense track of charge screens out the junction fields and allows current to flow from the emitter to the collector, driven purely by the bias between the two regions. Section 4 reports on simulation results for comparators that indicate that immediately after the charge track is generated, charge collection proceeds via the shunt effect between the emitter and substrate regions. After the shunt effect is completed, additional charge is collected for some time via normal diffusion and drift processes.

Op-amps and voltage comparators contain numerous bipolar transistors connected in a variety of different configurations dictated by their specific functions. Many of the transistors in linear devices have been found to be sensitive to ASETs when probed with a pulsed laser. For example, 20 of the 22 bipolar transistors in the LM119 op-amp show some degree of sensitivity. In a particle radiation environment, very few of the transistors will actually contribute to system upsets because many transistors have high thresholds and the ASETs they produce are of small amplitude [BU01]. To identify the most sensitive transistors requires a good understanding of bipolar circuit theory. Failing that, one could make use of circuit and device simulators, a pulsed

laser, or a focused ion microprobe. Among the most sensitive transistors in op-amps and voltage comparators are those in the input stage, specifically those that form the differential input pair. In fact, for small values of differential input voltage, the input transistors in voltage comparators dominate the circuit's ASET sensitivity.

3.3 Circuit Response

In is instructive at this point to see how a current pulse in a bipolar transistor produces an ASET at a circuit output. Propagation through a simple op-amp will be considered [HTTP]. **Fig. 10** shows a basic op-amp circuit. The input stage contains a differential amplifier consisting of a pair of identical n-p-n bipolar transistors, T1 and T2. The differential amplifier also contains two identical resistors, R_1 and R_2. Both emitters are connected to a constant current supply, T3. One of the output transistors (T5) is driven directly by the input pair and the other, T6, is driven via transistor T4. For a symmetric output around 0 V, $R_5 = R_6 = R_7 = R_8$. All the transistors are assumed to have the same high value of gain, which means that they all have negligible base currents. For this analysis all the base currents are assumed to be zero.
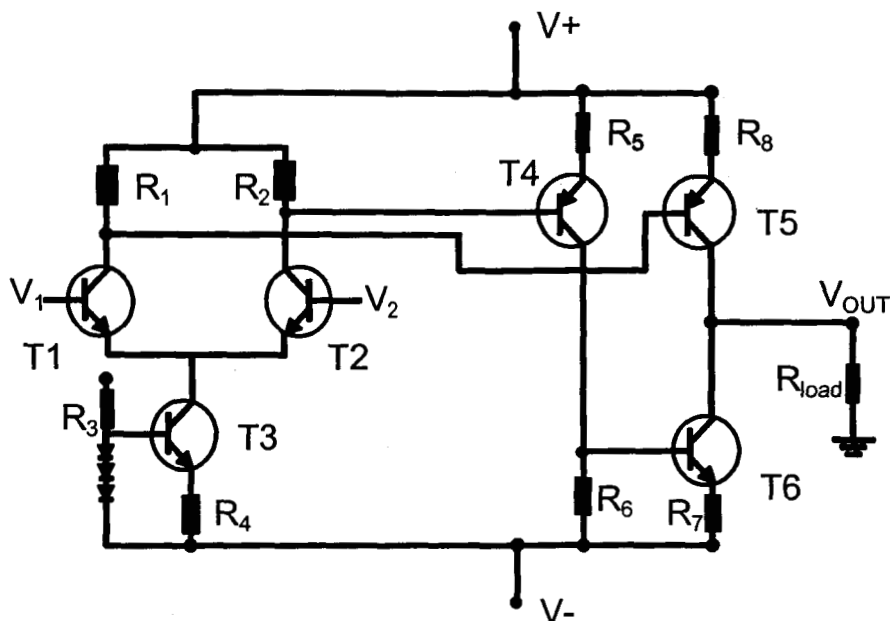

Fig. 10. Circuit elements for a simple operational amplifier consisting of six transistors [HTTP].

If $V_1 = V_2$ then $I_1 = I_2 = I_E/2$ and the current flowing through T4 and T5 will be the same. This also implies that the same current flows through R_5 and R_6 so that the potential difference across R_5 is the same as that across R_6. The diode ensures that the potential drop is the same across R_7 and R_5, so that when $V_1 = V_2$, the same current flows through T5 and T6. Therefore, the output voltage is midway between V+ and V-, i.e., at 0 V.

An increase in V_1 causes an increase in I_1 which, in turn, raises the voltage at the emitter of T1. Since the two emitters are connected, the voltage on the emitter of T2 is also increased, which causes a reduction in voltage across the E/B junction of T2. As a result, the voltage on the base of T5 increases and that on the base of T4 decreases. More current will flow through T5 and less through T6 which will raise the output voltage. Analysis of the circuit shows that ΔV_{out} is proportional to (V_1-V_2). The same analysis shows that if V_2 increases relative to V_1, ΔV_{out} will drop by an amount proportional to (V_2-V_1).

Based on the above analysis, it is relatively straightforward to explain how ASETs are produced when charge is injected into either one of the input transistors. Charge injected into the

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C/B junction of T1 will cause the E/B junction to be slightly more forward biased. As a result, I_1 will increase and I_2 will decrease. An increase in I_1 increases the voltage drop across R_1 and a decrease in I_2 decreases the voltage drop across R_2. Both voltage transients will propagate through the op-amp, the positive transient to the base of transistor T4 and negative transient to the base of T5. T5 becomes less conducting and T6 becomes more conducting. Together they cause the output voltage to drop. When the excess charge deposited in transistor T1 disappears, the voltage drops across R_1 and R_2 return to their original values and so do the voltages on the bases of T5 and T6. When that happens, V_{out} gradually recovers and the ASET disappears.

The discussion above is for a very simple op-amp that was used to illustrate how ASETs propagate through linear circuits. Practical op-amps contain multiple gain stages in addition to the input and output stages. To prevent op-amps from going into spontaneous oscillation, internal capacitors (compensating capacitors) are added that reduce the op-amp's bandwidth. The inclusion of the capacitor, which functions as a low-pass filter, can have a significant effect on the ASET pulse length. For instance, although charge collection in the input transistor of the LM124 op-amp occurs over a time interval lasting hundreds of nanoseconds, the presence of the compensating capacitor dampens the ASET, which has been shown experimentally to last on the order of tens of microseconds. Similarly, the OP293 (to be discussed later) has an even smaller bandwidth (25 KHz) resulting in ASETs that last on the order of hundreds of microseconds.

The analysis above is for ASETs originating in the differential input transistors of a very simple op-amp circuit. Some op-amps contain up to fifty transistors, many of which may be sensitive to ASETs. Clearly, the analysis to determine which ones are ASET sensitive is then quite a bit more complicated.

3.4 Critical Charge

Critical charge (Q_{crit}) is a metric used primarily for comparing SEE sensitivities of digital ICs [SE92]. It is defined as the minimum amount of charge required for producing a SEE. Q_{crit} is a circuit property that may be calculated from the product of the node capacitance (C) and the minimum voltage excursion (ΔV) required for a SEE. Q_{crit} may also be obtained experimentally by determining the threshold LET (LET_{th}) provided the collection depth (d) is known. At threshold, Q_{crit} equals the collected charge (Q_{col}), which, to a first approximation, is given by the product of LET_{th} and d. In some situations, the value of d is a guess, whereas in others it can be estimated using geometrical factors, such as the depth of an epitaxial layer. On the other hand, if the critical charge is calculated and the LET threshold measured, the charge collection depth may be obtained from the value of (Q_{crit}/LET_{th}). This is important information for the experimentalist wishing to measure SEU cross-section as a function of ion LET, because ion energies must be selected so that the ion ranges exceed the charge collection depth.

The concept of critical charge may also be applied to linear circuits. The value of Q_{crit} is somewhat arbitrary for linear devices since it must be related to a measurable quantity, such as ASET amplitude. Therefore, any definition of Q_{crit} should include the criterion used for measuring it. Q_{crit} may be defined as the minimum amount of charge required to produce an ASET of a given amplitude in a particular operating configuration. Q_{crit} may also be defined with respect to a system application for which some minimum amount of charge must be collected to cause a system upset.

Experiments have shown that the LET thresholds for some linear bipolar devices are small, on the order of 1 MeV·cm²/mg, which is equivalent to depositing 0.01 pC per micron [KO93]. Such a low LET begs the question as to whether the cause is a small Q_{crit} and a small collection depth or a large Q_{crit} and a large collection depth. To answer this question, Q_{crit} was determined for two linear circuits – the LM111 voltage comparator and the LM124 op-amp – using a variety of experimental techniques to be discussed later. Q_{crit} for the most sensitive transistor in each IC

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was also calculated from computer simulation. Results indicate that the critical charge is approximately 1 pC for each, which suggests that the collection depth is about 100 μm. Evidently, for these devices, charge is collected from well beyond the deepest junction, which is about 10 μm below the silicon surface. To measure ASET cross-sections accurately requires that the ions have ranges on the order of 100 μm, a requirement that limits the choice of accelerators to those that are able to supply high-energy ions.

4.0   ASET Simulation via Computer Modeling

Simulation is an important tool for studying ASETs. It requires the development of models to represent the devices (transistors, diodes, etc) in an IC. Once the model has been generated and validated, simulation may be used to obtain a great deal of information about ASETs that are not easily obtainable by any other means. In particular, modifications to ASET shapes and sensitivities resulting from changes in design and manufacturing can be studied. Another potent application of simulation is to the explanation of, and evaluation of possible mitigation approaches for anomalous ASETs. It may also be used to determine whether ASETs generated in an IC, such as an operational amplifier or voltage comparator, will propagate through a variety of potential follow-on circuits that have not yet been built.

There are two approaches to computer simulation of ASETs. One combines a device simulator with a circuit simulator, whereas the other uses only a circuit simulator program. The latter approach, which may be used when the response time of the circuit is much slower than the charge collection time, is the approach of choice because it is much less computer intensive.

4.1   Device Simulation

There are a few commercial device simulators available that may be used to simulate the response of a transistor to the injection of charge by an ion passing through or near the transistor. A device simulator solves the set of equations that govern the movement of charge in the device. The equations of interest are Maxwell's equations, Poison's equation, the continuity equations and the carrier transport equations. Since these equations cannot be solved analytically, the device simulator program solves them numerically. In this approach, a transistor of interest is selected as the source of an ASET and the equations are solved in either two or three dimensions. (For greater accuracy the device should be simulated in three dimensions, but the computer resources needed are considerable so most simulations are done in two dimensions.) Information needed for the device simulator includes doping levels, geometrical layout, and layer thicknesses, all of which must be obtained from the IC manufacturer or from reverse engineering. The response to the passage of an ion traversing a transistor is obtained by injecting charge along a track that simulates the charge track produced by a heavy ion. The charge density along both the track length (~ 100 μm) and track radius (< 1 μm) are assumed to be constant. (For a laser beam, the radial charge density profile is a simple Gaussian whose width varies along the track as determined by the optical components.) The movement of the charge (via drift and diffusion) and the response of the transistor's terminal voltages are calculated as a function of time.

The device simulator may be combined with a circuit simulator to calculate how the circuit as a whole responds to the changes in voltages at the transistor terminals. This procedure must be repeated for charge tracks at various locations throughout the transistor, because the sizes and shapes of ASETs depend on ion strike location. Each transistor in the linear IC must be simulated in turn, a mammoth task when one considers that some ICs contain on the order of fifty transistors. It is, therefore, not surprising that, to date, there have been no published reports on ASETs in linear ICs investigated with a combination of device and circuits simulator programs.

Device simulators by themselves have been used to study charge collection processes in isolated transistors representative of those in voltage comparators and op-amps. Most of the comparators and op-amps discussed in this monograph are manufactured using a process

optimized for vertical n-p-n devices. That process may be modified to produce three different bipolar transistor structures in the same circuit. **Fig. 11** shows the structures for the vertical n-p-n, vertical p-n-p (also known as substrate p-n-p) and lateral p-n-p transistors [PO03]. The presence of a buried n+ region under both the vertical n-p-n and lateral p-n-p structures limits the amount of charge collected via diffusion. In contrast, the substrate p-n-p has no buried layer and charge collection via diffusion may take place from well below the transistor.
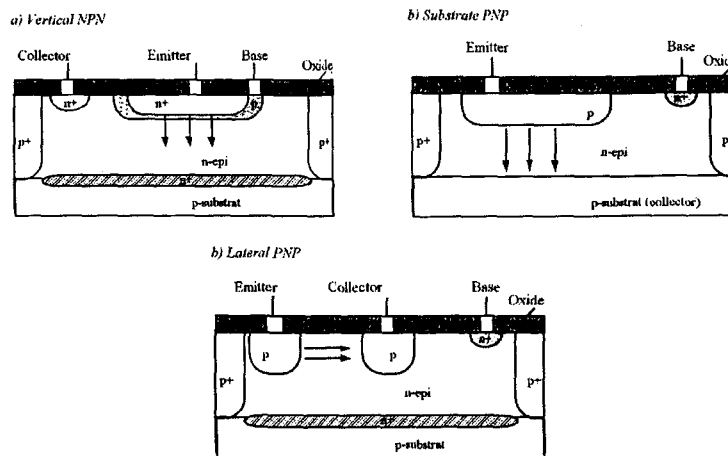
Fig. 11. Cross-sectional views of three different types of transistors all made using the same process. (a) is the vertical n-p-n, (b) is the substrate p-n-p and (c) is the lateral p-n-p.

Results have been reported for all three transistor types. For the substrate p-n-p, an ion track 400 μm long that passed through the emitter base and collector of the transistor was modeled. A bias of -0.42 V applied to the base resulted in a very small current flow, i.e., the device is very weakly turned on. **Fig. 12** shows the integrated charge collected at the emitter and collector as a function of time after the ion strike [JO00].
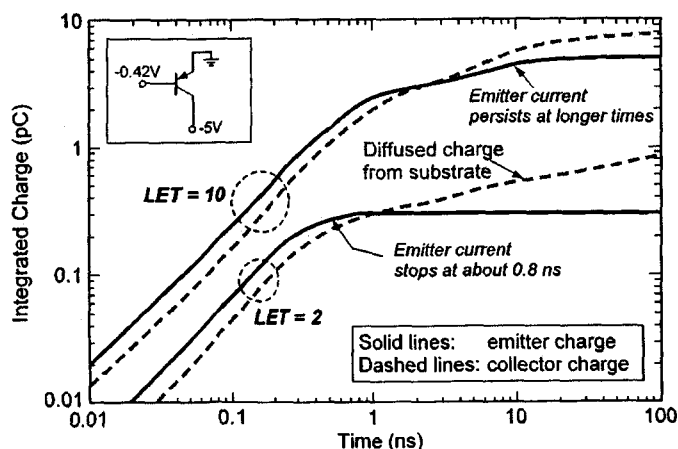

Fig. 12. Integrated charge collected as a function of time after an ion strike to a substrate p-n-p transistor. Charge collection on only the emitter and collector are plotted. Two different ion LETs are modeled. [JO00]

The results are shown for two different ions, one having an LET of 2 MeV·cm^2/mg and the other an LET of 10 MeV·cm^2/mg. At short times (<1 ns) the high-density charge track causes a collapse of the potential in the substrate and most of the current flows from the emitter to both the base and collector. Therefore, the emitter current exceeds the collector current. For ions with low LETs, the substrate potential begins to recover after 1 ns, and the remaining current flow is from

the base to the substrate and is primarily by diffusion from deep within the substrate, a process that appears to last for hundreds of nanoseconds. For the higher LET case, the increased charge density in the track causes the transistor to turn on and it stays on for up to 10 ns. The fact that the transistor turns on during the charge collection process is deduced by noting that the total charge collected for ions with an LET of 10 MeV·cm²/mg is sixteen times greater than for ions with an LET of 2 MeV·cm²/mg, even though the LET ratio is five. This suggests that the transistor is partially turned on by the injected charge.

Fig. 13 shows the excess charge (obtained by subtracting the DC current from the ion-induced current) at the collector as a function of E/B voltage for ions with three different LETs. [JO00] With the E/B voltage near 0 *V*, the transistor is turned hard off. Deposited charge is not sufficient to turn the device on, so the amount of charge collected is proportional to LET. As the E/B junction is more forward biased, the transistor gradually turns on. Any additional charge injected by the heavy ion turns the device on even more and the result is charge amplification. Therefore, with increasing E/B voltage the charge amplification factor increases, and the collected charge is not proportional to LET.
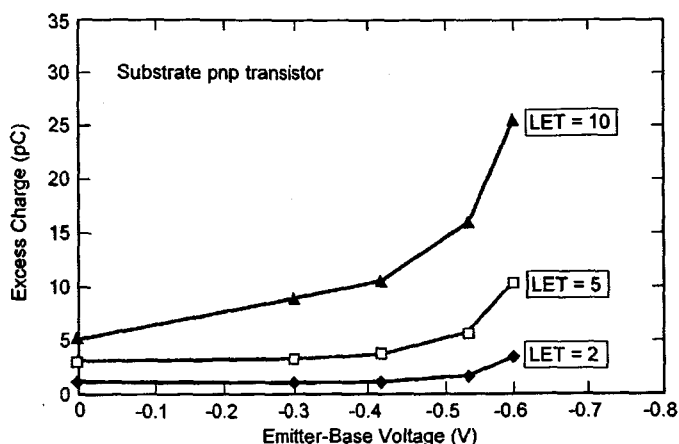

Fig. 13. Excess charge collected in the substrate p-n-p transistor as a function of emitter-base voltage for three different ion LETs [JO00]. The figure clearly shows that, with no bias across the emitter/base junction, the excess charge is proportional to ion LET. However, at a bias of -0.6 V, where the transistor starts to turn on, the excess charge resulting from the passage of an ion with an LET of 10 MeV·cm²/mg ion is greatly amplified over that produced by an ion with a LET of 2 MeV·cm²/mg.

An interesting case that reveals the complicated nature of the charge collection process in multilayer devices is the vertical n-p-n transistor. It is a four-layer device with a highly doped (n^+) buried layer below the collector that should prevent any charge collection from the substrate. Calculations show that at short times current actually flows from the emitter to the substrate, which can only happen if a "shunt" is formed by the charge track generated by the ion. The shunt lasts for a very short time, and once the fields collapse, the buried layer isolates the emitter from the substrate. However, there is continued charge collection between the collector and the substrate that contributes to the production of ASETs.

A very different case is that of the lateral p-n-p transistor for which gain appears not to be a factor in charge collection, even when the transistor is strongly forward biased. The reasons appear to be related to the low gain and long response time of the transistors, and to most of the current flowing from the base to the substrate, which does not contribute to ASET formation.

Device simulation was also used to study charge collection in n-p-n transistors that are used in fast voltage comparators, such as the LM119. Increased speed is obtained by using only vertical n-p-n transistors. Higher speeds also require higher supply currents. The n^+ buried layer

below the transistor extends from a depth of about 10 µm to about 28 µm, and is designed to eliminate charge collection from below the collector. **Fig. 14** shows the results of charge collection following the passage of an ion with an LET of 10 MeV.cm^2/mg through the device [JO02]. The E/B junction was forward biased to produce a DC current of 60 µA. The figure shows the complicated charge collection processes at very short times (<0.3 ns). That is due, in part, to the formation of a shunt between the emitter and the substrate immediately after the charge deposition. Current flows between the emitter and the substrate with very little reaching the collector. After approximately 0.9 ns the shunt disappears and the substrate current decreases, and by 7 ns no more substrate current flows. The remaining current flows between the emitter and collector and is largely over by 10 ns.
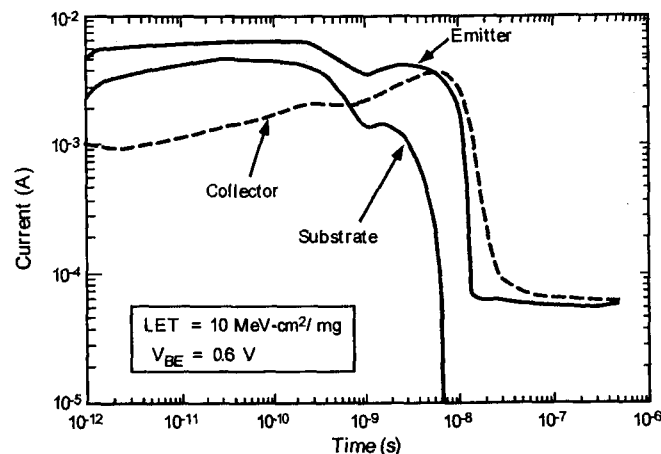

Fig. 14. Currents in the collector, emitter and substrate of an n-p-n transistor after an ion strike through the center of the emitter region [JO02]. Most of the current flow is over by about 20 ns.

One should note that the abscissa in Fig. 15 is a log scale and can be very misleading when estimating the integrated charge. The data sheet states that the response time of the LM119 is around 80 ns, and the graph shows that most of the complicated charge collection processes are over by then. In fact, the majority of the charge is collected during the decade from 1 ns to 10 ns. The complicated charge collection processes account for very little of the total collected charge.

4.2 Circuit Simulation

Circuit simulations require transistor libraries and a netlist for the IC. Transistor libraries contain all the needed parameters extracted from electrical measurements of individual transistors and a netlist describes how the transistors are interconnected. IC vendors usually do not provide that type of information because they consider their manufacturing processes and designs proprietary. One way to obtain the information is through reverse engineering. This involves isolating a transistor from the rest of the circuit by using ion-beam etching to sever all the connections [BO02]. Once a transistor has been isolated, contact to the terminals is made with mechanical probes and the current-voltage characteristics are measured. The parameters needed for the Gummel-Poon model as implemented in the circuit simulator program, SPICE, are obtained from the curves of current versus voltage across different transistor terminals.

The first step to validate the model is to apply an input signal to the IC and compare the output signals obtained experimentally and by simulation. A good illustration of the approach deals with the development of device and circuit models for the LM124 operational amplifier [BO02]. Both small-amplitude and large-amplitude square-wave signals were applied to the amplifier's input and the calculated response at the output was compared with those measured for an actual device. **Fig. 15** shows the response for a small square-wave input signal. The excellent agreement confirms that the transistor parameters used in the model are accurate [BO02]. **Fig. 16**

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shows the result obtained for the response of the LM124 to a large square-wave input signal [BO02].
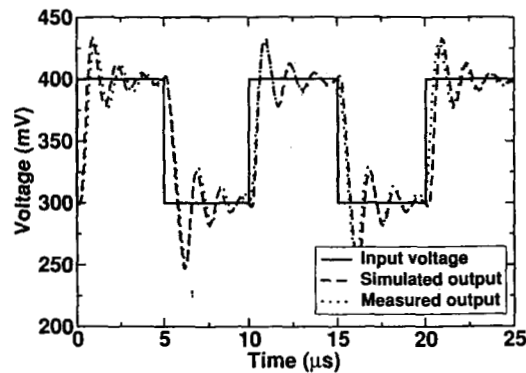

Fig. 15. Simulated and measured small-signal output waveforms for the LM124 when a square wave is applied to the input. The good agreement between the simulated and measured waveforms provides confidence that the SPICE model is accurate. [BO02]

The next step is to check that the model generates valid ASETs. Just because the model accurately calculates the output response of an IC to a particular input does not mean that it will reproduce ASETs accurately. Direct comparison between the calculated ASETs and those generated by heavy ions is one way to establish the validity of the model. A broad beam of heavy ions is of little use because there is no way to identify the origin of a specific ASET. Two other options are available. One is a focused ion microbeam and the other is a pulsed laser. Because of reasons to be discussed in Section 5, the method of choice is a pulsed laser, which has been shown to produce ASETs identical to those produced by heavy ions. A beam of laser light is focused on areas found to be sensitive to transients. Comparisons can be made between simulated and laser-induced ASET pulse shapes to gauge the accuracy of the model. Furthermore, many linear ICs contain parasitic elements that affect ASET generation but are not revealed during reverse engineering. The pulsed laser may be used to identify parasitic elements for inclusion in the model. Additional tweaking of the model might be necessary to ensure that the calculated transients match the experimental ones. These steps ensure that a valid model is used for simulation studies.
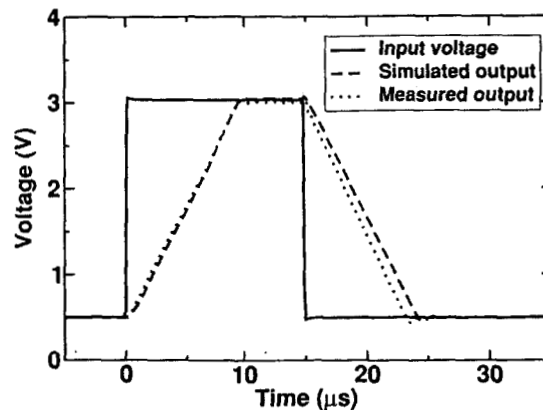

Fig. 16. Simulated and measured large-signal output waveforms for the LM124 when a square wave is applied to the input. The good agreement between the simulated and measured waveforms provides added confidence that the SPICE model is accurate. [BO02]

Considering the large effort necessary to develop and validate device and circuit models, it is really only worth it if the device is expected to have wide applications in space. An example of

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a popular device used by systems engineers would be the LM139 voltage comparator, which has been the subject of extensive modeling and experimental measurements.

To mimic the charge deposited by an ion, ideal current sources are connected across the bipolar transistor junctions. **Fig. 17** shows how the ideal current sources are connected. So long as the response time of the circuit is much longer than the time during which the charge is collected, the shape of the current pulse is immaterial. The only relevant variable is the total amount of injected charge obtained by integrating the current pulse over time. The amount of charge injected at each junction is varied by adjusting the current pulse's amplitude or duration until it matches that of an experimentally obtained ASET. If they don't match, the circuit model might have to be changed by adjusting some of the Gummel-Poon parameters or by including parasitic elements that might have been missed during the initial attempt at building a model.
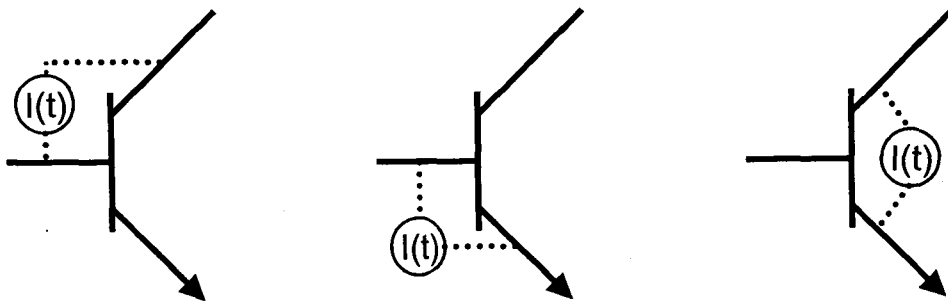

Fig. 17. Illustration showing the connections for the current generator across the collector/base, emitter/base and emitter/collector junctions.

Modeling results have proved conclusively that the ASET shape is insensitive to the injected current profile, provided the total integrated charge remains constant and provided the circuit response is slower than the charge collection time [ST02]. Further confirmation that the time evolution of the current pulse has no effect on the shape of the ASET comes from the lack of any discernable differences between the shapes of ASETs calculated with SPICE and those generated by focusing a pulse of laser light on the same junction of the same device.
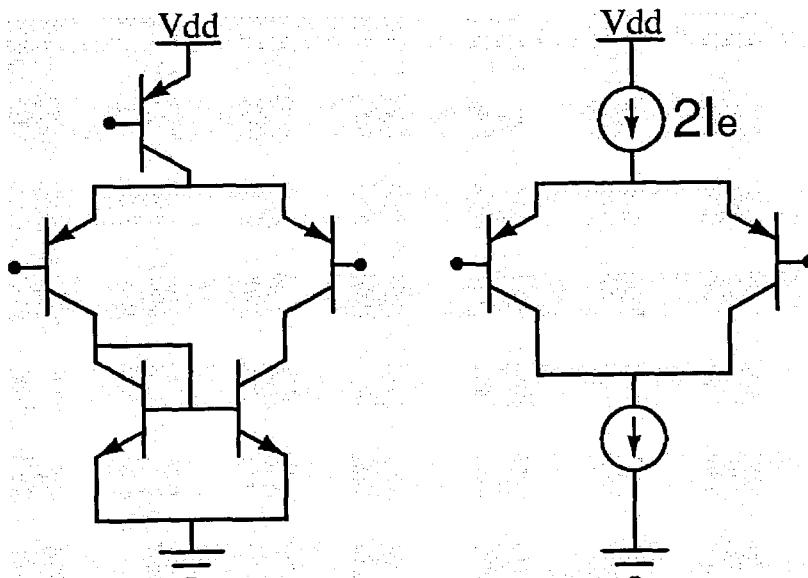

Fig. 18. The differential input circuit on the left contains three additional transistors needed for the current supply. In the macromodel, the transistors are replaced by ideal current sources.

The use of a circuit simulator for calculating ASETs requires micromodels for every transistor, capacitor and resistor in the IC. The greater the number of devices, the longer it takes to do the calculation. One possible way to speed up the calculations is to substitute some of the micromodels with a single macromodel. In fact, many of the data sheets provided by vendors contain circuit macromodels, which replace part of the circuit containing a number of devices with one simple macromodel. **Fig. 18** shows a simple example in which the biasing elements for a differential input stage of an amplifier have been replaced with current sources [BO03]. Much larger portions of a circuit may also be replaced by their equivalent macromodels. If properly implemented, macromodels are relatively accurate representations of the circuit elements they replace.

One should note that the use of macromodels to replace part of an IC when performing computer simulations of ASETs leads to the generation of ASETs that differ significantly from ASETs generated by micromodels. In fact, they do not accurately simulate ASETs at all. **Fig. 19** shows very poor agreement between transients calculated using micromodels and macromodels for the LM124 [BO03]. There are two reasons for the poor agreement. One is that the mapping between the physical IC layout and the circuit topology of the macromodel causes the removal of some sensitive junctions, as they are subsumed into the macromodel topology. This makes it impossible to use a current generator across a particular junction to simulate the ion strike. Instead, additional calculations are needed in order to determine how the parameters of the macromodel are affected by the localized charge injection. The second is that the propagation paths for the ASET may be modified as a result of the internal arrangement of the functional blocks that implement the various electrical functions of the IC. Any changes to the propagation paths will affect ASET characteristics, which are extremely sensitive to amplification or attenuation along the propagation path.
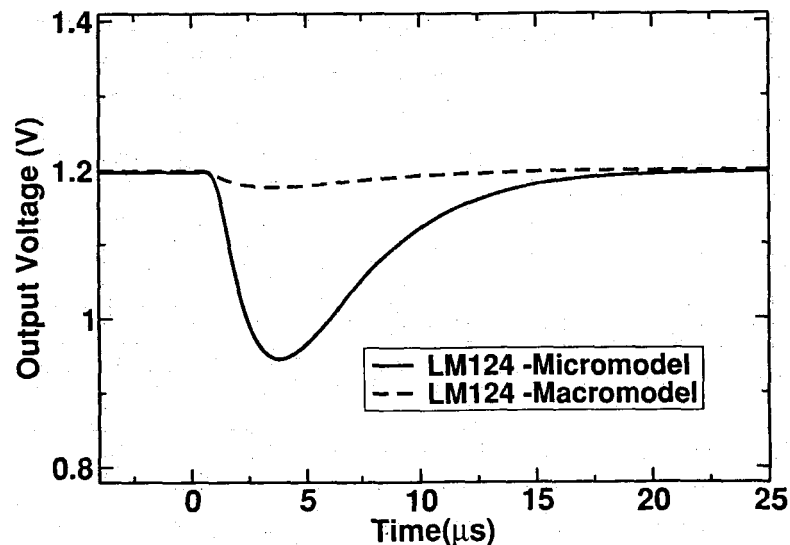

Fig. 19. Comparison of the calculated output transients of the LM124 using micromodels and macromodels. The discrepancy between the two transients is obvious, suggesting that the macromodel is not suitable for calculating ASETs.

Macromodels may replace parts of circuits through which ASETs propagate because they accurately reproduce the response of a circuit or sub-circuit to any input. One proviso is that the ASETs do not violate input requirements, such as limitations on voltage swing. Macromodels play a very useful role in reducing the calculations required for simulating ASET propagation through a system. The most efficient approach involves using micromodels to simulate ASET generation and macromodels for ASET propagation. This hypothesis was tested by analyzing

ASET propagation through a system consisting of two OP27 operational amplifiers functioning as a high-input Z differential amplifier [BO03]. **Fig. 20** shows the system. OP27 #1, in which the ASETs originated, was modeled using micromodels and OP27 #2, through which the ASETs propagated from input to output, was modeled using macromodels. To assess the accuracy of the macromodel, ASET shapes were compared with those produced when micromodels were used for OP27 #2. **Fig. 21** shows that the ASETs are almost identical, confirming that macromodels may be used for ASET analysis, provided they are not used to model the circuit in which the ASET is generated.
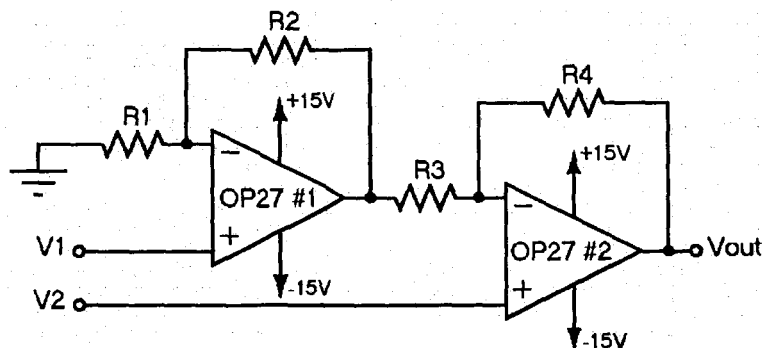

Fig. 20. Schematic of the high-input Z differential amplifier. With all resistors set to 100 kohms, Vout was equal to 2(V2-V1). The ion strikes were simulated by applying photocurrent sources to transistors of OP27#1 [BO03].
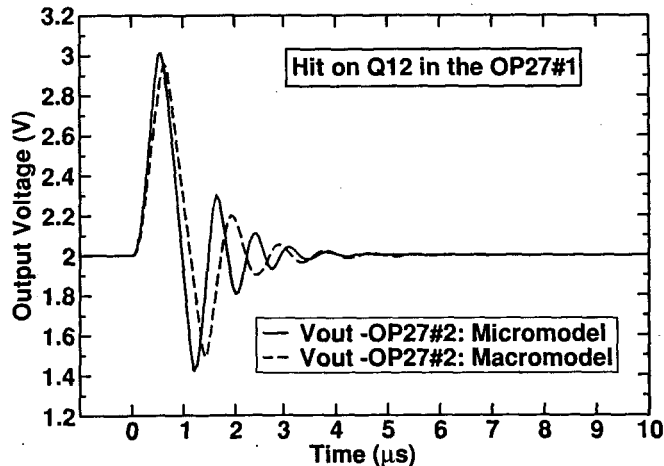

Fig. 21. Comparison of output voltage transients (Vout) originating in transistor Q12 in OP27#1 obtained using a micromodel and a macromodel [BO03].

5.0 Experimental Techniques for Measuring ASETs

Three different experimental approaches have been used for studying ASETs in analog ICs. They are unfocused and focused beams of ions from an accelerator and a focused beam of light from a pulsed laser. The application of all three techniques to the study of ASETs has proven enormously useful, providing information that is not available from a single technique. This section will be devoted to describing each technique.

The first measurements of ASETs involved exposing op-amps and comparators to a broad beam of heavy ions [KO93]. The approach adopted for detecting the ASETs is still in use today. It involves connecting the output of the linear device under test (DUT) to a storage oscilloscope

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and capturing transients with amplitudes greater than a given trigger level. With the oscilloscope's trigger level set at a relatively small voltage (~100 mV) all relevant transients may be captured. It was also recognized that merely counting the number of events in order to calculate the ASET cross-section is not sufficient because of the wide variety of ASET pulse shapes and amplitudes produced, particularly in op-amps. ASETs with large amplitudes and long durations are potentially more harmful than ASETs with small amplitudes and short durations. It was discovered that some devices (OP-15 operational amplifier, for example) produce ASETs with both positive and negative amplitudes with the largest being several microseconds in duration. The best approach is to capture and store all transients and then, at a later time, perform a detailed analysis to identify those that can trigger a particular follow-on circuit.

5.1 Accelerator Testing – Broad Beams of Heavy Ions

Accelerator testing is essential for predicting the SEE rate in space. The standard approach involves exposing an IC to a broad beam of heavy ions and counting the number of events for a fixed particle fluence (number/cm^2). The cross-section is calculated by dividing the number of events by the fluence. This procedure is repeated for several different ions, each having a different LET.
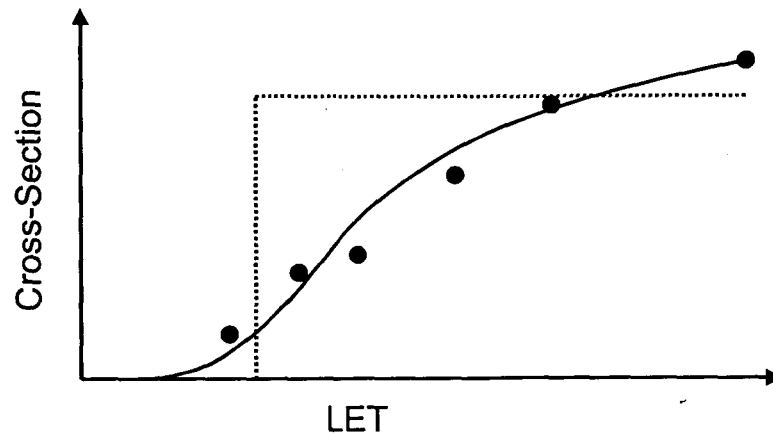

Fig. 22. Schematic showing the cross-section as a function of ion LET. The figure illustrates the data points that might be obtained from SEE testing of a part using heavy ions. The solid line is a best fit to the data points using a Weibull curve. The dashed line is a step function that would describe the cross-section for the ideal case where the sensitive volumes are all the same size, where the sensitivity does not vary across the surface, where the ions are normally incident on the device, and where there is no diffusion.

Fig. 22 shows schematically two curves of cross-section versus LET. One is based on a simple model that considers ions normally incident on a sensitive volume consisting of a rectangular parallelepiped. (RPP) The other is representative of actual measurements. For the simple model, σ(LET) is a step function with a threshold (LET$_{th}$) and a saturated cross-section (σ_{sat}). The step-function dependence may be explained by noting that at normal incidence, the amount of charge deposited in the sensitive volume is proportional to the product of ion LET and the thickness of the sensitive volume (d) so that only those particles with LETs greater than the threshold can produce SEEs. σ_{sat} is equivalent to summing the surface areas of all the RPPs.

In reality, measured cross-section curves deviate from the step function in that they increase gradually with LET above the threshold. Also, many measured cross-section curves do not saturate. The gradual increase may be attributed to spatially non-uniform charge-collection efficiency within the sensitive volume and to contributions from multiple junctions having different thresholds. The failure of the cross-section to saturate at high LETs is, in some cases, due to charge collection by diffusion from outside the junction volume.

Accelerator beam time may be used more efficiently by irradiating with just a few distinct ions, each with a different LET. Measurements may be performed at intermediate values of LET by rotating the device to change the angle of incidence. This approach is based on the assumed existence of a sensitive volume in the form of a rectangular parallelepiped. **Fig. 23** shows that, for non-normal incidence, the total charge deposited in the RPP is proportional to (LET·d·sec(θ)) as the ionizing particles travel a greater distance through the sensitive volume. Cross-section is then plotted as a function of effective LET, defined as LET·sec(θ).

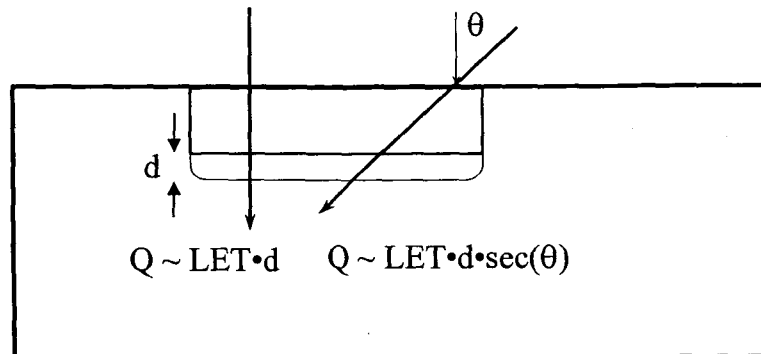$$Q \sim LET \bullet d \qquad Q \sim LET \bullet d \bullet sec(\theta)$$

Fig. 23. Comparison of the charge collected for a normally incident ion passing through a depletion layer of thickness "d" with that for an ion incident at an angle θ.

An issue that must be considered when measuring ASET cross-sections, particularly when the incident accelerator ions have low energies or are incident at large angles, is the ion range. Sensitive junctions in some bipolar transistors are quite deep (~10 μm below the surface) and additional charge collection by diffusion may take place from tens of microns beyond the junctions. In those cases, range cannot be ignored. For example, an ion available at Brookhaven National Laboratory (BNL) is I-127 with an energy of 321 MeV. The LET at the surface of the device is 60 MeV·cm^2/mg but the range is only 31 μm. At an incidence angle of 60 degrees the ion penetrates to a depth of only 15.5 μm, which is not sufficient to account for the large amount of charge collected by diffusion. This will lead to errors in the calculated ASET cross-section.
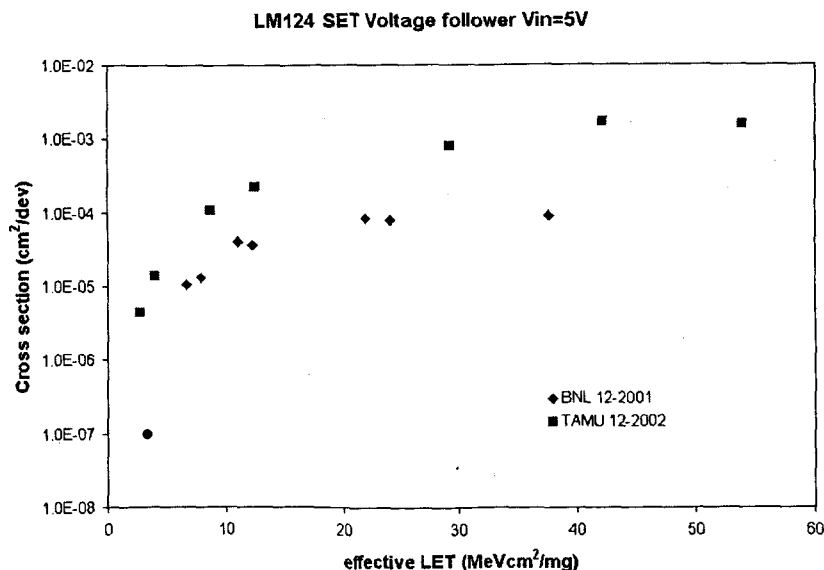

Fig. 24. Cross-section as a function of ion LET for the LM124 op-amp. The measured cross-section is larger for ions at TAMU than at BNL.

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Fig. 24 is a plot of σ(LET) for ASETs in the LM124 that reveals the role played by particle range. The ASET cross-sections measured at BNL are much smaller than those measured at Texas A&M University Cyclotron Institute (TAMU) due to the lower energies and smaller ranges of the ions at BNL.

To calculate the single event rate in space requires the following three inputs:

- The ionizing particle radiation environment characterized by the integral LET spectrum N(LET), where N(x) is the number of particles with LETs greater than x,
- σ(LET) as measured with a broad beam of heavy ions, the functional dependence of which is obtained by fitting the data points with a Weibull function that has four fitting parameters, for which at least four data points are required,
- An assumption of the shape and dimensions of the device sensitive volume, which is usually assumed to be a parallelepiped.

In addition to heavy ions, testing is often performed with energetic protons, particularly when the IC has a LET threshold for heavy ions less than 15 MeV·cm^2/mg. The amount of charge produced by protons via direct ionization is much too small to be able to cause ASETs in most analog devices. However, about 1 proton in 10^5 undergoes either an elastic or an inelastic collision with a silicon nucleus. Some of the particles emanating from the collision move a short distance through the lattice and ionize other silicon atoms. If, through this indirect process, sufficient charge is generated, an ASET is produced. To obtain the ASET cross-section for protons, the number of errors per unit fluence, σ, is measured as a function of proton energy (E_p). Proton-induced error rates are calculated by fitting $\sigma(E_p)$ with the Bendel 1-parameter or 2-parameter equation, or with a Weibull function [BE83].

The unique nature of ASETs is evident when comparing the experimental approach used for measuring their cross-section with that used for measuring the SEU cross-section of a memory. To test a memory for SEUs, a pattern of "1s" and "0s" is written to the memory. The memory is then exposed to a predetermined fluence of heavy ions or protons. After the exposure, the memory is read, the number of errors recorded, and the cross-section calculated. Since ASETs appear as temporary disturbances at the output of a bipolar IC, the device itself does not record the number of disturbances. A counter must be connected to the device output to count and record the total number of ASETs. A counter with a fixed trigger level is of limited value because experiments have shown that σ(LET) depends on trigger level and it is unlikely that the fixed trigger level will match that for a particular application. A better approach would use a digital pulse-height analyzer with a variable trigger level so that the trigger level can be adjusted to equal that of the application, provided the level is known.

Merely counting the number of ASETs that exceed a counter's specific trigger level is not sufficient for calculating the ASET cross-section because the bandwidth of the application is not considered. For example, none of the ASETs may cause a problem if the bandwidth of the application is sufficiently small. The best approach is to use a fast digital storage oscilloscope to capture all transients, and then decide later whether any of the ASETs will propagate through an application with a particular bandwidth. To calculate the cross-section, it is necessary to count only those ASETs that exceed minimum values of amplitude and width determined by the application's bandwidth.

Another factor to be considered is the configuration of the intended application. Configuration for an operational amplifier refers to power-supply voltages, input voltages and output impedance, as well as to whether the device acts as a voltage follower or an amplifier with gain. Since ASET sensitivity depends on all these factors, the device must be tested under configuration conditions identical to those of the application, so that the test results are only applicable to the specific configuration tested.

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The use of an oscilloscope to capture ASETs requires consideration of two factors – the trigger level and the capacitance of the probe. An early experiment investigated the effects on cross-section of trigger level setting [KO93]. The ASET cross-section of the OP-42 was obtained by connecting the output to a pulse height discriminator and counter. The cross-section was calculated for each pulse height setting by counting the number of ASETs per unit fluence. The experiments were repeated for different pulse height settings for the discriminator, a procedure that made it possible to replicate the different "decision" levels for logic circuits connected to the output of the OP-42. **Fig. 25** shows that an increase in the voltage trigger level on the pulse height discriminator caused an increase in the LET threshold [KO93]. Using a special circuit to count the number of ASETs is generally not necessary because the storage oscilloscope itself keeps track of the number of captured ASETs.
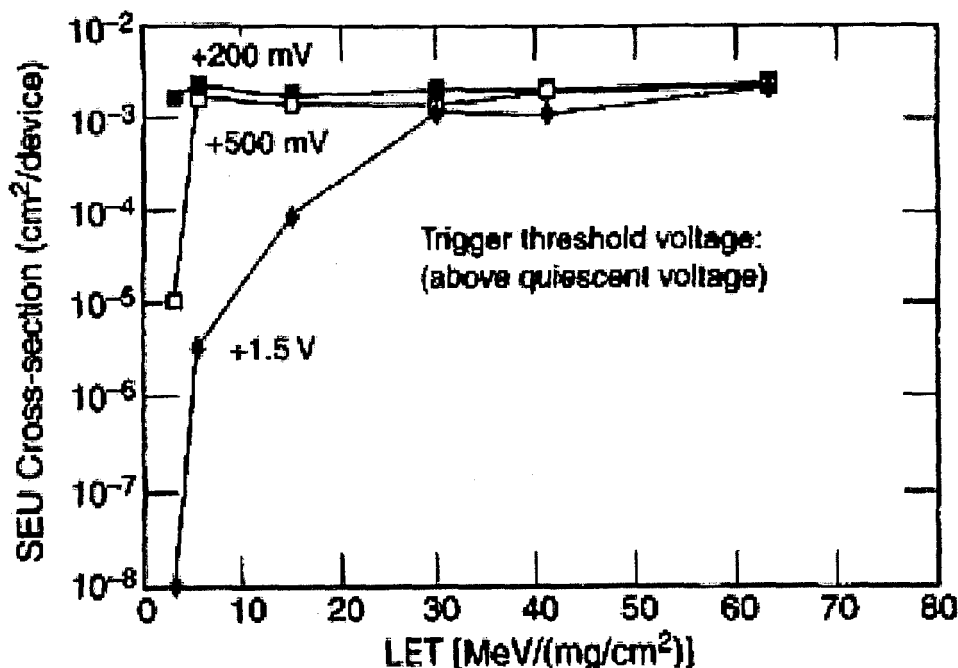

Fig. 25. ASET cross-section as a function of ion LET for the OP-42 [KO03]. The data are for three different settings of the oscilloscope trigger level. The figure clearly shows that as the trigger level is increased, the cross-section decreases because few ASETs are captured.

To obtain good statistics on ASETs during broad-beam testing, a large number of such ASETs should be counted and captured. Data error bars are proportional to $N^{\frac{1}{2}}$. Therefore, for 5% statistics, exposure should continue until 400 ASETs are captured. As will be discussed in Section 7, plots of ΔV vs Δt are generated using the ion data. They should contain points representative of all the possible transients, particularly those at the highest LETs that have maximum amplitudes and widths, because those are the ones most likely to cause an upset in a follow-on circuit. This requires capturing and analyzing a few hundred ASETs.

The large variety of pulse shapes for ASETs generated in the LM124 operational amplifier was shown earlier in Fig. 1. In order to capture both positive and negative ASETs with the digital storage oscilloscope in a single experiment, two probes should be attached to the output of the device. Each probe is connected to a different channel on the oscilloscope. One channel is set to trigger on positive pulses and the other on negative pulses. Care must be taken when connecting the output of the device to the oscilloscope's input. Long cables will have sufficient capacitance to distort the ASET shape, particularly very fast ASETs. To avoid this problem, active probes with very low capacitances (<10 pF) may be used. Testing at some accelerators is only possible

with the device located inside a vacuum chamber. The typical BNC feedthroughs should be avoided because of their limited bandwidth. Instead, the active probes should be placed inside the vacuum chamber so that they can be connected directly to the output pins. Special feedthroughs are necessary for the active probes. Most of these problems may be avoided by testing in air, which is possible at accelerators with high-energy ions.

Fig. 26 shows the setup used for performing heavy-ion testing of amplifiers and comparators at accelerators where the experimenters must conduct the test remotely. One option is to place the oscilloscope and power supply close to the device under test and control everything remotely with a computer. Another option is to locate all the equipment outside the radiation chamber and use long cables to connect the DUT to the oscilloscope. Because the DUT generally does not have sufficient drive for the load imposed by the 50 ohm terminated BNC cable, the signal from the DUT should be connected to a high-speed buffer located adjacent to the output of the device. The high-speed buffer has sufficient drive to transmit an undistorted ASET to the oscilloscope.
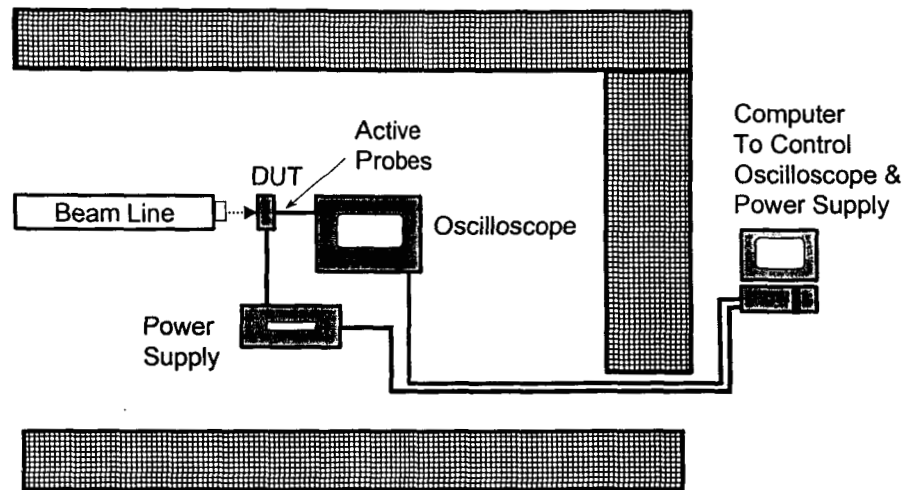

Fig. 26. Typical experimental setup used when doing heavy-ion testing at Texas A&M Cyclotron facility. The DUT is positioned in air in front of the accelerator port. An active probe is attached to the DUT's output for capturing the ASETs, which are then transferred to a computer operated outside the radiation chamber. The compute controls the operation of the oscilloscope and the power supply.

The approach used for testing other analog devices, such as pulse-width modulators is similar, except that ASETs in PWMs appear as changes in the pulse length. In order to capture those types of ASETs, the oscilloscope must be set to trigger on changes in pulse length.

Flux, which is defined as the number of particles crossing unit area per unit time, is another parameter that must be considered for ASET testing. The choice of flux does not affect the measurements of SEUs in a static memory. High fluxes are desirable because they reduce the amount of time needed for testing, but they present a problem if ASETs are generated so rapidly that they overlap and it becomes difficult to distinguish individual pulses. For accurate cross-section determination it is important that every ASET be counted. A key consideration is the down time of the oscilloscope used: the event rate must be such that the probability of two events occurring within the acquisition time of the oscilloscope is small.

An ASET test report should include all the test conditions so that others may determine whether the data are relevant to their application. For example, a test report for an operational amplifier should include information on the supply voltage, input voltage, configuration, gain, output loading, and oscilloscope trigger level, in addition to ion species, LET, flux and fluence.

In some cases, ambient light has been found to have an effect on ASETs. For instance, some of the most sensitive transistors in the LM124 are insensitive to ASETs in the presence of ambient light. Because heavy-ion testing requires that the packaging be removed in order for the ions to reach the device, the die is exposed to any ambient light present. Therefore, not only should the room lights be turned off, care should be taken to make sure there are no other sources of light, such as an ionization gauge with a glowing filament used for measuring pressure in a vacuum chamber or beam line. (see Section 5.5.5.2)

5.2   Accelerator Testing – Broad Beam of Protons

A device having a heavy-ion LET threshold below 15 MeV·cm^2/mg is considered so sensitive to single event effects that they may also be sensitive to protons-induced SEEs. Therefore, linear devices, which have LET thresholds of approximately 1 MeV·cm^2/mg would, according to the above rule, be expected to be proton sensitive. However, as already pointed out, the LET threshold is small because the long charge collection depth partially compensates for the relatively large critical charge. Given the short range of the secondary particles generated in a nuclear interaction, it is certainly not a given that protons could produce transients in linear devices.

The first linear device tested for ASET sensitivity to protons was the LM139 voltage comparator, which had a LET threshold of 2 MeV·cm^2/mg when the differential input voltage was 25 *mV* and the trigger level was 2 *V* [NI96]. To improve the chances of seeing ASETs with protons, the differential input voltage was reduced to 12.5 mV. The corresponding critical charge, which depends on the differential input voltage, was much reduced. **Fig. 27** shows the measured cross-sections as a function of proton energy for a trigger level of 2 *V*. Although there is some scatter in the data, the trend is unmistakable – as the proton energy increases, so does the cross-section. The data also reveal a greater ASET cross-section for negative values of differential input voltage than for positive values. Low-energy (30 *MeV*) protons produced smaller transients than high-energy (200 *MeV*) protons, and when the differential input voltage was increased to 25 *mV*, only 200 *MeV* protons produced ASETs.

To calculate the ASET rate in space requires data from both heavy ion and proton experiments. In fact, in some cases the rate from protons will most likely dominate that from heavy-ions, so it is essential to do proton testing when, for example, the differential input voltage of a comparator is small.

Broad-beam accelerator testing is essential for characterizing linear devices for their ASET sensitivity and for calculating ASET rates in space. As a diagnostic tool, however, the accelerator has two major deficiencies – it provides neither spatial nor temporal information. The other two experimental techniques, focused ion microbeam and focused pulsed laser light, are capable of providing detailed spatial information. In an ideal world, the radiation effects engineer would have access to all three!
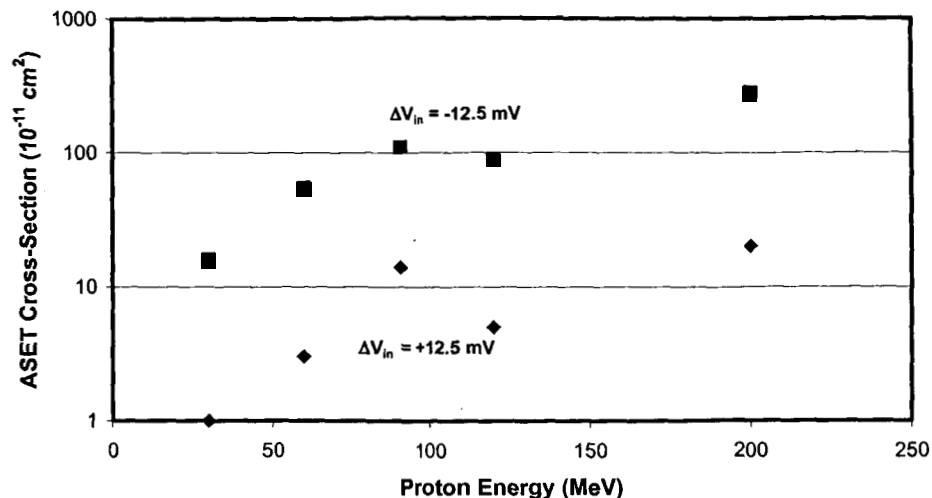
Fig. 27. ASET cross-section for the LM139 as a function of proton energy for two different values of differential input voltage [NI96].

5.3 Accelerator Testing – Focused Ion Beam

The major drawback of broad-beam ion testing is the inability to obtain spatial information concerning the physical origins of the induced transients. That type of information can be enormously helpful in understanding anomalous behavior and in validating models used for computer simulation studies. A focused ion beam is an experimental method that provides information on the spatial origins of ASETs [SE96].
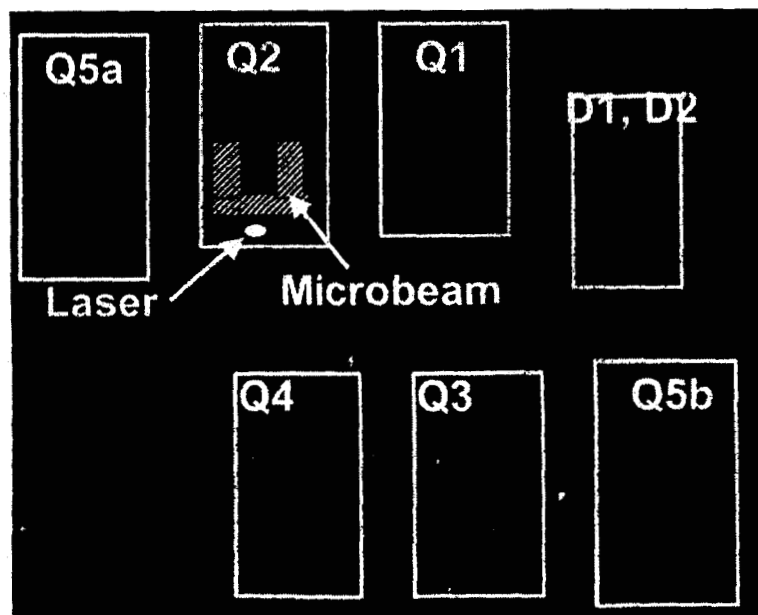

Fig. 28. Photomicrograph of the input section of the LM111. The region scanned with the ion microprobe is marked Q2 [PE02].
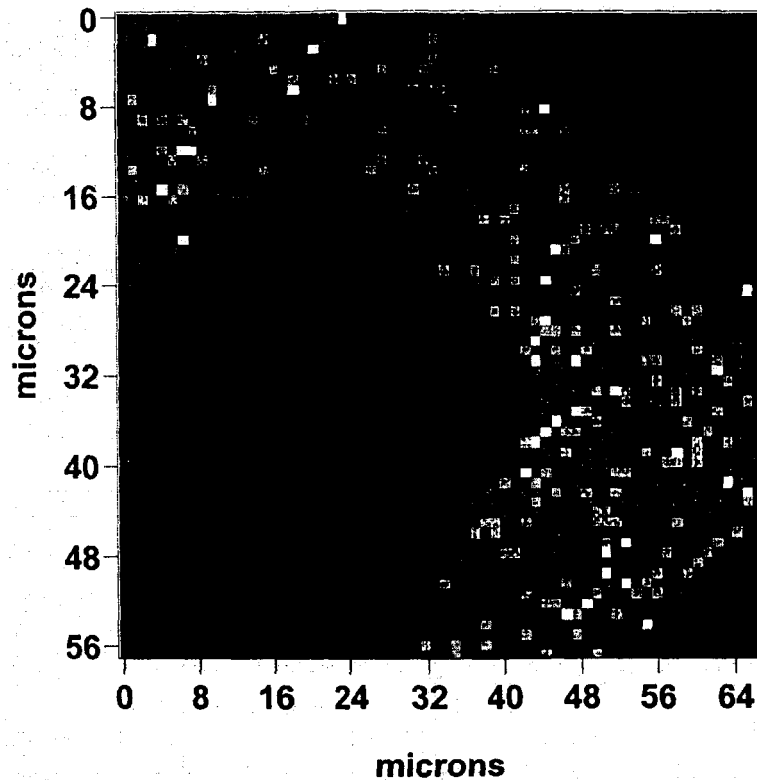
Fig. 29. Location of ASETs generated in transistor Q2 of the LM111 using the ion microprobe. The sensitive region surrounds the emitter contact on three sides. The figure is rotated about 135 degrees with respect to the image in Fig. 28.

There are numerous microbeam facilities throughout the world, including Sandia National Laboratories in the USA and Gesellschaft für Schwerionenforschung in Germany. Unfortunately, this experimental technique has not found wide use for investigating ASETs due to a number of reasons: limited accessibility to almost all facilities, the use of low-energy ions at some facilities that have small ranges in silicon, and the difficulty of changing ion species.

Both the utility and the limitation of the technique are revealed in the results obtained for the LM111 voltage comparator. [PE02] **Fig. 28** is a photomicrograph of part of the LM111 showing the transistors in the input circuit. **Fig. 29** shows the results of an ion microbeam scan of an input transistor Q2 using 40-MeV Cl ions with a range in silicon (after accounting for overlayers) of 6 – 7 μm and an initial LET of about 18 MeV·cm^2/mg. Each point corresponds to an ion strike that resulted in an ASET with amplitude greater than 0.1 V. Comparison of the two figures clearly shows that the region sensitive to ASETs is the emitter-base depletion region that is partially covered by metal. The highly doped contact region in the center, and the region adjacent to the base contact appear not to be sensitive to ASETs. This information proved very useful in establishing a model for the ASET sensitivity of the input transistor, a model that included the spreading resistance of the base. The fact that the focused ion beam failed to identify other ASET-sensitive areas in the LM111 points to the major deficiency of the focused ion beam at SNL – the low energies and, therefore, limited ranges of the ions.

Another limitation of the ion microprobe is the radiation damage induced in the IC by the large number of heavy ion strikes required to obtain the data in Fig. 28. Radiation damage takes the form of both TID and DD. At very high levels it may affect the shape of the transient, as will

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be described in a later section. In summary, very few experiments on ASETs have been performed with focused ion beams.

5.4   Pulsed Laser Testing

Over the years, the pulsed picosecond laser has been successfully applied to the evaluation of single event effects in a number of different circuits and devices, including SRAMs, DRAMs, logic circuits, analog-to-digital converters, etc. [BU87], [BU90], [MC94], [ME94], [MO95], [BU96], [BU97], [MC00], [BU04a]. It is in the area of ASETs, however, that the pulsed laser truly has come into its own. It has been unequivocally demonstrated for the devices investigated to date that the ASET shapes generated by pulsed laser light are *identical* to those generated by heavy ions. The similarity of the pulse shapes suggests that the differences in the mechanisms responsible for free-carrier generation – Coulomb excitation for charged particles and light absorption for photons – are not important for the devices tested thus far.

One key factor that distinguishes the pulsed laser from a broad ion beam, apart from the physics of carrier generation, is the control over the location of the charge injection. By focusing the laser pulse to a spot with a diameter of approximately one micron and scanning the spot across the surface of the IC, information regarding the locations of ASETs as well as their pulse amplitudes and shapes can be obtained.

One attractive feature of the pulsed laser is that the spatial information is obtained without any concomitant radiation damage (total ionizing dose or displacement damage) to the device being tested, provided the light intensity is not excessive. Additional practical features of the technique are that testing may be performed in air, and it is a simple matter to adjust the "equivalent LET" merely by increasing or decreasing the laser pulse energy.

The laser approach has been used to extract a great deal of useful information regarding ASETs. For example, the information provided by the pulsed laser has proved vital for fine-tuning the models used to calculate ASET pulse shapes with computer programs such as SPICE [PE02]. Parasitic capacitances and resistances not available from manufacturers' data sheets have had to be included in the circuit models to match calculated ASET pulse shapes with those obtained experimentally [BO02]. The pulsed laser also has provided essential information regarding the location of anomalous ASETs, such as unusually long pulses observed in some circuits [BO4a]. It has been used to study the effect of changing supply and input voltages as well as device configuration on the shapes and amplitudes of ASETs [BU01]. Finally, the pulsed laser has been used to determine whether a linear device is suitable for a specific application by measuring maximum amplitudes and widths of ASETs generated by scanning a laser beam with maximum energy across the linear IC and determining whether any of the output pulses exceed the minimum values required for being latched into a follow-on circuit [BU04].

The physical mechanism responsible for ASET generation in ICs with pulsed laser light is the excitation of electrons from the valence to the conduction band of the semiconductor by the absorption of photons. The free carrier generation rate (dN/dt) is given by:

$$\frac{dN(r,z)}{dt} = \frac{\alpha I(r,z)}{\hbar\omega} + \frac{\beta_2 I^2(r,z)}{2\hbar\omega}, \tag{4}$$

where $I(r,z)$ is the pulse irradiance in W/cm^2 at a distance z from the surface and a radial distance r from the center of the track. N is the density of free carriers generated by the light, α is the linear absorption coefficient, β_2 is the two-photon absorption coefficient, which is the real part of χ^2, the second-order nonlinear-optical susceptibility, and $\hbar\omega$ is the photon energy. Eqn. (4) includes both linear and non-linear processes. The linear term governs one-photon absorption, and the quadratic term governs two-photon absorption.

To date, two different methods of charge injection using laser light have been developed for studying ASETs. The first, well-established approach involves single-photon absorption, and the second, recently developed, relies on the nonlinear-optical process in which two sub-bandgap photons are absorbed simultaneously to generate a single electron-hole pair. The two processes may be prevented from interfering with each other by selecting the appropriate values of laser wavelength, pulse energy, and pulse width [ME94]. The photon energy, which is inversely proportional to wavelength, should be chosen to be greater than the bandgap of Si (1.1 eV) for linear absorption, and less than the bandgap for non-linear (two-photon) absorption to be the dominant process. To obtain sufficient intensity for efficient carrier generation in the latter, an optical pulse of around 100 fs (or less) duration is focused to a spot of about one micrometer in diameter. This pulse length is about a factor of 10 to 100 shorter than that typically used for single-photon absorption experiments, facilitating the nonlinear-optical process in this case.

Currently there are five pulsed-laser facilities used for studying SEEs. Two are in the United States – one at The Naval Research Laboratory [ME94], [MC00] and the other at The Aerospace Corporation [MO95],[LA02]. There is one at Matra BAE Dynamics in Great Britain [CH02], and there are two in France – at IXL in Bordeaux [PO99], [LE01] and at EADS Corporate Research Centers in SURESNES [DA02], [MI04]. The results presented in this monograph make it clear that access to a pulsed laser facility provides a convenient and non-destructive method for characterizing SETs in analog circuits, identifying sources of anomalous behavior, and performing hardness assurance testing. The role of the pulsed laser is to complement, but not replace heavy-ion testing.
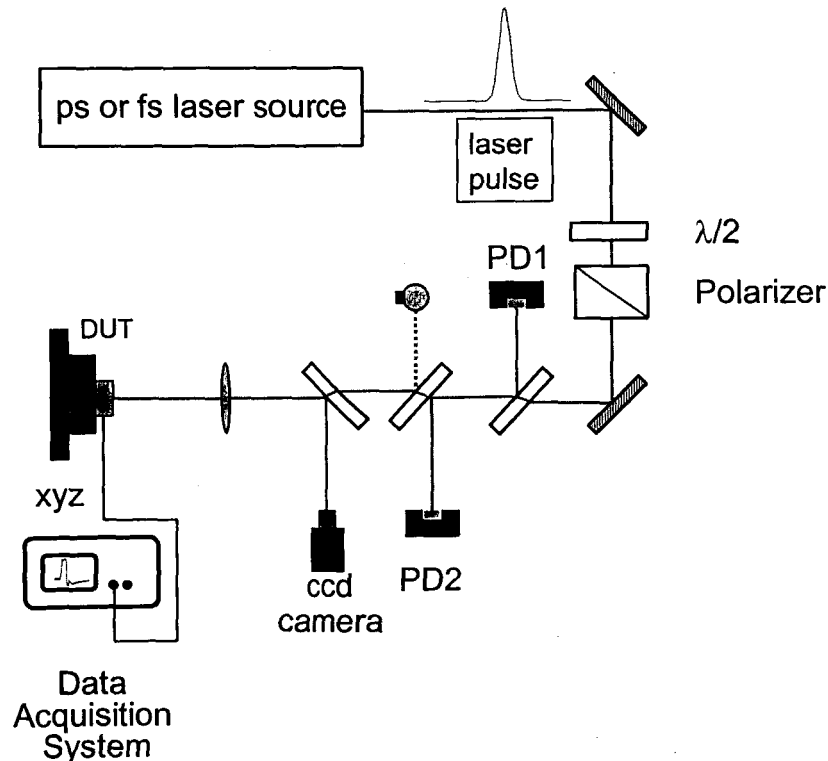

Fig. 30. Schematic diagram of typical setup for performing pulsed laser SEE: PD1 and PD2 are calibrated photodiodes for measuring the reflected and incident laser pulse energy; DUT is the device under test; xyz is a motorized xyz stage; and λ/2 is a half-waveplate.

Fig. 30 shows a schematic diagram of a typical pulsed laser SEE setup. This figure illustrates a generic setup that is applicable to either single-photon or two-photon SEE measurements. In general, laser SEE experiments require a pulsed laser source in which the pulse repetition rate can be controlled over several decades, from single shot to over a MHz, depending on the characteristics of the experiment involved.

For visible-wavelength, above-bandgap laser experiments several different types of laser systems have been utilized. The initial systems used were based on flashlamp-pumped, modelocked Nd:YAG lasers that produced nominally 30 ps pulses at a pulse repetition rate of 10 Hz′ [BuU87], [BU90]. Typically two wavelengths were accessible: the fundamental at 1064 nm, and the second harmonic at 532 nm. While generally quite robust, these pulsed lasers suffer from large pulse-to-pulse amplitude fluctuations and the limited choice of wavelengths available. Recently, a newer generation of pulsed Nd:YAG lasers has become available, two varieties of which are presently in use for SEE studies [DA02], [JO00], [CH02].

The early pulsed Nd:YAG lasers were quickly replaced for SEE studies by synchronously-pumped, cavity-dumped dye laser systems. These lasers are pumped by cw (continuous-wave) modelocked Nd lasers, and exhibit significant improvements in stability when compared to the pulsed lasers. Such systems, which have been in use at the Naval Research Laboratory [ME96] and the Aerospace Corporation [MO95] for over a decade, are very robust, offer a wide tuning range from the visible into the near-infrared spectral regions, produce optical pulses with a typical duration of 1 ps to 10 ps, and cavity dumping provides switch-selectable control over the pulse repetition rate. The major drawbacks of dye-laser systems are related to the performance of the now-obsolete modelocked Nd:YAG and Nd:YLF pump lasers, and the inconvenience of working with liquid dye solutions. The former objection has been diminished by the recent development of high-stability and highly reliable diode-pumped, modelocked solid-state lasers.

A second laser system that has been applied to single-event effects studies is the modelocked Ti:sapphire laser [ME96], as has been implemented by the group at ILX in Bordeaux [LE01]. The Ti:sapphire laser has the advantage of being all solid state, with excellent stability and reliability characteristics. Its typical tuning range is from 750 nm to 950 nm in the near-infrared region of the spectrum (this varies with the optics used), well suited for investigations involving silicon. The Bordeaux implementation uses an external pulse-picker for repetition rate control, but these lasers can be cavity dumped as well. The pulse width of Ti:sapphire lasers is typically less than 100 fs, for which competing nonlinear-optical processes become a concern [ME96], but nominally 1 ps versions are available.

A third type of laser system that has been applied to single-event effects studies is the modelocked Ti:sapphire laser [ME96], as has been implemented by the group at ILX in Bordeaux [LE01]. The Ti:sapphire laser has the advantage of being all solid state, with excellent stability and reliability characteristics. Its typical tuning range is from 770 nm to 900 nm in the near-infrared region of the spectrum (this varies with the optic set used), well suited for investigations involving silicon. The Bordeaux implementation uses an external pulse-picker for repetition rate control, but these lasers can be cavity dumped as well. The pulse width of Ti:sapphire lasers is typically less than 100 fs, for which competing nonlinear-optical processes become a concern [ME96], but nominally 1 ps versions are available.

For the sub-bandgap two-photon SEE measurements the requirements of the laser source are significantly different from those of the visible/near-infrared experiments. First, to optimize the nonlinear term in eq. (3), high irradiance, ultrashort optical pulses with durations on-the-order-of 100 fs (or less) are required. The Naval Research Laboratory TPA SEE setup is based upon a tunable optical parametric amplifier (OPA) that is pumped by an amplified femtosecond Ti:sapphire laser system. The OPA utilizes a beta barium borate nonlinear crystal for parametric

light generation in the 1.1 μm to 3.0 μm wavelength range. For the TPA SEE experiments on silicon-based structures the OPA typically is tuned to produce a signal beam at 1.2 μm to 1.3 μm with a nominal pulsewidth of less than 150 femtoseconds.

The other optical elements evident in Fig. 30 typically are common to all laser SEE setups, although the details vary with the optical wavelength used. In particular, a waveplate/polarizer combination is used for continuous adjustment of the laser pulse energy. This can be supplemented by the use of calibrated neutral density filters (not shown), as required. Calibrated photodiodes are used to monitor the laser pulse energy incident on (PD2), and reflected from (PD1) the surface of the device under test (DUT). Typically, large area silicon photodiodes are used for the visible experiments; InGaAs photodiodes for the sub-bandgap experiments. Note that all neutral density filters and photodiodes must be calibrated for each wavelength used. The optical pulse is focused onto the DUT using a long-working-distance 100X microscope objective, giving rise to a spot size of approximately 1 μm for the visible experiments, and somewhat larger for the infrared experiments. The DUT is mounted on a computer controlled x-y-z stage, typically with 0.1 μm resolution. An optical imaging system is used to observe the location of the laser spot on the surface of the chip. For the visible experiments this consists of a source of white light directed through the microscope objective to illuminate the surface of the chip, with a silicon CCD camera and monitor to view both the device surface and the position of the focused laser spot. A primary motivation for development of the TPA technique is the ability to interrogate the SEE response of the device through the wafer, eliminating interference from metallization. Imaging through the silicon wafer is facilitated by the use of an InGaAs focal-plane array (FPA), which has a maximum sensitivity in the near infrared spectral region.

The application of each method is described in detail below.

5.4.1 Linear Absorption.

For photon energies larger than the bandgap of the semiconductor, α in (3) is greater than zero. At low light intensities, the first term on the right hand side of equation (3) dominates, and the light intensity $I(r,z)$ decays exponentially with distance z from the surface according to:

$$I(r,z) = I_o e^{-\alpha z} \qquad (4)$$

The penetration depth (δ) is defined as the depth at which the intensity drops to 1/e (37%) of its intensity at the surface and is given by the inverse of the absorption coefficient, which depends on the wavelength of the light. For example, the pulsed laser at the Naval Research Laboratory typically operates at a wavelength between 590 nm and 610 nm, and δ is approximately 1.8 μm in silicon. The charge density along the track varies in the same way as does the intensity given in eqn. (4). **Fig. 31a** shows the charge track produced in silicon by focusing a 590 nm optical pulse width a microscope objective lens. The radial charge density ideally has a Gaussian shape whose profile is determined by the characteristics of the incident laser beam and the focusing power of the microscope objective lens. **Fig. 31b** illustrates the corresponding carrier density profile produced by 800 nm an optical pulse focused under analogous conditions.
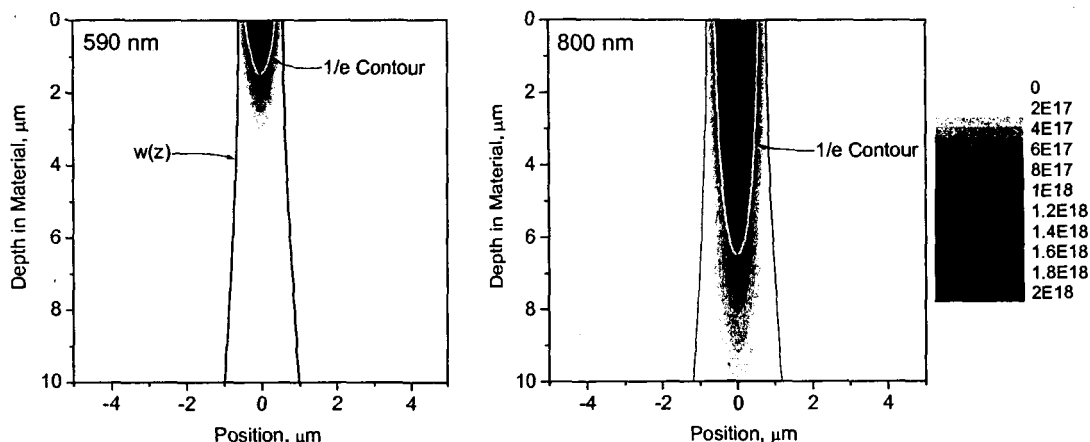
Fig. 31. Electron-hole density plot for 590 nm and 800 nm single-photon excitation processes in silicon as a function of depth in the material for a 1 ps pulse focused to fwhm diameters of 1.2 μm and 1.6 μm, respectively. The carrier density is plotted in electron-hole pairs/cm^3 [MC02].

There are some issues regarding the pulsed laser technique that bear consideration. The first, and most obvious, is the presence of metallization that prevents the light from reaching some of the junctions. This can be a problem for some devices, such as dense memories and microprocessors with multiple layers of metal (although the significance varies from part to part). Fortunately, however, transistors in many analog devices have large surface areas devoid of metal, making it possible to probe almost all potentially sensitive areas with laser light. In those cases where metal does completely cover a sensitive area, two options remain. One is to focus the light onto a spot adjacent to the metal and increase the light intensity so that charge can diffuse under the metal to the sensitive region. One example in which this was necessary was the LM111 discussed above (cf., Figs. 27 and 28) [PE02]. The impact of metal coverage of the sensitive nodes on the results was minimal in that case, and quantitative agreement with heavy ion measurements was achieved (vide infra). Another approach, which is described in detail in the next section, is the use of sub-bandgap optical pulses that propagate through the wafer from the back side of the chip. The sub-bandgap laser pulse propagates unimpeded through the substrate until it reaches the focal point of the microscope objective lens, at which point it has sufficient intensity to generate carriers via the two-photon processes.

The diameter (~1 μm) of the focused laser beam is an issue that must be addressed when testing devices, such as memories, with sensitive areas of transistors much smaller than the area of the focused laser spot. Under those circumstances, it can be a challenging task to measure energy thresholds for ASETS. In contrast, most of the linear devices encountered so far have transistors that are significantly larger than the diameter of the focused laser beam, making it a simple matter to measure absorbed energy in a quantitative fashion. Calculations have clearly demonstrated that differences between charge track structures produced by focused laser light and by heavy ions may be ignored because, in a matter of a few picoseconds after the tracks are generated, the charge distributions become comparable [MC96].
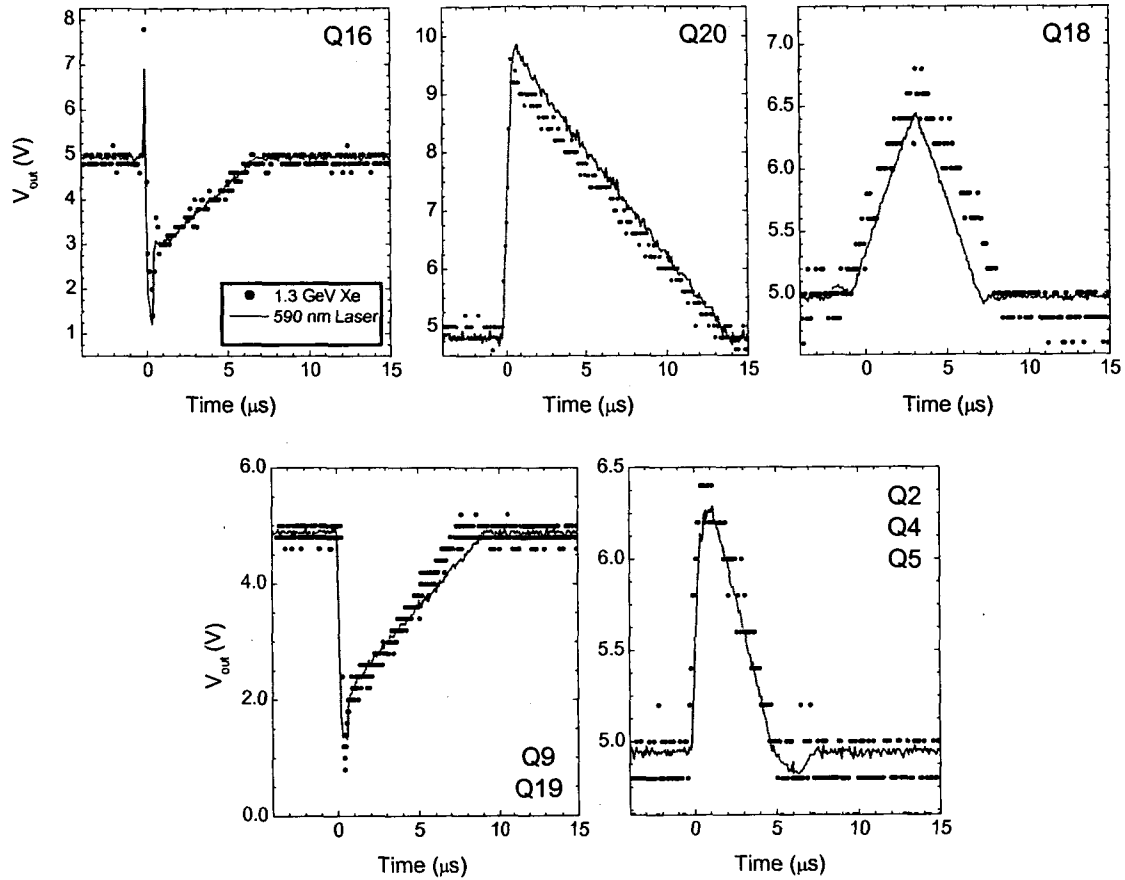
Fig. 32. Comparison of ASETs induced by a broad beam of heavy ions and 590 nm pulsed laser light [BU04a].

Previous experiments have demonstrated that it is possible, in many cases, to relate the pulsed laser light energy needed to produce a SEU with the threshold LET measured with heavy ions [MC00], [MO95]. The method is purely empirical and found valid for a variety of devices, all of which have their junctions near the surface of the semiconductor. In contrast, analog devices frequently make use of different types of bipolar transistors (vertical n-p-n, substrate p-n-p, and lateral p-n-p) with junctions at different depths. The fact that the amount of light reaching two junctions at different depths will be different makes the direct comparison of their ASET sensitivities challenging.

The decisive test showing unequivocally that the pulsed laser faithfully reproduces ASETs was obtained by comparing ASET pulse shapes generated by laser light and heavy ions. **Fig. 32** shows that the pulse shapes of the ASETs generated in the LM124 by these two methods are effectively identical [BU04a], suggesting that the charge deposition processes and details of the spatial profile of the deposited charge do not play a significant role in determining the resultant ASET output pulse shape, provided the charge is deposited in a time shorter than the response time of the circuit. As already noted, this observation is of practical importance for modeling because it suggests that the actual shape of the current generator used to simulate charge injection generally is not important. Instead of using double exponentials or more complex pulse shapes for the current generator, simple trapezoidal current pulses may be used, as has been verified by comparison to experiment. For the example of Fig. 31, after collection of the HI SET measurements, the unique signatures of the different nodes were identified using a 590 nm pulsed

laser. To obtain the correspondence illustrated in Fig. 31, the laser pulse energy was adjusted so that the ASET amplitude matched (approximately) that of the HI transient for each node of interest [BU04a].

Pulsed lasers have been used for some time to identify sensitive transistors in amplifiers and comparators. The identities of the individual transistors sensitive to ASETs are determined by focusing the pulsed laser light to a spot with a diameter on the order of one micron and scanning the beam across the die while monitoring the device's output. Some of the first measurements with the pulsed laser were on the OP-15 [KO96]. Those early measurements confirmed predictions that the transistors most sensitive to ASETs are located in the input section. The initial measurements did not compare the shapes of the ASETs produced by the pulsed laser light with those produced by heavy ions. However, they did compare the saturated cross-section determined with heavy ions with the total area sensitive to ASETs as measured with the pulsed laser. The total sensitive area for the OP-15 was obtained by summing up the sensitive areas for each ASET sensitive transistor. The total sensitive area was 3×10^{-3} cm^2, which is within a factor of 2 of the saturated cross-section measured with heavy ions.

The technique is ideally suited for automated scanning of the surface of an IC to map areas sensitive to ASETs. IXL Microelectronics Laboratory in Bordeaux, France has developed a very sophisticated laser scanning system that is well suited for probing analog ICs [PO00]. The IC of interest is mounted on an x-y stage and a focused beam of light is directed at the IC surface. A computer controls the movement of the x-y stage as well as the oscilloscope that captures the ASET. A complete scan of the IC is performed for a series of laser energies. During the scan, all ASETs are captured and their locations noted. From such measurements, contour plots of ASET amplitude or width may be generated. The contour plots are then superimposed on a photomicrograph of the chip so that the exact locations of all the ASETs may be identified. **Fig. 33** shows an example of the type of contour plot obtained. The software is sufficiently powerful that it can produce contour plots of any ASET characteristic of interest, such as pulse width, pulse amplitude, positive pulses, negative pulses, pulses larger than an arbitrary threshold, location of bipolar pulses etc. Scans of localized areas are achieved by reducing the step size to 0.1 μm, whereas scans of the whole chip are more efficiently done with larger step sizes. This scanning method is ideally suited for accurately pinpointing the most sensitive regions of a device.

5.4.2 Non-linear Absorption.

The second method for injecting charge to generate ASETs involves the nonlinear-optical process of two-photon absorption (TPA). The wavelength of the optical pulses is selected so that the individual photons have energies smaller than the bandgap of the semiconductor. In this case, α in (3) is effectively zero, and the light passes through the semiconductor un-attenuated by linear absorption processes. However, as the pulse irradiance is increased the second term in (3) becomes non-negligible and electrons can be excited to the conduction band via the simultaneous absorption of two photons. In practice the laser pulse irradiance is increased by using a very short optical pulse (~100 fs) with a high pulse energy and focusing it to a small (~1 μm) spot. The free-carrier generation rate for TPA is given by the second term in equation (3), and is proportional to the square of the laser pulse irradiance. As already noted, TPA requires a laser system that has different capabilities fromthan the one used for single-photon absorption; the photons must have energies less than 1.1 eV, the bandgap of silicon, and the pulses must be on the order of 100 fs or less.
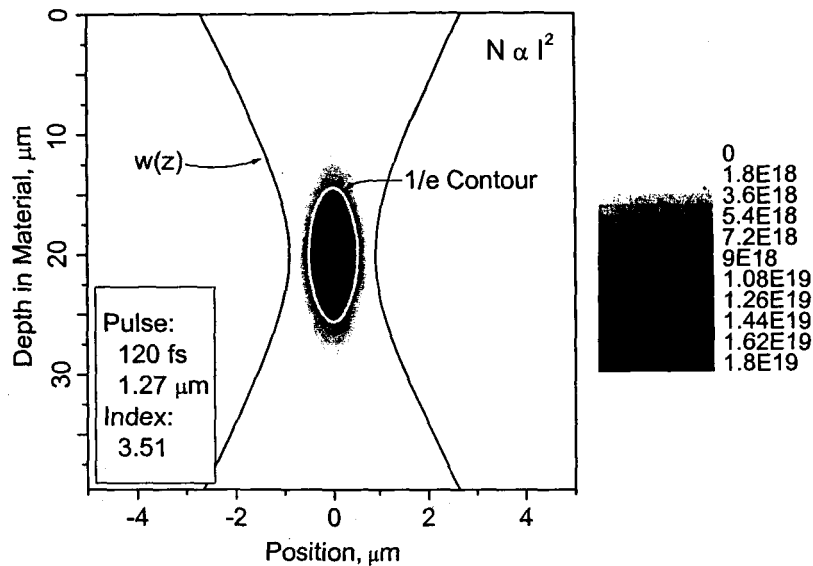
Fig. 33. Electron-hole density plot for the 2-photon excitation process in silicon 1.26 μm as a function of depth (z) for a 1 nJ, 120 fs pulse focused to a fwhm diameter of 1.6 μm. The carrier density is plotted in electron-hole pairs/cm^3 [MC02].

Fig. 33 shows a first-order calculation illustrating carrier deposition profile for propagation of a sub-bandgap femtosecond optical pulse through intrinsic silicon under conditions optimized for efficient TPA [MC02]. As is evident, absorption only occurs near the focal region where the pulse irradiance is a maximum. The carrier profile produced by TPA has the shape of a "cigar" whose dimensions determined by the confocal parameter of the incident laser beam, the focusing power of the lens, and the index of refraction of the material. When higher-order effects are included in the calculation, the longitudinal symmetry evident in **Fig. 33** is lost for high pulse irradiances. Using this approach, because of the absence of linear absorption processes (*cf.*, first term on rhs of eq. (3)), the focal point, and hence, the location of the carrier deposition, can be positioned at any depth below the surface of the IC by translating the device relative to the lens. Two advantages accrue from this approach. One is the ability to inject carriers in a localized volume at any depth below the surface to separate the contributions to ASETs from different junctions, so they may be studied independently. The second is potentially more important in that it provides another option for ASET testing of devices that may be covered with metal or are packaged "face down". Access to the sensitive regions may be gained by directing the incident light through the wafer from the back side of the IC. Reservations about the utility of the pulsed laser technique arising from the presence of metal layers on the surface of the IC that would prevent the laser light from reaching sensitive junctions are allayed backside probing.

The one situation in which the two-photon technique requires additional processing is for the case of highly doped ($>10^{18}$ cm^{-3}) silicon substrates. When the free-carrier density in the semiconductor is sufficiently high, the incident optical pulse is attenuated by free-carrier absorption [SC81]. This impacts both the optical pulse propagation through the wafer, and the imaging aspects of the experiment. In this case it is necessary to thin the device by removing most of the substrate material, an approach that has been demonstrated recently [MC05].
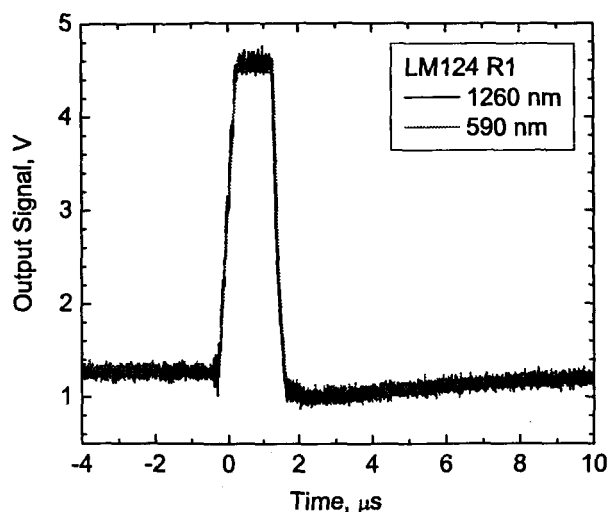
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Fig. 34. Comparison of ASETs generated by one-photon and two-photon processes in the LM124. In both cases the light was focused on the same spot on resistor R1.
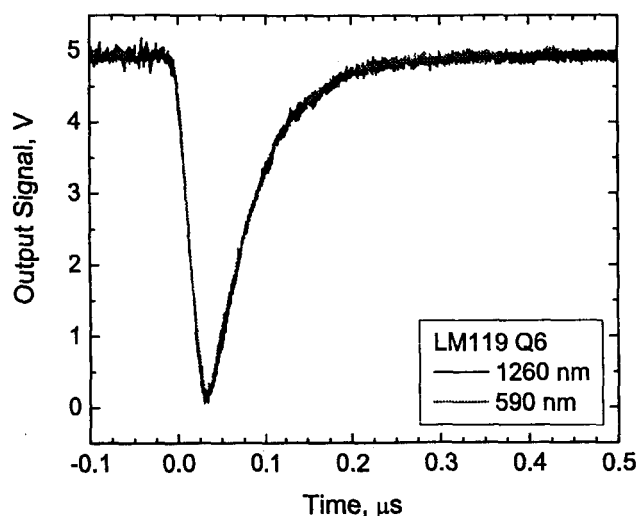

Fig. 35. Comparison of ASETs generated by one-photon and two-photon processes in the LM119. In both cases the light was focused on the same spot on transistor Q6.

The two-photon method for producing ASETs was first validated by comparing the ASETs generated in the LM124 for one- and two-photon absorption processes. **Figs. 34** and **35** illustrate that for top-side illumination there is no difference in the ASET pulse shapes generated by the two approaches [MC02]. Validation of the through-wafer approach was performed by comparing ASET pulse shapes generated by front-side and back-side illumination at identical locations in a number of transistors in the LM124 operational amplifier. **Fig. 36** shows that there is no difference in the ASET shapes, or in the amount of energy needed to produce equivalent ASET pulses for light incident from the top side of the chip, or for optical pulses that propagate through the unthinned wafer from the back of the IC [MC04]. The minor differences between the two data sets are not significant, and are associated with uncertainties in the laser spot location.

The TPA method represents a novel approach to SEE evaluation with unique capabilities not exhibited by other techniques. The back-side geometry eliminates interference from the metallization layers, and circumvents many of the issues associated with testing flip-chip-

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mounted parts. Recent generation technologies are becoming increasingly complex, with multiple metallization layers becoming a major impediment to conventional top-side laser SEE testing. Additionally, the advent of flip-chip mounted devices renders both top-side laser testing and conventional heavy-ion testing impractical (or impossible). The results summarized here reveal that the back-side TPA technique represents a potentially valuable alternative to the conventional laser and ion techniques that can be made even more powerful by additional effort in the development of dedicated lasers and optical testing schemes.
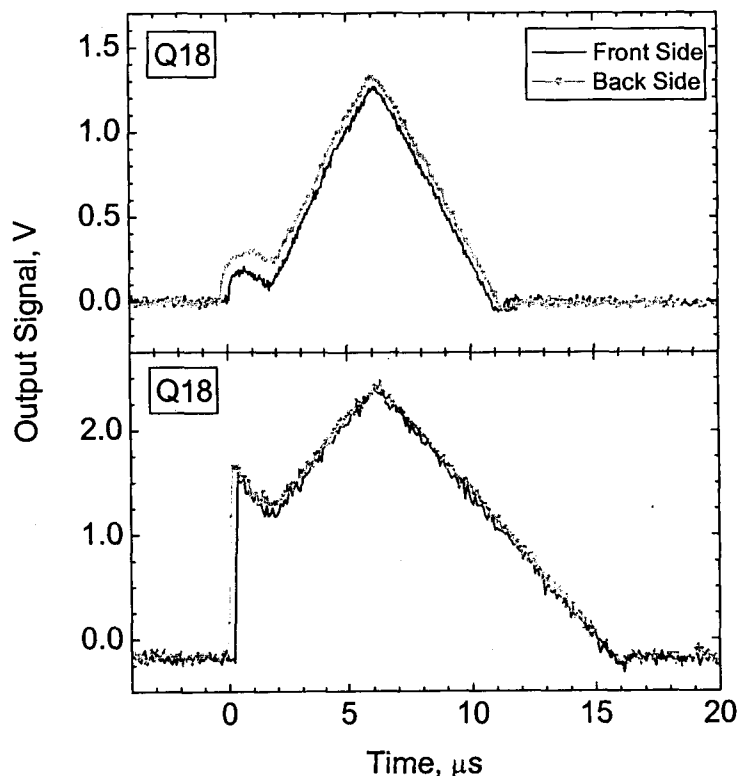

Fig. 36. Transients obtained as a result of two-photon absorption at two different locations on transistor Q18 of the LM124 op-amp. The dark lines are for light incident from the front side and the grey lines are for light incident from the backside. No adjustment of the light intensity was made. The close match shows that there was negligible absorption of the light as it passed through the substrate [MC03].

5.5 Space Experiments

Predictions of SEE rates in space are based on the results of ground testing. There is considerable uncertainty in the predicted SEE rate as a result of random errors in the data and, more importantly, systematic errors in the models of the radiation environment, the interaction between particles and the device, as well as device-to-device variability. In fact, the calculated SEE rate has been found, on occasion, to differ from the measured rate by as much as an order of magnitude. Obtaining more accurate predictions for SEE rates in general, and ASET rates in particular, requires that the models describing the mechanisms be improved.

The Microelectronics and Photonics Testbed (MPTB) is a space experiment launched in November 1997 to measure the effects of radiation on various electronic and photonic devices. One of the experiments on MPTB had as its objective the measurement of ASETs in an op-amp (LM124) and a voltage comparator (LM139) [CR01]. The inclusion of particle detectors on the spacecraft to monitor the environment made it possible to correlate measured ASETs in the two linear devices with the actual particle radiation environment.

Both devices were operated with ± 5 V power supplies. The differential input voltage of the LM139 comparator was set at +0.1 V, so the output was "high" and all ASETs were negative-going transients. The LM124 had no feedback and the output was set at either the positive rail or in the middle. The occurrence of an ASET as well as its amplitude were measured throughout MPTB's orbit that extended from below the radiation belts out to geosynchronous orbit.

Ground testing was performed on the devices in the identical configuration used in space. Based on the data obtained from ground testing, ASETs rates were calculated for the devices on board MPTB [CR01]. Unfortunately, no quantitative comparisons were made between the predicted and measured ASET rates.

The data show that the LM124 produced many ASETs and that the rates correlated well with the changing radiation environment – the ASET rates were highest when MPTB was in the Earth's radiation belts and when there was a solar event, but the overall rate decreased with time due to the approaching solar minimum. Very few ASETs were produced by the LM139 until the differential input voltage was reduced. The majority of ASETs detected in both devices had amplitudes no greater than 1 V, information that is important for the design engineer.

6.0 Case Studies using a Combination of Pulsed Laser, Heavy Ions and Circuit Simulation

Section 5.4 presented the pulsed laser as a convenient laboratory tool for studying ASETs because analog ICs may be evaluated for ASET sensitivity with a minimum of delay and a maximum of convenience. The ability to focus the light on a specific transistor junction is essential for identifying the sources of anomalous ASET responses. Since linear devices can be used in a large number of different operating configurations (gain, output load) and voltages (supply and input), it is impractical to perform accelerator testing for all possible conditions. By supplementing conventional accelerator testing with pulsed laser testing and circuit simulation, the full spectrum of ASET responses and sensitivities can be investigated and characterized. What follows is a brief overview of some examples for which the pulsed laser and/or circuit simulations have proven invaluable in unraveling the complex SET response of some linear ICs.

6.1 Dependence of ASETs on Circuit Parasitic Elements

This section will describe briefly how focused laser light was used to identify specific areas in linear ICs that were not originally known to be ASET sensitive. In fact, in the cases outlined below, sensitive areas were first identified by scanning the focused laser light across the entire surface of the IC and noting where ASETs were generated. Knowing which transistors are sensitive is enormously important for interpreting the results of broad-beam heavy-ion tests and for improving the accuracy and completeness of the device models used for simulation.

The first example is that of the LM119 high-speed voltage comparator [ST02]. A laser scanned across the surface of the die revealed an unexpected result: SETs were produced when the laser spot was focused on some internal resistors. Closer examination revealed that the resistors were long narrow p-type structures formed in n-wells. Light focused on the resistor increased the number of free carriers, which caused an increase in conductivity. In theory, an increase in conductivity could cause an ASET, but the fact that the ASET amplitude depended on the position of the charge injection along the resistor's length, ruled out conductivity modulation as the sole mechanism responsible for ASET production. An alternate mechanism was proposed to explain this effect: injected charge was separated by the resistor/substrate p-n junction. The charge-separation effect was modeled by replacing a single resistor with two resistors in series, and adjusting their resistances in proportion to their relative lengths. A diode connected to V_{dd} was added to the circuit to simulate the junction, with a current generator across the diode used to simulate the charge injection. **Fig. 37** shows excellent agreement between the charge required to produce an ASET using computer simulation, and that measured by charge injection using a

pulsed laser. This analysis would not have been possible without the detailed spatial information provided by the pulsed laser interrogation. This study has also affirmed the accuracy of the SPICE model used for simulating the ASETs is the LM119.
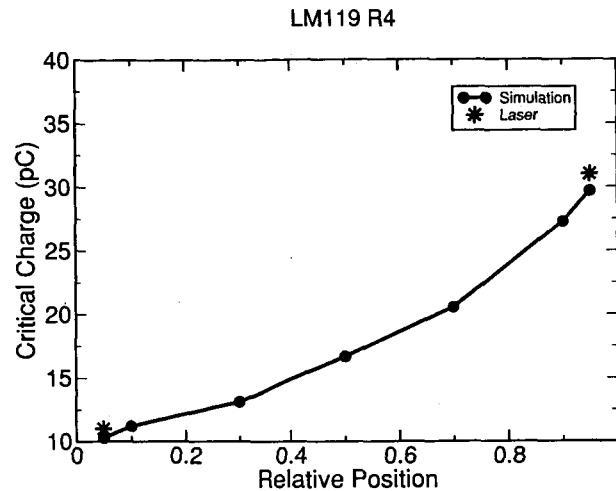
LM119 R4

Fig. 37. Critical charge calculated for ASETs produced in the LM119 voltage comparator (solid line). The two data points were obtained with a pulsed laser [ST02].

In a second example, pulsed laser SET measurements proved essential in the development of an accurate SPICE model for the current source used for the LM111 voltage comparator [ST02]. **Fig. 38** shows a circuit schematic of the differential input pair in the LM111. The pulsed laser identified the C/B junction of transistor Q2 as the area most sensitive to ASETs for the bias configuration under consideration. To simulate an ASET in SPICE, a current source was connected across the C/B junction. However, the direct connection to ground meant that an injected current would flow to ground and not disturb any voltages across the transistor. To accurately reproduce the experimental results it was necessary to include a spreading resistance between the base and the input contact, and to connect the ideal current source between the emitter and base.
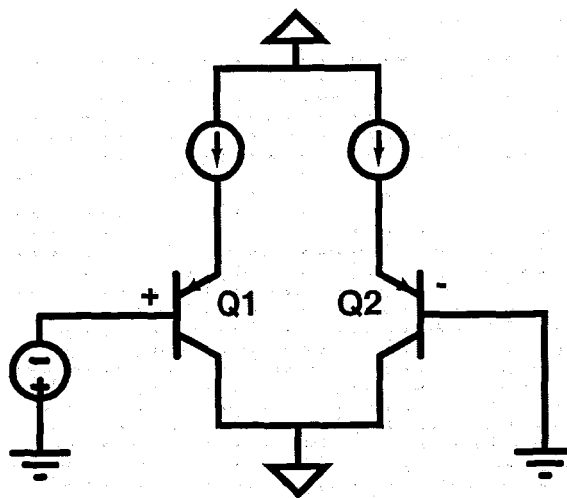

Fig. 38. Schematic showing a differential pair of p-n-p transistors (Q1 and Q2) frequently used in the input section of op-amps and comparators. Also shown are the current sources. Q2 is grounded and Q1 is connected to a bias which controls the current flow through Q1 [ST02].

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Fig. 39 shows how the spreading resistance was included in the model. The Gummel-Poon compact SPICE model includes resistances for the emitter, base, and collector internal to the model, but the ASETs are produced by charge injected across the junctions and the current sources must be connected between the resistances and the internal nodes. With these modifications, the calculated ASET shapes and sensitive junctions agree with those measured with the pulsed laser. This is an example of how the proper experimental calibration of SPICE models is essential for the development of accurate circuit models, and how the pulsed laser provides the quantitative, node-specific information required for such calibrations. We note, also, that the laser-induced ASETs measured for the LM111 exhibit excellent agreement (shape and magnitude) with measurements performed with an ion micro-beam [PE02], as discussed below.
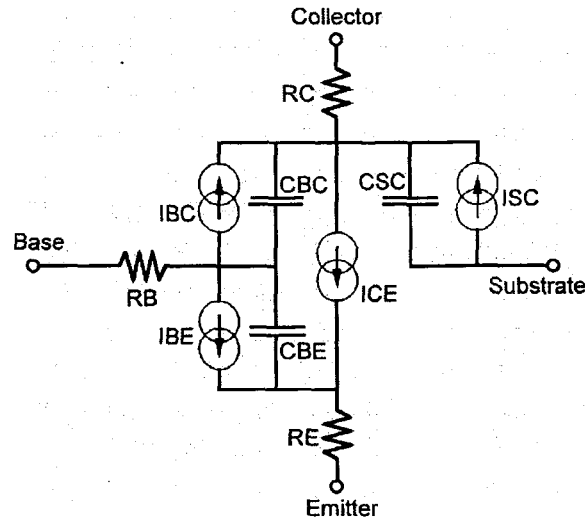

Fig. 39. Parasitic elements included in the SPICE model of a simple p-n-p transistor [ST02].

The third example is that of the LM124 operational amplifier in which a device designated as a resistor in the manufacturer's schematic diagrams was found to be the most sensitive location for ASET production [ST02]. The ASETs produced by charge deposition in this "resistor" were unlike those produced anywhere else in the circuit, having large positive amplitudes with very narrow, almost square wave, characteristics. Those ASETs were observed in both heavy-ion and pulsed-laser experiments (with the pulsed laser results identifying the resistor structure as the origin of the unique transients). This "resistor" is used as a biasing element in the gain stage of the amplifier. Following considerable physical analysis, it was determined that the resistor was fabricated as a floating-base transistor. Once the structure of the resistor was established, it was straight-forward to understand its sensitivity to ASETs: any charge deposited in the "floating" base would cause a large change in the potential that could produce a transient that would propagate to the output of the device. Furthermore, once this information was understood, it was straight-forward to include the floating base transistor in a circuit model that was more complete than that supplied by the manufacturer.

The examples cited above demonstrate clearly how the pulsed laser plays a key role in the development of accurate circuit models.

6.2 Long-Duration ASETs

It has long been recognized that the pulsed laser is a powerful tool for investigating the origins and mechanisms of anomalous SEEs. One particularly interesting, and totally unexpected case was the occurrence of long-duration pulses (LDPs) in the LM6144 operational amplifier [BO04a]. The LDPs were observed during heavy-ion testing at Texas A&M University Cyclotron, and it was the pulsed laser that helped identify the mechanisms responsible.

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The LM6144 was configured as an inverter with gain ($10V/V$) and $V_{cc} = - V_{ss} = 10$ V. With the input set at 625 mV, the DC output is -6.25 V. **Fig. 40** shows the long duration pulses (LDPs) that occurred when the part was irradiated with heavy ions having LETs greater than 50 MeV·cm^2/mg. The longest ASET measured in the heavy-ion tests had a width of 1.5 ms, which is approximately two orders of magnitude longer than ASETs typically observed for similar op-amps. Of particular interest was the fact that the LDP amplitude saturated at about 6 V, which is well short of the maximum possible amplitude of 16.25 V, determined by the difference between the rail (+10 V) and the DC output (- 6.25 V).
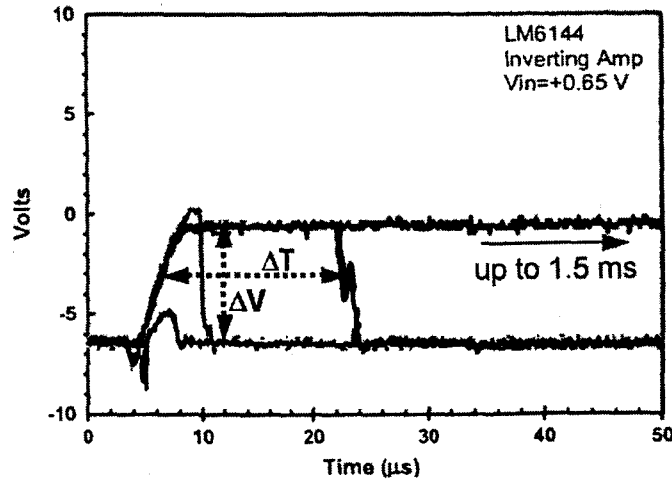

Fig. 40. Long duration pulses (LDPs) observed for the LM6144 exposed to a beam of heavy ions [BO04a]
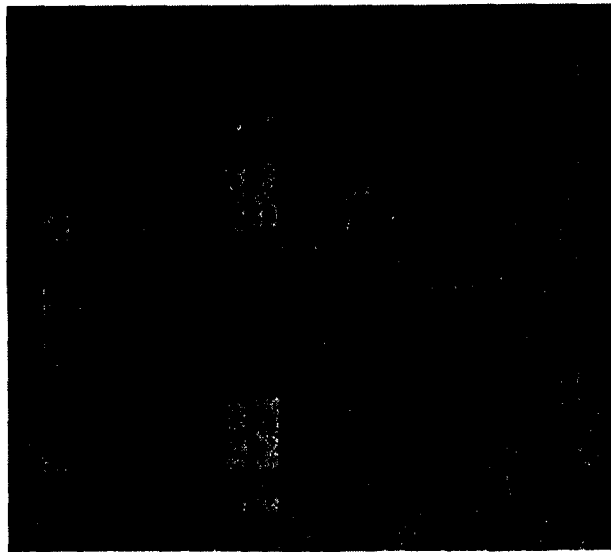

Fig. 41. Photomicrograph of the LM6144. The area containing the ASET-sensitive transistors is marked in black [BO04a].

The pulsed laser was used to determine the origins of the LDPs by scanning the focused laser light across the IC surface while monitoring the output. **Fig. 41** is a photomicrograph of the LM6144. The rectangular area in black indicates the region of the chip where the LDPs originate. A layout of the circuit, provided by the manufacturer, helped identify two n-p-n transistors as the sensitive nodes in question. The two transistors are part of a startup circuit whose function is to force the bias circuit into a particular state so that the op-amp will assume a stable operating state

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when power is first applied. The entire startup circuit is contained in the area demarcated by a thick black line in Fig. 41.

Fig. 42 shows the response of the circuit to a laser pulse focused on one of the two transistors. For this test the configuration of the part was the same as used during the heavy-ion testing except that the input was set at -60 mV instead of +650 mV. Therefore, the DC output was at +0.6 V. The ASET amplitude was - 0.6 V and the duration 25 ms.
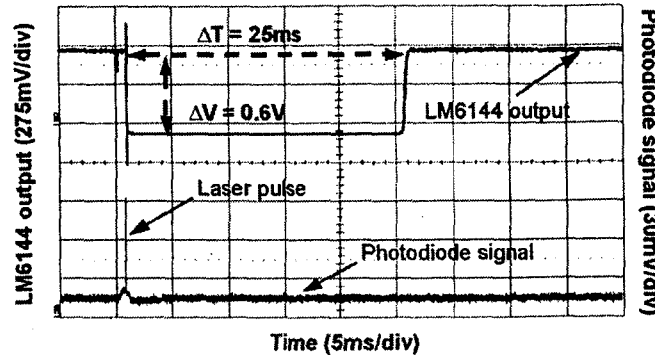

Fig. 42. Two oscilloscope traces, one for the signal from the photodiode monitoring the light emission by the pulsed laser (lower trace) and the other for the ASET obtained from the LM6144 [BO04a].

A detailed study was undertaken to unravel the processes associated with the occurrence of LDPs in this device. It was noticed that background light had a major effect on the duration of the pulse – the LDP persisted as long as any background light was present. There are numerous sources of background light that bedevil the experiment. They include: the light bulb used to illuminate the surface of the chip when positioning the laser pulse on the area of interest; the room lights; and the non-coherent or scattered light emitted by the laser (the scattered light provides a constant, low-level background collinear with the coherent laser beam). Simply blocking the laser beam was not sufficient; it was necessary also to turn off both the room lights and the illuminator before the LDP would disappear. Conversely, with the room lights and the illuminator bulb off, the LDPs persisted even when the coherent laser light was attenuated by rotating a half-wave plate with respect to a polarizer, implicating the role of the un-polarized scattered background light. Evidently, the incoherent scattered light was sufficient for the LDPs to persist indefinitely after their initial generation.

Another phenomenon discovered with the laser was that once a LDP was generated in the presence of background light, it could be removed with a laser pulse directed at a transistor outside the initially sensitive area. This was an important finding that helped explain some of the heavy-ion data. During heavy-ion testing, the delidded part was exposed to light from an ionization gauge used to measure the vacuum level of the beam line. It is believed, though not conclusively demonstrated, that the intensity of the light from the ionization gauge was sufficient to cause a LDP to persist indefinitely. However, once a LDP was generated by an ion strike in the sensitive region, another strike in the surrounding circuit could cause the LDP to switch off. It is believed that the varying lengths of the LDPs measured in the heavy-ion tests are a consequence of the random arrival times of the individual ions exiting the accelerator.

Pulsed-laser testing also revealed that, as the power supply voltage was reduced, the recovery time increased. For example, when the supply voltages were set at ± 10 V, the LDP width was 25 ms, at ± 7.5 V it was 45 ms, and at ± 5 V it was 100 ms.

The explanation proffered by the authors was that there are two different stable operating states for the bias circuit, and that injection of charge onto either one of the two n-p-n transistors in the startup circuit causes the bias circuit to switch into a stable state different from the one it

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entered when power was first applied. A change in the bias circuit affects many transistors throughout the op-amp, and the result is a change in the op-amp's output. As long as even a small amount of charge is continuously being injected into either one of the two n-p-n transistors by background light, the bias circuit remains in the undesirable state. Removal of all external sources of light allows the circuit to return to its original intended state.

The role of the bias/startup circuit was confirmed by computer simulation. All the observed effects mentioned above were simulated. For example, **Fig. 43** shows the results of calculations of LDP-width as a function of supply voltage, and shows general agreement with the experimental results. Once the source of the LDPs was understood, a simple mitigation for the LDPs was devised by adding small capacitors across the base/collector junctions of the two NPN transistors.
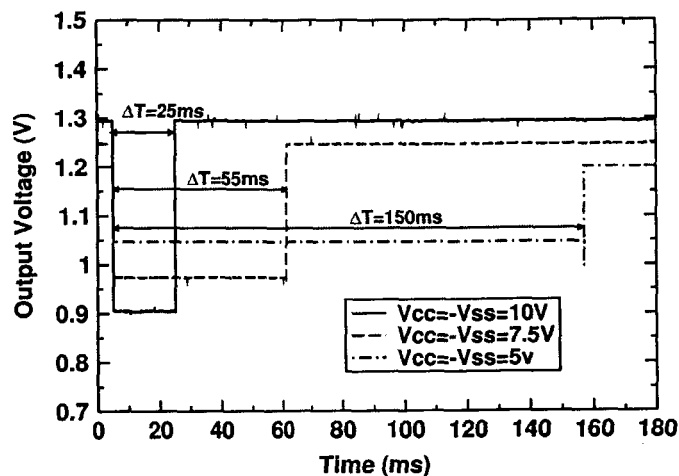

Fig. 43. Simulation results for the effect of power supply voltage on the width and amplitude of the LDPs [BO04a]. As the power supply voltage is increased the recovery of the LM6144 is speeded up and the transients become shorter while their amplitudes increase [BO04a].

The realization that even relatively little background illumination can affect SEE generation means that special attention must be given to reducing all background light when performing either laser or heavy-ion testing. Obviously, background illumination is not an issue in space, but it is a significant issue for ground testing because the IC die must be exposed to the beam. These results reveal that it is not always sufficient to turn off the room lights: all sources of light should be eliminated as a matter of course for any SET experiment.

6.3   ASETs in a Fast Voltage Comparator (LM119)

Mention has already been made of the fact that voltage comparators are used in many different configurations and that the ASET sensitivity depends on the actual configuration implemented. A detailed investigation of ASETs in the LM119 voltage comparator was undertaken with the pulsed laser to study how ASETs are affected by changes in operating conditions [BU01].

The ASET-sensitive transistors were identified by scanning the pulsed laser across the surface of the IC. Two different values of ΔV_{in} were used, i.e., +/- 60 mV. Of the 22 transistors in the LM119, seven are ASET sensitive for ΔV_{in}= +60 mV and eleven are sensitive for ΔV_{in}= - 60 mV. Three of them are sensitive in both configurations. For ΔV_{in} = +60 mV, the most sensitive transistor is the output transistor (Q16), whereas for ΔV_{in} = - 60 mV, the most sensitive is the input transistor (Q1).

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Modeling results have indicated that for small values of ΔV_{in}, the transistor most sensitive to ASETs is the "off" input transistor in the differential input pair. For the case of the LM119, ΔV_{in} must be less than +60 mV. For negative values of ΔV_{in}, the amplitude of the ASET generated at an input transistor shows little dependence on the differential input voltage.

The first accelerator tests of the LM119 indicate no dependence on ΔV_{in}, in agreement with the pulsed laser results [KO00]. However, subsequent pulsed laser testing at reduced values of ΔV_{in} revealed that the LM119 is, in fact, sensitive to ASETs, with the most sensitive device being the input transistor (Q2). [BU01]. Heavy-ion measurements later confirmed that the ASET sensitivity of the LM119 depends on ΔV_{in} when the trigger level was set at 50 mV or lower [JO02]. **Fig. 44** shows the ASET amplitude as a function of ΔV_{in} for a fixed amount of laser pulse energy deposited in the sensitive region of Q2. Clearly, the ASET sensitivity of Q2 varies, being greatest for very small or very large values of ΔV_{in}. The reason no ASETs were observed in the original data is that both ΔV_{in} (>100 mV) and the trigger level (2.5V) were too large.
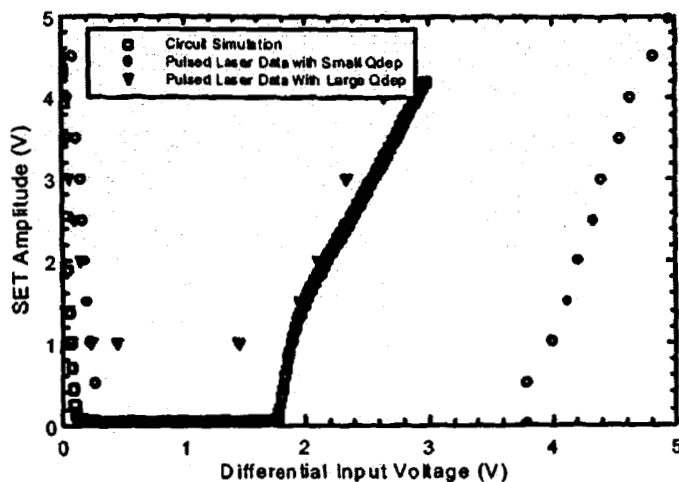

Fig. 44. ASET amplitude as a function of differential input voltage for light focused on transistor Q2 of the LM119 voltage comparator. The light remained focused on the same spot for all measurements and its intensity was also kept constant [BU01].

Other ASET characteristics (rise time, fall time, amplitude and threshold) may be investigated with the pulsed laser. Table I lists the results obtained when transistor Q15, located close to the output, is irradiated. Since the differential input-voltage is positive, the DC output is at 5V and transients appear as pulses with negative amplitudes. Increasing the supply voltage causes the fall time to decrease, but it has no effect on the subsequent rise time. The latter is due to the fact that the LM119 has an open collector that is connected to V_{DD} through a "pullup" resistor. The combination of the resistor and the capacitance of the large output resistor together determine the recovery time. Since neither of those two values changes as the supply voltage increases, the recovery time is constant. Notice that the amplitude of the negative-going pulse increases as the supply voltage increases, while the energy to produce the ASET decreases.

TABLE I

DEPENDENCE OF ASET CHARACTERISTICS ON SUPPLY VOLTAGES ($V_{DD} = -V_{SS}$)

Supply Voltages	5V	10V	15V
Leading Edge Fall Time (ns)	48	20	15
Trailing Edge Rise Time (ns)	220	220	220
Amplitude (ΔV)	-5	-5.6	-6
Threshold (a.u.)	8	5	4

One LM119 was irradiated with 3-MeV protons to produce radiation damage in the form of both total ionizing dose and displacement damage and the effect of damage on the energy threshold needed to produce an ASET was measured. With increasing proton induced damage, the amount of energy needed to produce an ASET also increased. **Fig. 45** shows the dependence of threshold energy for three different transistors of the LM119 as a function of proton fluence [BU01]. It is clear that the energy threshold increases with increasing proton fluence.
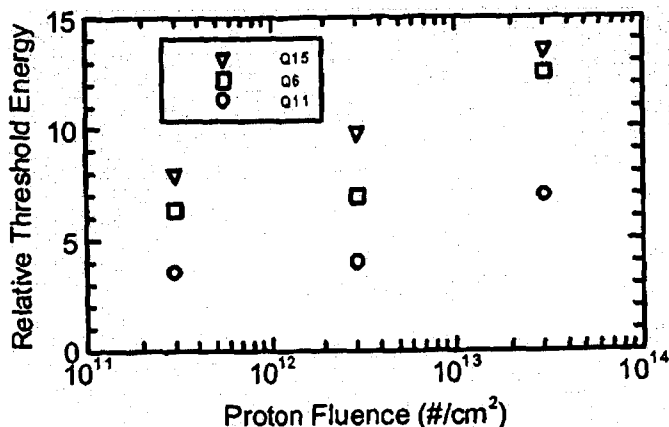

Fig. 45. Relative laser energies to produce the ASETs with the same amplitude for three different transistors (Q15, Q6, and Q11) as a function of proton fluence.

Finally, the effects of changing the value of the "pullup" resistor on ASET shapes and thresholds were measured [BU01]. A reduction in the value of the resistor by almost an order of magnitude (from 1.7 kΩ to 0.157 kΩ) had no effect on the leading edge fall time or the threshold, but the recovery time was reduced from 145 *ns* to 50 *ns*.

6.4 Application Dependence of ASETs in the LM111 Voltage Comparator

As was mentioned in the previous section, if a valid model for an IC is available, computer simulation may be used to study ASETs in ways that are sometimes difficult or impossible to do experimentally. For example, it is straight-forward to use computer simulation to study the dependence of ASET shape and sensitivity on the values of internal resistors and capacitors.
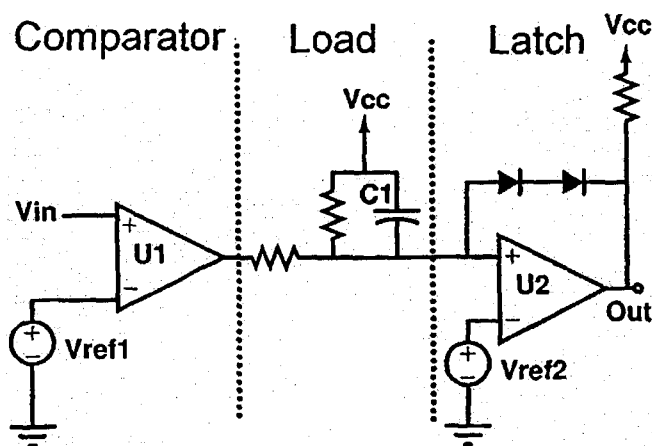

Fig. 46. Components used in an undervoltage detector. U1 and U2 are both LM111 voltage comparators [ST01].

Dramatic effects on ASET sensitivities have been found when the load is slightly altered. The application chosen for analysis was an under-voltage detector incorporating the LM111 voltage comparator [ST01]. **Fig. 46** shows the application, which includes a comparator, a load,

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and a latch. Under normal circumstances, the output of the circuit is high, but if the voltage drops below a reference voltage (V_{refl}), the output latches into a low state. **Fig. 47** shows a simplified diagram of the LM111 using macromodels for parts of the circuit not sensitive to ASETs. Calculation revealed that the transistors most sensitive to ASETs were Q1, Q8 and Q14.
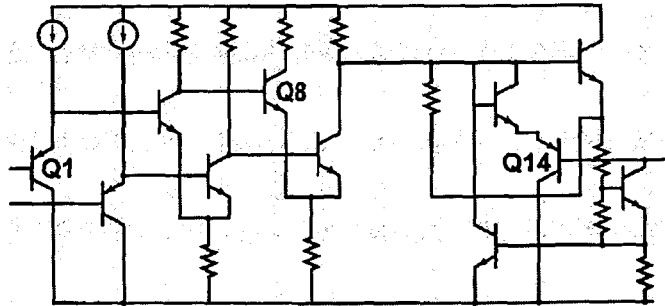

Fig. 47. Simplified circuit diagram of the LM111 op-amp [ST01]. Q1, Q8 and Q14 were identified as the transistors most sensitive to ASETs. Macromodels were used to describe the rest of the circuit.

ASETs generated in U2 did not cause latching. Therefore, the study concentrated on ASETs generated in U1 that were able to switch the state of the latch. The most significant result was that the identity of the transistor most sensitive to ASETs depended on the external application circuitry, in particular on the value of the capacitor (C1). For values of C1 up to 0.3 nF, Q1 was the most sensitive transistor. For values greater than 0.4 nF and less than 1.3 nF, Q8 was the most sensitive transistor, whereas for values greater than 1.2 nF, Q14 was the most sensitive. The study also found unexpected behavior of the critical charge with increasing capacitance. **Fig. 48** shows that the critical charge for a single transistor increased slightly as the capacitance increased, but when the identity of the most sensitive transistor changed, the critical charge increased by orders of magnitude [ST01].
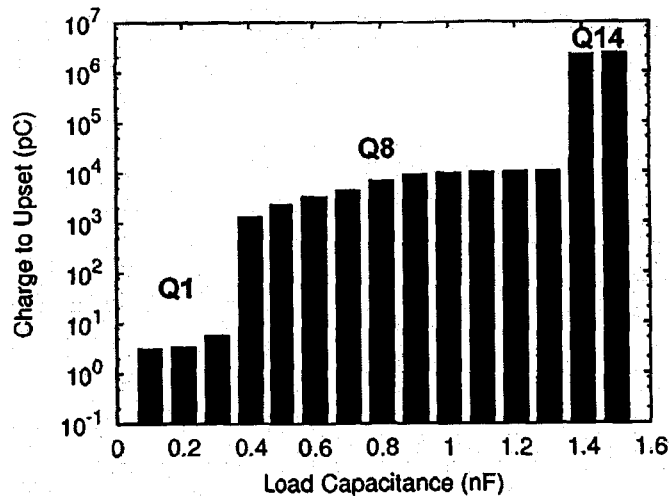

Fig. 48. Sensitive transistor and critical charge for different values of load capacitance [ST01]. As the load capacitance increases so does the critical charge. There are large discontinuities when the most sensitive transistor changes identity.

The implications of these calculations for laser testing are obvious: Since the identity of the transistor most sensitive to ASETs sometimes changes abruptly with small increases in capacitance, pulsed laser testing should not be confined to only one transistor. Instead, for each application a complete scan of all the transistors in the circuit must be undertaken to identify which ones are the most sensitive for each application.

6.5 Determination of Critical Charge

In Section 3.4, mention was made of the fact that the LET thresholds for some linear devices are quite small (~1 MeV·cm²/mg) yet they have large critical charges, suggesting long collection depths. These results were obtained by comparing the amount of laser pulse energy required to produce an ASET with that obtained from simulations [PE01].

Pulsed-laser testing of the LM111 established the minimum amount of energy deposited in the most sensitive transistor to produce an ASET with amplitude of 0.1 Volt. For ΔV_{in} = +20 mV, the most sensitive transistor was the "off" transistor in the differential input pair. The measured energy deposition for laser light was 2 pJ, which was equivalent to 1 pC. This value agrees well with the results of computer simulation for the same transistor (1.1 pC), and with the results of broad-beam heavy-ion testing (~1 pC) and focused ion microbeam measurements (1.2 pC). The excellent agreement observed between the laser and heavy ion results, once again demonstrates the utility of the pulsed laser technique.

For the LM124, the value for Q_{crit} measured with laser light agreed with the value calculated using SPICE for the transistor identified as the one most ASET sensitive [PE01]. However, the pulsed laser and the focused ion microprobe revealed that the most sensitive device in the LM124 was not a transistor, but a resistor. The identification was made easy by the unique pulse shape shown in Fig. 35. It was not possible to generate this type of waveform from a simple resistor using SPICE. After much physical analysis, as described above, the structure of the resistor was determined to be that of a floating base transistor and the micromodel for that structure was included in the circuit [PE01]. Subsequently, SPICE was successfully used to generate the ASETs shown in Fig. 35.

The fact that Q_{crit} is quite large, in the range between 0.3 pC and 1.0 pC for the LM111, yet LET_{th} was small (1 MeV·cm²/mg) suggests a long charge collection length – from 30 μm to 100 μm. The implications of these results are that LET_{th} must be determined using ions with sufficient range (> 100 μm). The two-photon results describe above for the LM124 provide insight into this parameter [MC03].

7.0 Data Presentation

The point has been made numerous times already that merely counting the number of events is not sufficient to characterize the ASET sensitivity of analog devices. What is needed in addition is specific information on pulse width and amplitude.
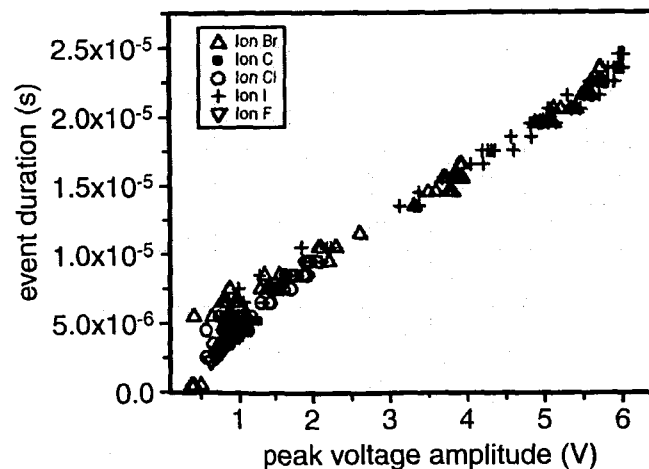

Fig. 49. ASET width as a function of amplitude for the LM124. The data points are for a variety of heavy ions spanning a wide range of LETs [AD00].

Time restrictions at accelerators require that ASETs be captured with a digital oscilloscope and stored for later analysis. When the time for data analysis arrives, one is faced with the prospect of having to deal with a database containing potentially several hundred ASETs with many different shapes and sizes. Only amplitude (ΔV) and width (Δt) are needed to determine whether ASETs pose a problem for amplifiers and comparators. The fine details of the pulse shape are generally irrelevant. A convenient and compact way of presenting that information is needed. The first publication to address this issue suggested that plots of ΔV versus Δt provide a useful way of presenting relevant ASET characteristics. **Fig. 49** is such a plot for the LM124 [AD00]. All the data points fall on a straight line, which means that there is only one kind of ASET whose width increases in proportion to its amplitude. Also, the higher LET ions produce the largest ASETs.

The method for displaying ASET characteristics described above was expanded upon in a subsequent publication. **Fig. 50** is another plot of ΔV vs Δt for the LM124. It includes data from many runs, each with a different ion LET [SA02]. For this case, both positive and negative pulses were included, and the different families of points reveal that ASETs from a single amplifier may have a variety of shapes. A point worth stressing is that the authors of the publication clearly identified the exact conditions under which the data were obtained. This is important because the distribution of points is not necessarily the same for different configurations.
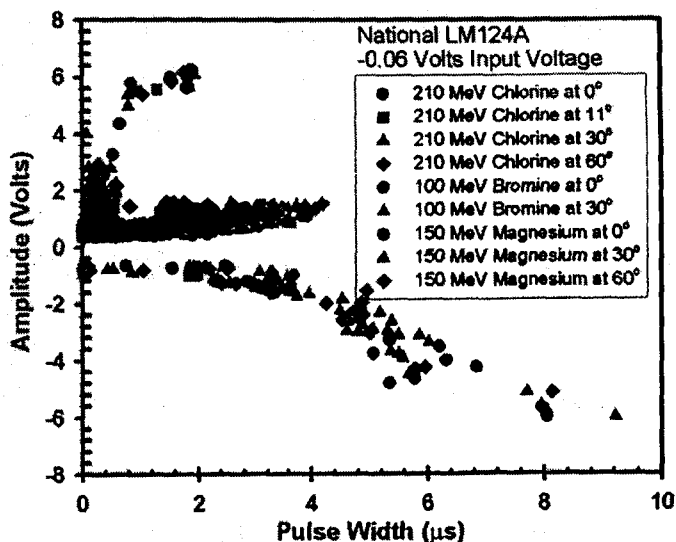

Fig. 50. Plot of amplitude versus width for the LM124 configured as a closed loop non-inverting amplifier with gain (2X) [SA02]. Both positive and negative pulses were included.

Plots of ΔV vs Δt are easily generated using a computer program that examines each pulse, measures its amplitude and width, and plots the data. The Radiation Effects and Analysis Group at NASA/GSFC has developed a computer program that analyzes large numbers of transients and automatically generates plots of ΔV vs Δt for a variety of operating conditions. A quick visual scan of actual ASET shapes should be done to make sure that the computer program correctly plots ΔV vs Δt for all the ASETs. Some ASETs are bipolar, and it is important that the program identify and plot both positive and negative components of a transient. Measuring width is not straightforward because some ASETs have complicated shapes. **Fig. 51** shows a complicated ASET with a very narrow pulse on top of a much broader pulse. The magnitude of the narrow component changes relative to the broad component as the ion LET changes. The very narrow component should be ignored if it is too fast to affect the circuit, and only the amplitude and width of the broad component should be measured.
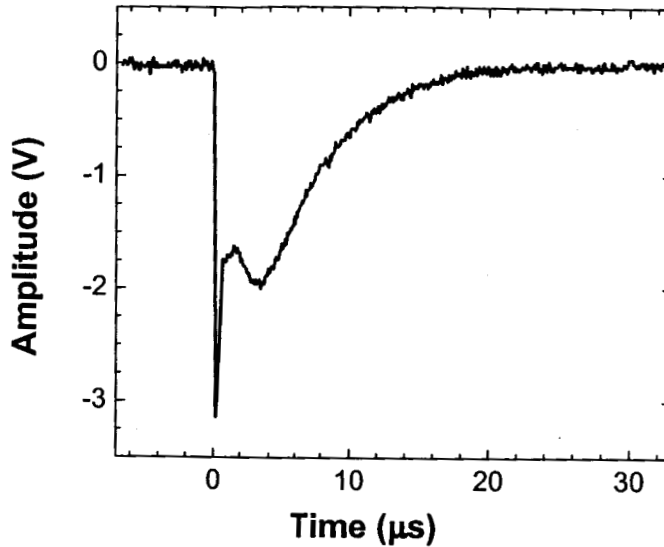
50

Fig. 51. Example of a complex ASET with both fast and slow components that complicate measurement of ASET width.

Regardless of whether the data is displayed as in Fig. 49 or Fig. 50, the same analysis can be used to determine whether any of the ASETs pose a threat to a system containing the analog device being tested. The analysis involves determining the critical values of pulse amplitude (ΔV_{crit}) and width (Δt_{crit}) for propagation through the system. Those values are included in the plots by drawing vertical and horizontal boundary lines that separate propagating ASETs from non-propagating ASETs. The result is a "phase space" for ASETs. The phase space for a particular device depends on its application.
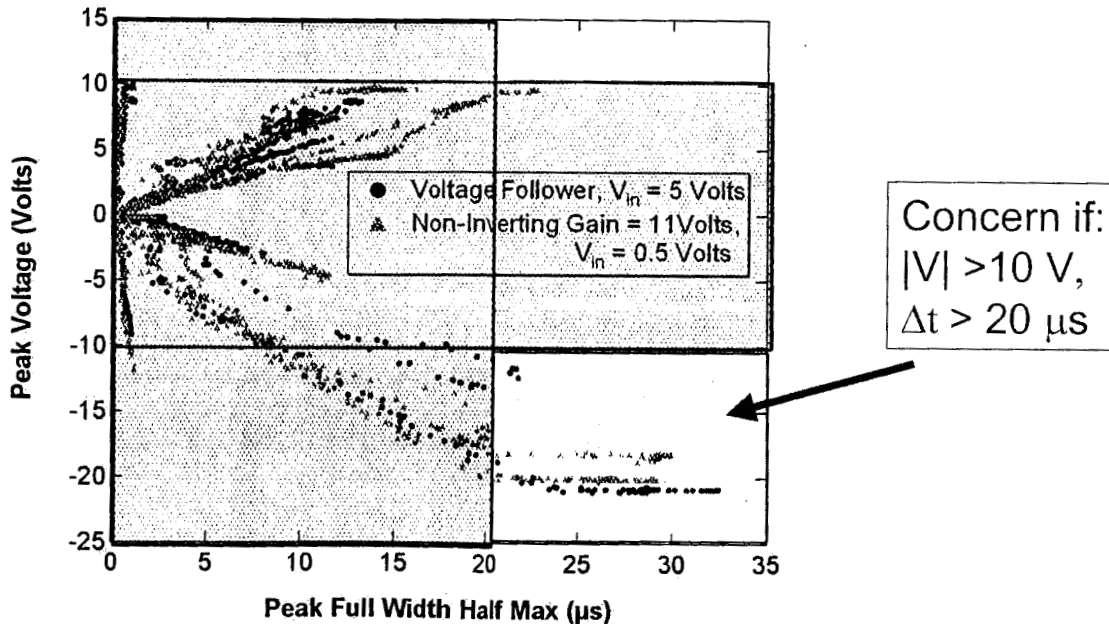

Fig. 52. Plot of amplitude versus width for the LM124 showing the phase space where ASETs will have no effect on the system and where ASETs will have an effect on a system ($\Delta V>10V$ and $\Delta t>20$ μs).

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Fig. 52 is a plot of ΔV versus Δt for the LM124 op-amp. The plot includes the phase space separating ASETs that would affect a particular follow-on circuit from those that would not. For this example, only pulses with amplitudes greater than 10 V and widths longer than 20 μs need be considered [BU04]. The figure includes data obtained for several ions with different LETs. To calculate the ASET cross-section as a function of ion LET, this type of plot would have to be generated for each ion LET. In each case only the points beyond the lines representing $\Delta V = 10$ V and $\Delta t = 20$ μs need by counted.

The advantage of including all the points on a single plot is that it presents a complete picture of ASET shapes. The drawback is that the clutter makes it difficult to count precisely the number of points representing propagating ASETs. These types of plots are useful for identifying which ASETs pose a potential threat for a system.

The next step is to plot σ(LET). The plot will be depend on the application – in this case the application is MAP, which was discussed in the Introduction. **Fig. 53** shows two plots for the PM139 voltage comparator manufactured by Analog Devices [PO03]. The differential input voltage was set at 1 Volt. The plot with the higher saturated cross-section and lower LET threshold was obtained by counting all transients generated in the PM139 with amplitudes greater than 0.5 volts. The second plot includes only those transients with amplitudes greater than 2.5 Volts that would produce resets in the processor. The saturated cross-section in the second plot is a factor of four smaller than the first, and the LET threshold is a factor of two higher. One can use the Figure-of-Merit (FOM) approach to get a rough estimate of the change in the error rate. The error rate, given by the FOM, is proportional to the saturated cross-section and inversely proportional to the square of the LET threshold [PE98]. Therefore, the actual error rate will be smaller by a factor of sixteen $(4 \times (2)^2)$ than the error rate calculated by counting all transients with amplitudes greater than 0.5 V.
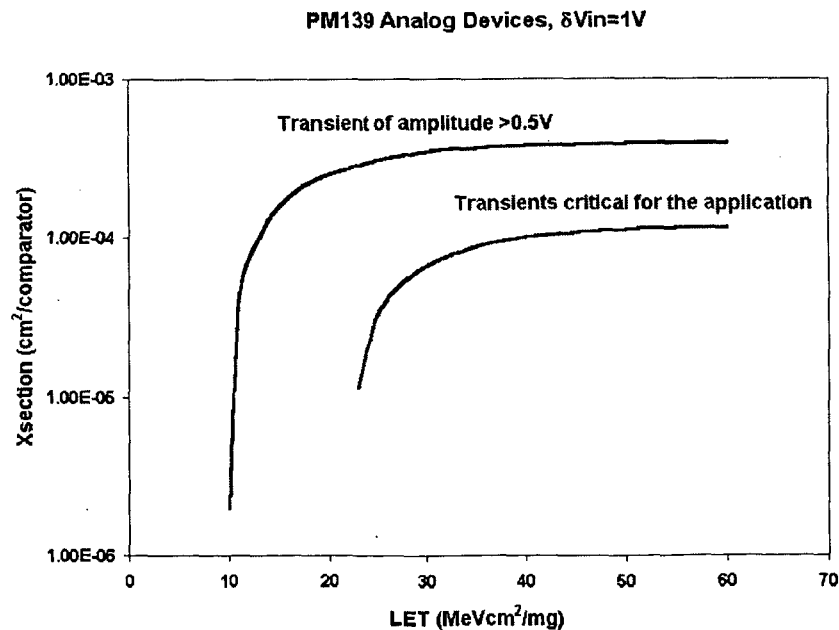

PM139 Analog Devices, δVin=1V

Fig. 53. ASET cross-section as a function of ion LET. In one case (upper curve) all transients with amplitudes greater than 0.5V are counted. In the actual application, only ASETs with amplitudes exceeding a value determined by the application are counted [PO03]. Because the LET threshold is higher and the saturated cross-section is lower for the curve applicable to the application, the error rate will be a factor of 16 smaller than if all the ASETs are counted.

An alternate approach to presenting ASET data is to include another variable, such as pulse amplitude, in plots of σ(LET). **Fig. 54** is a plot of cross-section vs LET for the OP-27 operational amplifier that includes pulse height [SA04]. The plot is based on the observation that for each LET there is a wide spectrum of pulse amplitudes due to different ion strike locations. The plot was generated by binning the data according to pulse height. The next step was to integrate the frequency of pulse heights so that each data point represented the number of pulses with amplitude equal to or greater than that height. Finally, a plot of σ(LET) was generated that includes contours of constant amplitude. **Fig. 55** shows such a plot for the OP-27 [SA04]. The glaring deficiency of this approach is that it fails to include information about pulse width. In these plots, large pulses with very short durations that fall into the non-propagating category are not distinguished from long pulses that would propagate. Therefore, no definitive conclusions may be drawn regarding which of the data points represent propagating ASETs. A more useful representation would be a three-dimensional plot that included contours of both amplitude and width.
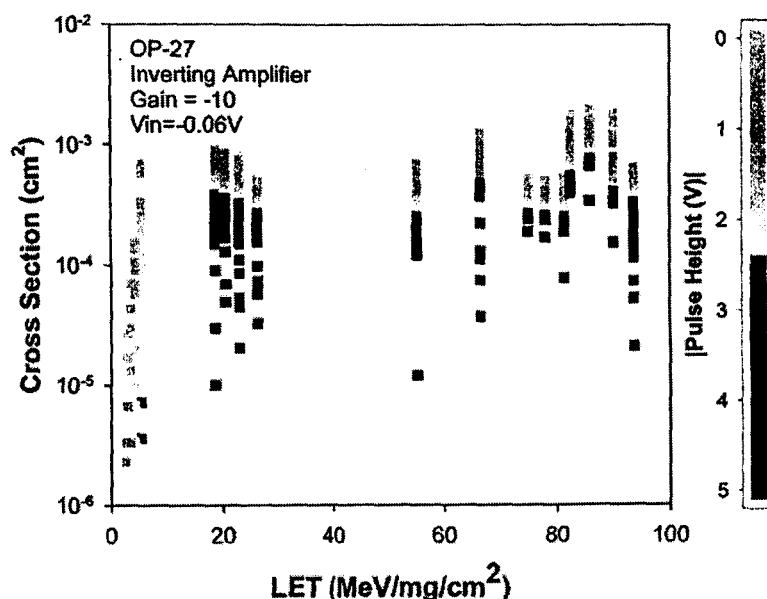

Fig. 54. ASET cross-section as a function of ion LET for the OP-27 configured as an inverting amplifier [SA04]. The figure also includes amplitudes, and the larger the amplitudes, the smaller is the cross-section.

Fig. 56 illustrates the useful information that may be obtained from $(\Delta V, \Delta t)$ plots, while at the same time serving as a warning that inspection of the actual ASETs is always advisable. [SA04] The figure contains data obtained from the OP-27 operational amplifier and shows that pulses produced by higher LET ions are generally shorter than those produced by lower LET ions. This has implications for hardness assurance as it is generally agreed that one need test with only the highest LET ions as they will produce ASETs with the largest pulses. The data in Fig. 56 show that this is not always the case. However, inspection of the actual ASETs reveal that most of them are bipolar in character and that the relative sizes of the negative and positive components change with ion LET. As the LET increases, the positive component grows in both amplitude and width at the expense of the negative component. The computer program selected only the component with the larger amplitude, regardless of width, and it ignored the smaller component, which, in some cases, had the greater width and therefore presented more of a threat. These results emphasize that the program used to generate plots of ΔV versus Δt should include both positive and negative components of bipolar ASETs to avoid generating potentially misleading data.
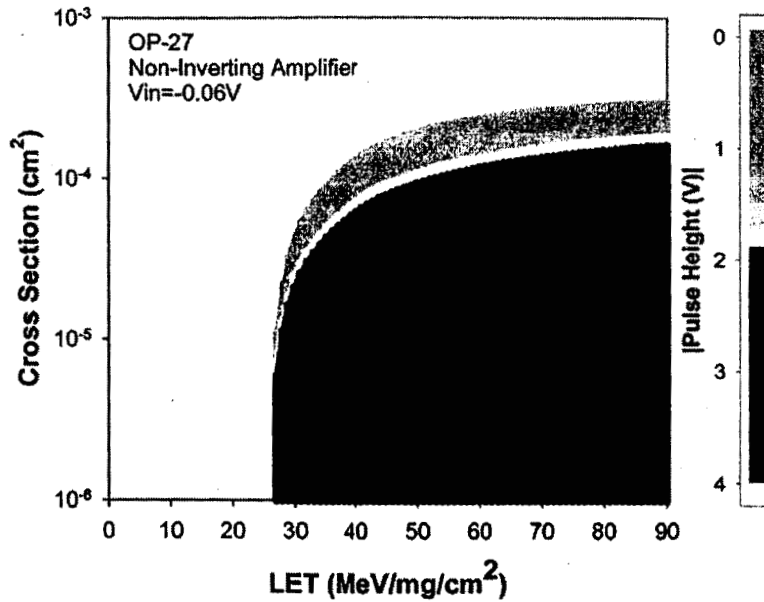
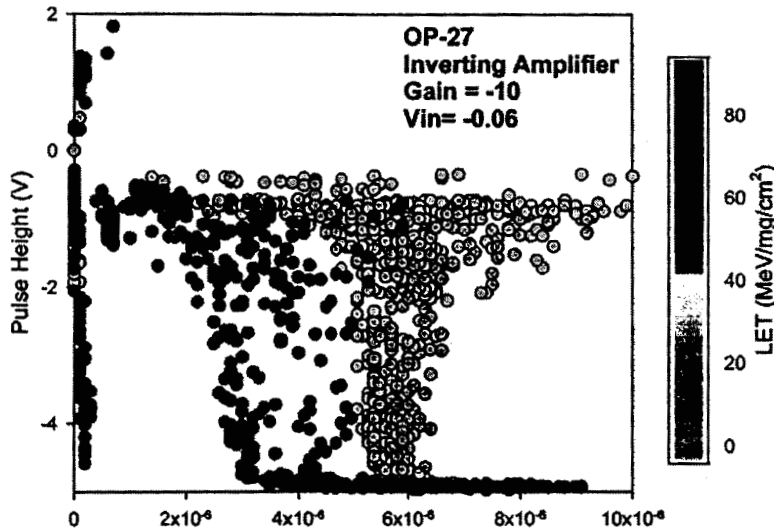**Fig. 55.** Contour plot of the cross-section as a function of ion LET for different ASET amplitudes [SA04].

Fig. 56. Pulse-height versus pulse-width for the OP-27 as an inverting amplifier with ΔV_{in} = -0.06V [SA04]. The figure shows that some of the largest pulses have the narrowest widths.

The same kinds of plots may be generated using a pulsed laser. The laser light is focused on each sensitive transistor and all the ASETs are captured as the laser pulse energy is gradually increased. One has the option of plotting the data for a single transistor or for all the transistors in the IC. **Fig. 57** shows the data points generated with the laser [BU04]. The usefulness of the laser data stems from the fact that, because the identity of each transistor in the IC is known, the source of each $(\Delta V, \Delta t)$ point is known. A circuit designer can use this information when devising ways to harden the circuit.

Another point is that a comparison can be made of the ASETs produced by heavy ions and by laser light. All the data obtained from the two methods are included in a single plot and the fact that the two sets of data agree validates the approach of using the pulsed laser for hardness qualification discussed in a later section.

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Presentation of ASET data is also a problem for those doing simulation. Large numbers of transients can be generated from computer simulations, and a compact and manageable way of presenting the data is necessary. All the information for ASET propagation in a system may be combined together into plots of ΔV vs Δt, just as was done for the data obtained from accelerator and pulsed-laser testing. The data from both simulation and experiments may be combined in a single ($\Delta V, \Delta t$) plot to assess the accuracy of the simulations.
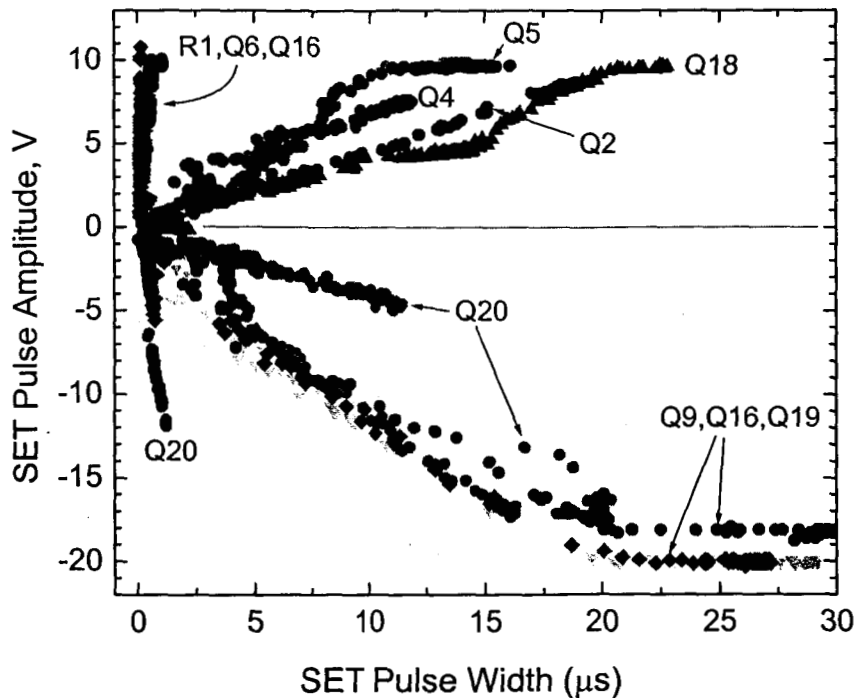

Fig. 57. Pulse amplitude versus pulse width for ASETs generated at various transistors in the LM124 op-amp obtained with a pulsed laser [BU04].

8.0 ASETs in Operational Amplifiers and Voltage Comparators

This section introduces the reader to some of the unique aspects of ASETs in op-amps and voltage comparators.

8.1 Operational Amplifiers

Op-amps were among the first linear ICs tested for ASET sensitivity. It was recognized early on that op-amps contain multiple amplification stages capable of amplifying small voltage glitches in transistors located in input stages. By the time those glitches reach an output, they will have been magnified to such an extent that they may be able to induce errors in mixed-signal applications.

ASET amplitude and width are dependent on a number of factors, some internal and some external to the op-amp. These same factors also affect ASET sensitivity. In the next two subsections, external and internal factors will be considered [ST02a].

8.1.1 External Factors

It seems reasonable to assume that ASETs will be affected by such external factors as operating configuration, supply voltage, input voltage, output load, and gain. Initial studies in a few op-amps indicate that some external factors have an effect and others do not. More

systematic studies are necessary in order to identify which factors are important, especially given the wide variety of op-amp designs available. The results presented in the following sections are for a small number of op-amps and are not meant to be definitive.

8.1.1.1 Device Configuration

Op-amps may be used in a number of different configurations, including voltage follower, inverter with gain and non-inverter with gain. **Fig. 58** shows the various configurations.

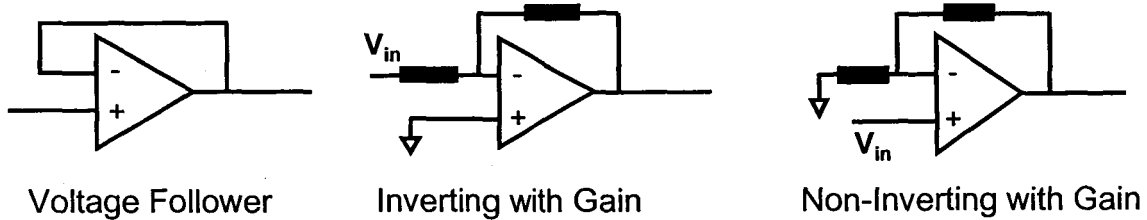Voltage Follower   Inverting with Gain   Non-Inverting with Gain

Fig. 58. Three different configurations in which an amplifier can be operated.

The LM124 was selected to determine whether changes in operating conditions affect ASET cross-section. **Fig. 59** shows the ASET cross-section as a function of ion LET for three different configurations and for a variety of input bias conditions [PO03]. The figure surprisingly shows that the cross-section is independent of configuration, supply voltage and input voltage. These results imply nothing about the effects of different configurations on transient shape because the oscilloscope was set to trigger if the output deviated by ±0.5 V from the DC level, regardless of ASET shape. Transient shapes cannot be compared unless they are from the same physical location, something that is not possible with broad-beam testing. These results imply only that the number of transients with amplitudes greater than 0.5V is independent of operating configuration if the fluence and LET remain fixed. The ASET shapes may have changed, but the total number of transients did not.
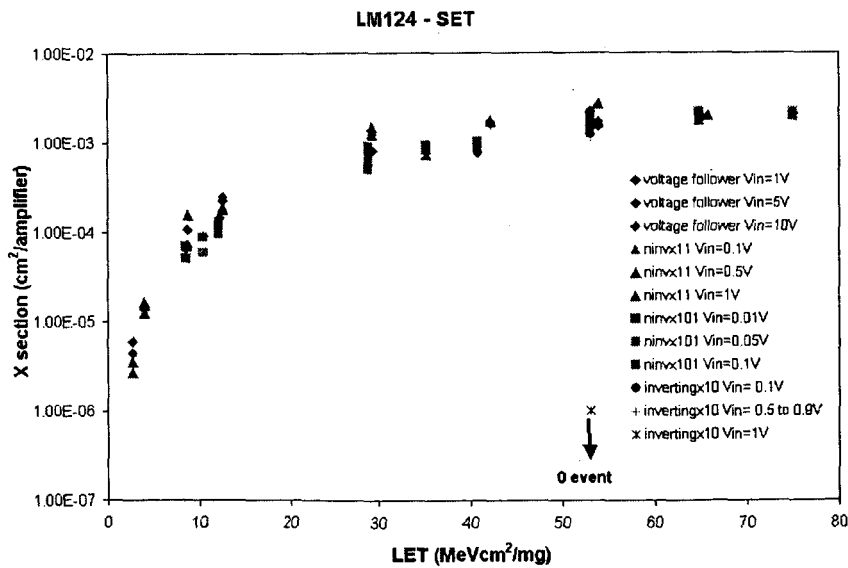

Fig. 59. ASET cross-section as a function of ion LET for a number of different operating configurations and input voltages [PO03].

Confirmation that the ASET shapes for the LM124 were unaffected by changes in operating conditions required the use of a pulsed laser. The laser light was focused on the sensitive junction of a transistor in the LM124 configured as a voltage follower. The configuration was switched to that of an inverting amplifier with gain of ten without moving the device or changing the location or energy of the laser beam. No noticeable changes were observed in the ASET shape. In addition, the measured energy thresholds were also independent of configuration. The procedure was repeated for a number of different transistors in the LM124, and in each case no obvious changes were detected. Not only did the pulsed laser confirm the data obtained with heavy ions, it also revealed that the ASET shapes were independent of configuration, information that could not be obtained with broad-beam heavy ion testing. Note that these results are for only two configurations, so they merely confirm the heavy-ion results but in no way suggest that this is universally true.

8.1.1.2 Power Supply Voltage

A unique aspect of operational amplifiers is that they are designed to operate over a wide range of power supply voltages. For example, the LM124 can operate with power supply voltages from 5V to 15V. Power supply affects ASETs in two ways. An increase in the power supply voltage causes an increase in Q_{crit}, which makes the device less susceptible to ASETs. However, a larger power supply increases the available drive, which should magnify some of the smaller transients. Also, a larger the supply voltage makes possible ASETs with larger amplitudes because of the increased "overhead" between the DC output and the rail, A comprehensive study has, to date, not been undertaken to determine how supply voltage affects ASET shape or sensitivity.

8.1.1.3 Input Voltage

Fig. 59 suggests that input voltage has very little effect on cross-section, i.e., LET_{th} and $\sigma_{sat}(LET)$ appear to be independent of input voltage over a large range that extends from 0.01 V to 10 V. Because the cross-section is determined by counting the total number of transients captured with an oscilloscope, small changes in ASET shape would have no effect on the cross-section measured under these conditions.

Device input voltage may affect the magnitude of an ASET if the DC output level is close to a "rail". As an illustration, we consider the case of an amplifier with non-inverting gain of two and voltage supply of 10 V. If the input signal is a DC voltage of 1 V, the output is at 2 V and the maximum amplitudes of positive and negative ASETs are +8 V and -12 V, respectively. If the input signal is increased to 4 V, the maximum amplitudes are +2 V and $-$ 18 V. For most ASETs, an increase in the amplitude is accompanied by an increase in the width. Therefore, in the example cited above, increasing the input signal level reduces the threat posed by positive ASETs to follow-on circuits, but increases the threat posed by negative ASETs.

8.1.1.4 Gain

An interesting and relevant question is whether gain affects ASETs. An attempt to answer this question involved an experiment to measure ASET cross-section of the LM108 as a function of gain. The part was configured as an inverter with two different values of R_2/R_1, i.e., -1 and $-$ 10. Gain was found to have no effect on the measured cross-section. This is not surprising if the cross-section is calculated from the number of ASETs captured with a fast oscilloscope set to trigger at some relatively low voltage level [EC94].

The optimum method for studying how gain affects ASET shapes is computer simulation. Simulations were carried out for ASETs generated in the LM124 op-amp for different values of gain using a model validated with the results of pulsed-laser measurements. To ensure that the

DC level would not affect the amplitude of the transients, the input was set to 0 V. The calculations were for ASETs generated in transistors located in the input, gain and output stages of the op-amp [ST02a]. The largest effects were for transistors in the input stage where increasing the gain from 2X to 50X caused a broadening of the transient from about 2.5 μs to 10 μs, a factor of about four. Transients originating in the gain exhibited a similar increase in width. However, transients originating in the output exhibited a much smaller increase. **Fig. 60** shows that transient width increased from about 1 μs to 1.5 μs. The calculated transients for transistors in the input and gain stages showed very little change in shape as long as the gain increased was less than a factor of 5. Larger increases caused proportionally greater increases in width. In all cases, changing the gain had no effect on the amplitudes of the transients.
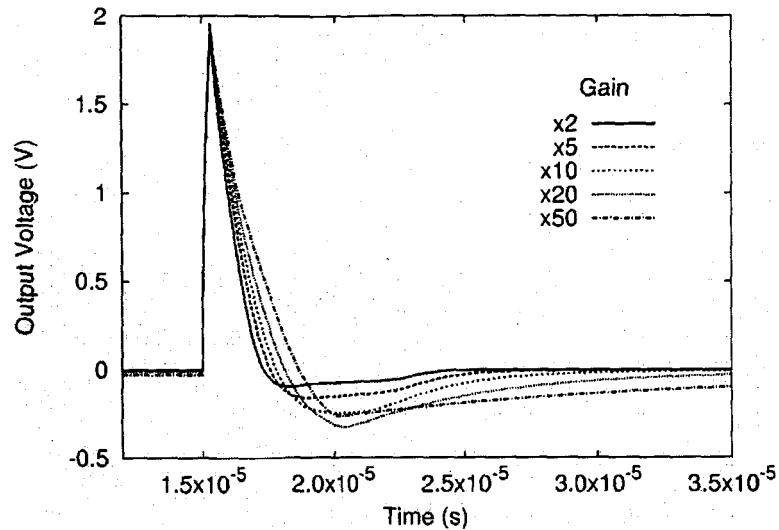

Fig. 60. Simulation of the effect of gain on the shape of an ASET generated at transistor Q14 in the output section of the LM124 op-amp [ST02a]

The cross-section depends on both the amplitude and width of the transient. Large increases in width caused by changing the configuration from one with a small gain to one with a large gain would require that the measurements be repeated.

Calculations were also performed to determine whether the transient shapes were affected by changing the values of the resistors R_1 and R_2, while keeping the gain (R_2/R_1) fixed [ST02]. **Fig. 61** shows that increasing the values of resistors R_1 and R_2 caused a widening of the pulses generated at a transistor in the gain stage of amplifier. Maximum width increases were a factor of two. Again, there was little effect on the amplitude. The explanation for the broadening of the transients with increasing gain in the LM124 has to do with the presence of a compensating capacitor between in the input and gain stages that acts as a low-pass filter. Increasing the gain means the bandwidth of the low-pass filter decreases resulting in a broadening of the pulses.
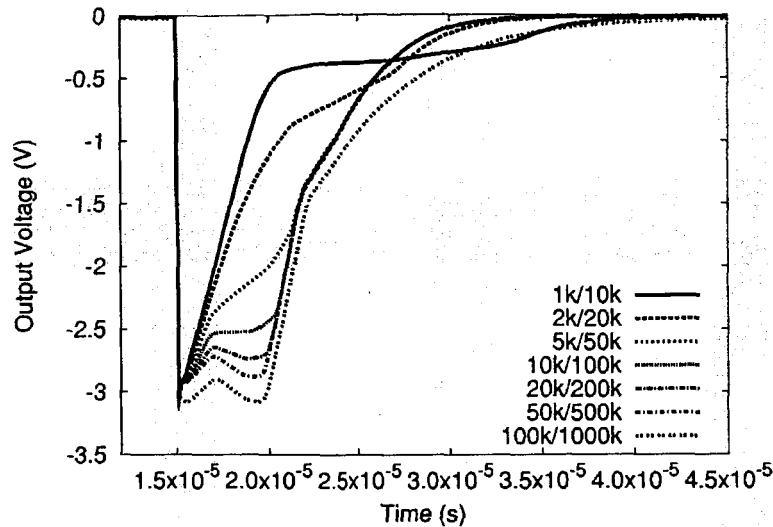
Fig. 61. SET dependence on resistance values for a fixed gain on Q9 in the gain stage [ST02a].

The above results explain why the measured cross-sections did not depend on gain. Since only the width changed appreciably when the gain changed, the number of transients captured on an oscilloscope would not be expected to change. Whether gain is important for ASET cross-sections for a particular configuration depends on the magnitude of gain. Very high values of gain will give rise to wide transients, and wide transients are more likely to cause upsets in mixed signal applications.

These findings are important because they serve to underscore the point that measurements of cross-section as a function of ion LET are not sufficient to characterize an analog IC for ASET sensitivity. Transient amplitude and width are two criteria that should be used to judge whether an ASET will propagate through the subsystem of the intended application.
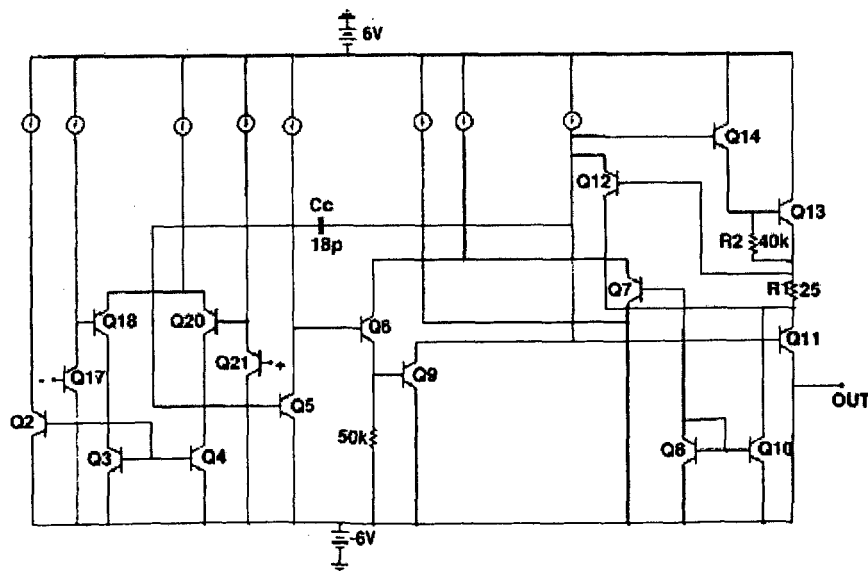
8.1.2 Internal Factors

Fig. 62. Simplified circuit diagram for the LM124 [ST02A].

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Fig. 62 shows a simplified schematic of the LM124. Like most amplifiers, the LM124 consists of three stages – input stage, amplifier stage and output stage. Resistors are added for negative feedback to obtain a stable output with a gain given by the ratio of the two resistor values. An amplifier's internal gain and bandwidth play a crucial role in determining ASET responses. Three transistors, one in each section of the amplifier, were selected as sources of ASETs to investigate how changes in the internal operating parameters affect ASET shape and sensitivity [ST02A].

8.1.2.1 Compensating Capacitor

The LM124 contains a compensating capacitor between the input and gain stages to prevent oscillations [ST02a]. Its value was found by physical analysis to equal 18 pF. The first transistor selected for investigation was Q4 in the input stage. An ideal current source was applied across the same junction as was irradiated with the pulsed laser. The amplitude and width of the current pulse were adjusted until the calculated ASET shape matched that obtained with the pulsed laser. Next, the size of the capacitor was increased in steps from 18 pF to 40 pF to determine how the ASET was affected. **Fig. 63** shows that with increasing capacitance the ASET amplitude is reduced and the width is increased. This is consistent with the gain and output sections acting as a low-pass filter with a cutoff frequency determined by the value of the capacitor.
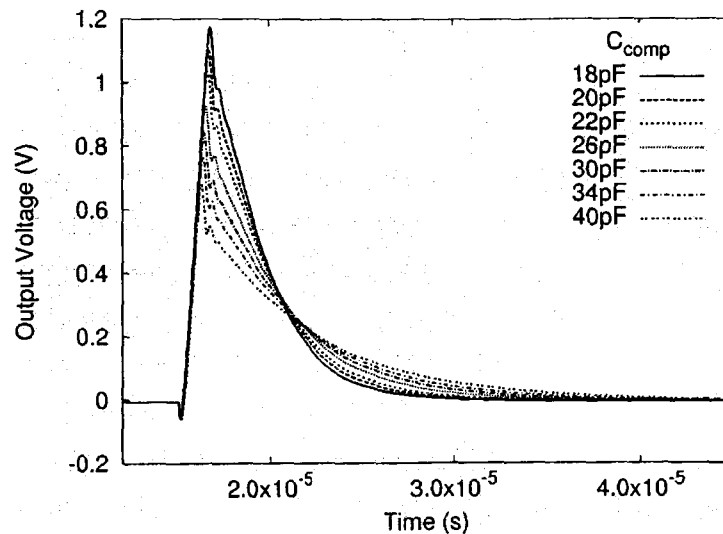

Fig. 63. Simulated ASET at transistor Q4 of the LM124. With increasing value of the compensating capacitor, the ASET's amplitude decreases and its width increases [ST02a].

The next transistor studied was Q9 in the gain stage. **Fig. 64** shows how the shape of the ASET changed with capacitance. The ASET is complicated, having both fast and slow components. Changing the capacitance had no effect on the fast component, but did increase the recovery time for the slow component. The large amplitude produced by Q9 implies that it is the transistor most sensitive to ASETs.
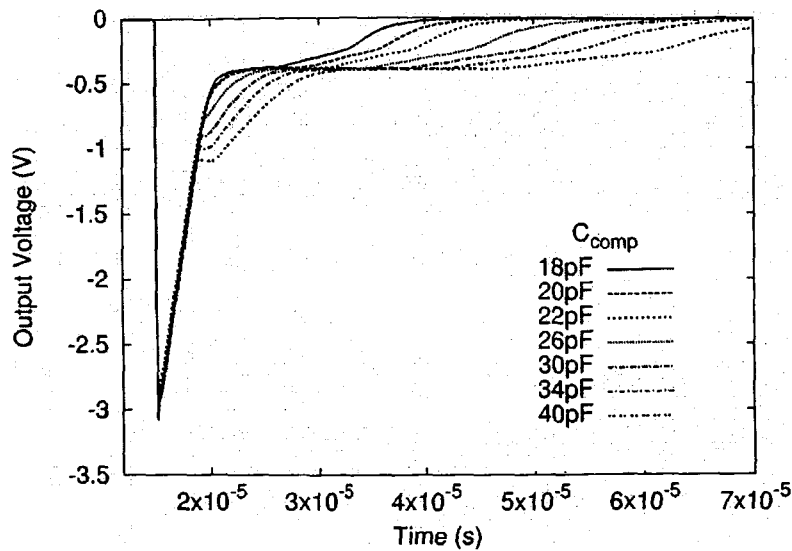
Fig. 64. Simulated ASET at transistor Q9 in the gain stage of the LM124. With increasing value of compensating capacitance, the ASET's width increases [ST02a].

The transistor in the output stage selected for investigation was Q14. **Fig. 65** shows that the shape was not affected by changes in capacitance because it was beyond the influence of the capacitor.
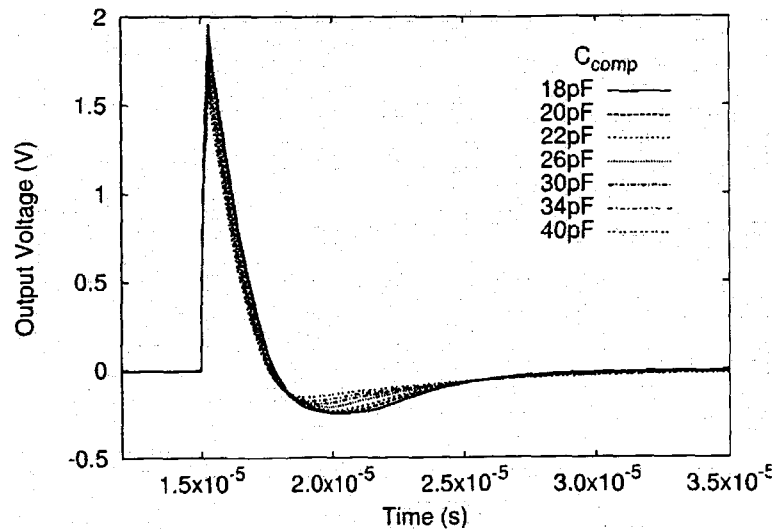

Fig. 65. Simulated ASET at transistor Q14 in the output stage of the LM124. The shape is essentially independent of the value of the compensating capacitance [ST02a].

The general conclusion from this work is that both internal and external factors affect the shape and sensitivity of ASETs. Circuit simulation is the best way to determine what factors will affect ASET sensitivity.

8.2 Voltage Comparators

Voltage comparators are amplifiers without feedback. Their outputs are high for a positive value of differential input voltage ($\Delta V_{in} = V^+ - V^-$) and low for a negative value. A voltage comparator (LM111) was among the first analog devices tested for ASETs [KO93]. The device was operated with power supplies set to $V_{dd} = \pm 15$ V and the output was connected through a 1.5 kohm resistor to V_{dd}. **Fig. 66** shows an example of one of the ASETs captured during testing. The

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ASET cross-section was measured as a function of ion LET by counting all negative pulses whose amplitudes exceeded 1 V. **Fig. 67** shows the cross-section curves for three values of differential input voltage, i.e., 0.05 V, 0.3 V, and 0.7 V. Although there are relatively few data points, the reduction in the cross-section with increasing differential input voltage is evident. This behavior has been observed in all voltage comparators, regardless of whether they are fast or slow.
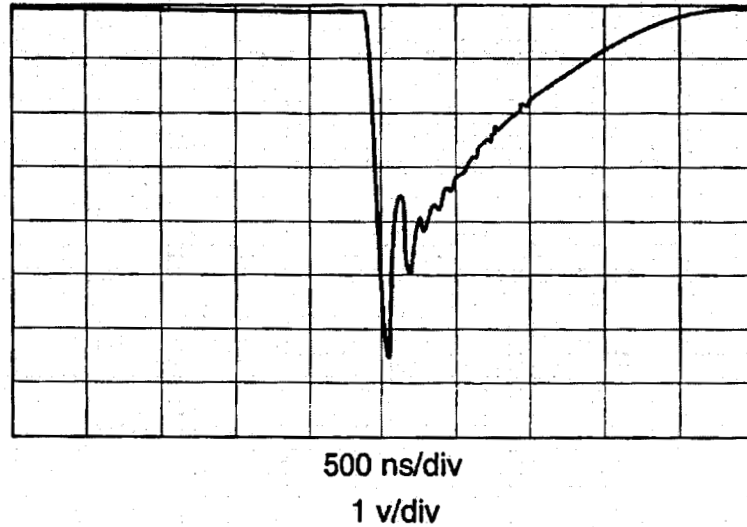
500 ns/div

1 v/div

Fig. 66. One of the first ASETs reported in the literature. The ASET was produced by irradiating an LM111 voltage comparator with heavy ions and capturing the voltage transient with an oscilloscope [KO03].
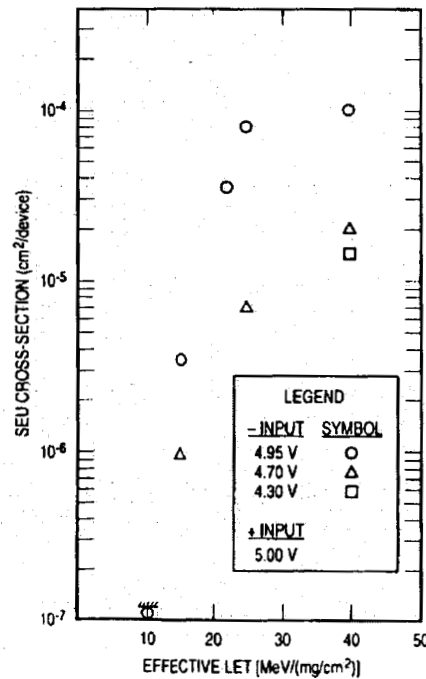
Fig. 67. ASET cross-section as a function of ion LET for three values of differential input voltage for the LM111 voltage comparator [KO93].

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Fig. 68 shows more clearly the same dependence on ΔV_{in} for the LM139, another voltage comparator [KO97]. The figure shows that increasing ΔV_{in} causes an increase in LET_{th} and a decrease in the saturated cross-section. This behavior is consistent with a decrease in the sensitivity of the "off" transistor in the differential input pair as ΔV_{in} is increased. At sufficiently high values of ΔV_{in}, the transistor is no longer sensitive, which results in a decrease in the total ASET cross-section.
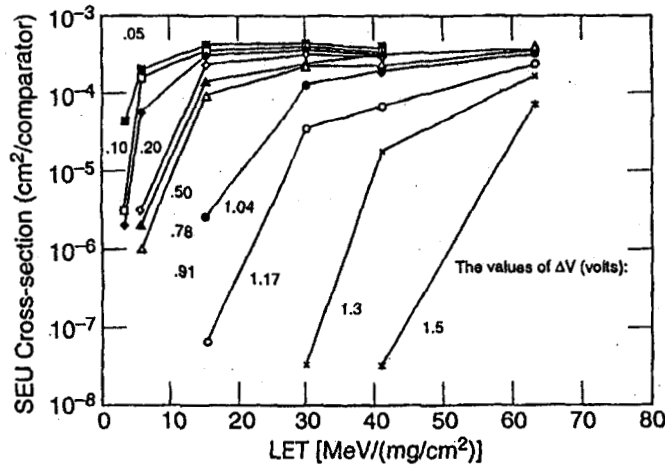
Fig. 68. ASET cross-section as a function of ion LET for the LM139 for different values of ΔV_{in} [KO97].

9.0 Hardness Assurance and Qualification

The goal of a hardness assurance (HA) program is to minimize the risk posed by the radiation environment for circuits used in space systems. HA methodologies have been used for many years in the areas of total ionizing dose and displacement damage dose. In fact, HA guidelines have been developed for total dose and neutrons (MIL-HDBK-814) and for dose rate (MIL-HDBK-815).

Fig. 69. Very long ASETs produced in the OP293 during heavy ion irradiation [LA03].

The large number of malfunctions in space systems attributable to ASETs has stimulated interest in a HA program specifically for ASETs in linear devices. The first such attempt used a combination of existing heavy-ion data, circuit simulations and pulsed laser testing for op-amps and comparators to 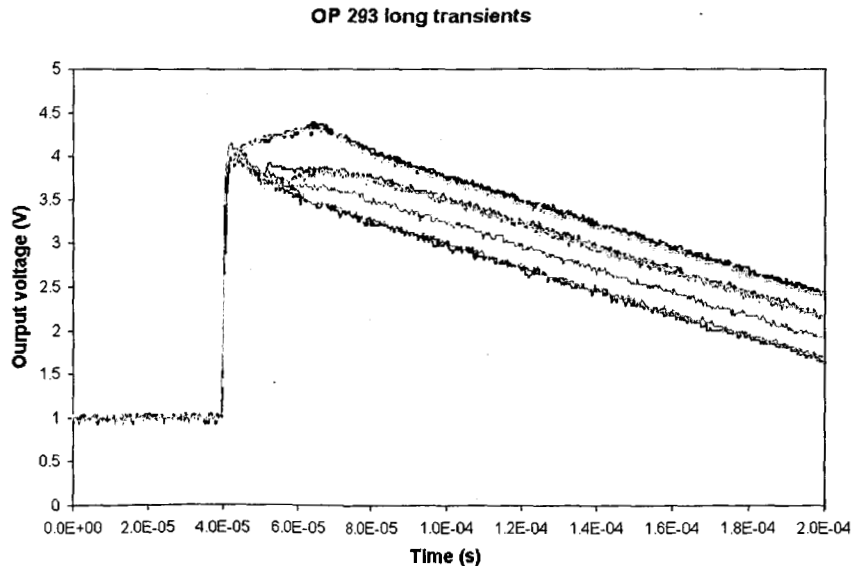determine whether ASETs constituted a threat to the system. [MA01] Those that did were deemed unacceptable and those that did not were deemed acceptable. In the absence of radiation data, it was assumed that ASETs in op-amps and comparators were rail-to-rail with widths no greater than 20 µs and 10 µs, respectively. If the bandwidth of a subsystem prevented propagation of those ASETs, the part was assumed to be radiation hard.

The discovery of millisecond long ASETs in the LM6144 [BO04a] and the OP293 effectively doomed that approach [LA03]. Long ASETs in the LM6144 have already been discussed. They only occur with ions having LETs greater than 50 MeV·cm^2/mg, which means they would occur very infrequently in space and do not present a significant threat. However, long ASETs were also observed in the OP293 at relatively low LETs. The part was tested with three different ions having LETs of 8.5 MeV.cm^2/mg, 20 MeV.cm^2/mg and 43 MeV.cm^2/mg. The longest ASETs lasted for more than 200 µs. **Fig. 69** shows some of the long ASET observed in the OP293. Ions having smaller LETs produced ASETs with smaller widths. The threshold for transients lasting more than 200 µs was about 16 MeV·cm^2/mg and for transients lasting longer than 150 µs was about 10 MeV·cm^2/mg. Even with ions having LETs of 8.5 MeV·cm^2/mg the longest transients exceeded 100 µs. The heavy-ion data were supplemented with data from the pulsed laser, which showed that the duration of the transient appeared to be proportional to the difference between the rail voltage and the nominal output voltage. This means that for a rail voltage at the maximum rating for the part and a nominal output of 0 volts, ASETs as long as 1 ms may occur. These results make the above hardness assurance approach problematic.

A more rigorous HA program was proposed for ASETs [PE04a]. Such a program must satisfy the following steps:
1. Identification of the causes of a circuit's failure,
2. Identification of failure modes,
3. Determination of a failure level,
4. A method for testing for failure,
5. Sufficient parts (> 10) to gather statistically significant data,
6. Assignment of parts to a hardness category.

Each of the steps mentioned above requires further clarification because ASETs are fundamentally different from total ionizing dose and displacement damage.

Since ASETs are caused by energetic particles, the particle radiation environment in space must be well characterized in order to quantify the threat. The usual approach is to calculate the particle LET spectrum for the mission, for which knowledge of the orbit, launch date and mission duration are required. Most models used to describe the radiation environment are not very accurate. Models of the near-earth environment are fairly accurate when averaged over the long term (~10 years) but may be way off over the short term. Models for galactic cosmic rays and solar particle events assume worst-case conditions, so they generally overestimate the threat. Considering all the uncertainties, environmental calculations may be off by up to an order of magnitude.

The failure modes of concern in linear ICs are ASETs. A linear IC is never used in isolation, but is always part of what will be referred to as a subsystem. In a previous section, it was pointed out that not all ASETs will upset a subsystem. Small ASETs will have no effect and may be ignored. The failure mode is defined in terms of critical values for ASET amplitude (ΔV_F) and width (Δt_F). It is the job of the system designer to determine the critical values by performing a detailed electrical analysis of the complete subsystem. The analysis may be done by using a

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circuit simulator program such as SPICE and representing all the components in the subsystem with macromodels. The critical values of ΔV and Δt are determined by gradually increasing the amplitude and width of an ASET until subsystem failures occur. Only ASETs that exceed the critical values for amplitude and width need be considered.

Failure levels are specified based on mission requirements. The most obvious failure metric for ASETs in linear devices is the error rate, defined as the number of upsets per unit time. Depending on the criticality of the subsystem function, allowable upset rates can vary significantly.

The next step is to do testing to determine the error rate. Testing involves exposing a statistically significant number of parts (more on this later) to an ion beam at an accelerator and measuring the ASET cross-section as a function of ion LET. As described in the experimental section, the cross-section is defined as the ratio of the number of ASETs to the fluence. ASETs that do not meet the minimum requirements for ΔV and Δt will have no effect on the system and should not be included in the calculation of the cross-section. The experiment must provide values of cross-section at a minimum of four different LETs if a Weibull function is used to fit the data. The Weibull fitting parameters are extracted and used as input for CREME96. Additional information concerning the amount of shielding, orbit parameters, launch date, and mission duration are required.

The error rate obtained from the heavy-ion data is compared with that specified for the mission. A metric known as the radiation design margin (RDM) is used to classify the part. RDM is the ratio of the maximum mandated error rate to the experimentally obtained error rate. If the RDM is less than two, the part is considered unacceptable. If the RDM is between two and ten, the part may be used with the understanding that mitigation may be required for critical applications. Any part for which the RDM is greater than ten is considered non-critical and may be used without reservation. The factor of ten takes into account all sources of errors, including environment models, interaction models, experimental uncertainty and part-to-part variations.

Any proposed ASET HA program must deal with two issues unique to ASETs. One is the small number of parts that are usually tested, and the other is the dependence of σ(LET) on the device operating conditions.

Consider first the issue of the number of parts tested. The TID HA guidelines specify that a statistically significant number of parts be tested because the TID sensitivity can vary greatly from one part to another, sometimes even within the same lot. Normally a minimum of ten devices is required. Since all the devices can be exposed simultaneously to gamma rays in a Co^{60} cell, obtaining good statistics is generally not a problem. In contrast, ASET testing is done by exposing one part at a time to a beam of ions at an accelerator. ASET testing suffers from all the limitations associated with heavy-ion testing, i.e., limited access to the facility, limited time at the facility and considerable expense. As a result, the radiation effects engineer is expected to make a decision on whether parts will meet mission requirements based on testing two or three linear devices.

In many cases the ASET sensitivity of a particular device type does not vary significantly from one part to another. This is not surprising given that the ASET sensitivity depends primarily on geometrical factors and doping levels that are tightly controlled by the device manufacturer. The one parameter that is not well controlled is substrate doping. Because variations in substrate doping tend to have negligible effect on a device's electrical performance, circuit manufacturers are willing to accept substrates with doping levels that vary over a wide range. This presents a problem when testing some devices for ASET sensitivity. Normal transistor operation occurs relatively close to the silicon surface, but ASETs can involve charge collection from regions well below he surface (~100 μm for the LM111). Variations in substrate doping will alter the depth

from which charge collection occurs and will affect both the LET threshold and cross-section. As long as all the parts are from wafers with the same doping levels, the ASET sensitivity should not vary from one part to another. One way to ensure this is that all the parts tested have the same date and lot codes so that only one or two parts need to be tested for ASETs in order to make acceptable rate predictions in space.

Occasionally, manufacturers make design changes that can have a large effect on ASET sensitivity. Also, there are large differences in ASET sensitivity among devices of the same type but from different manufacturers due to design variations. For example, differences in the ASET sensitivity of the LM124 op-amp manufactured by Texas Instruments and National Semiconductor have previously been observed. [MA01] As long as the devices being tested are from the same date and lot codes, a statistically significant number of devices needed for ASET HA testing may be as low as three.
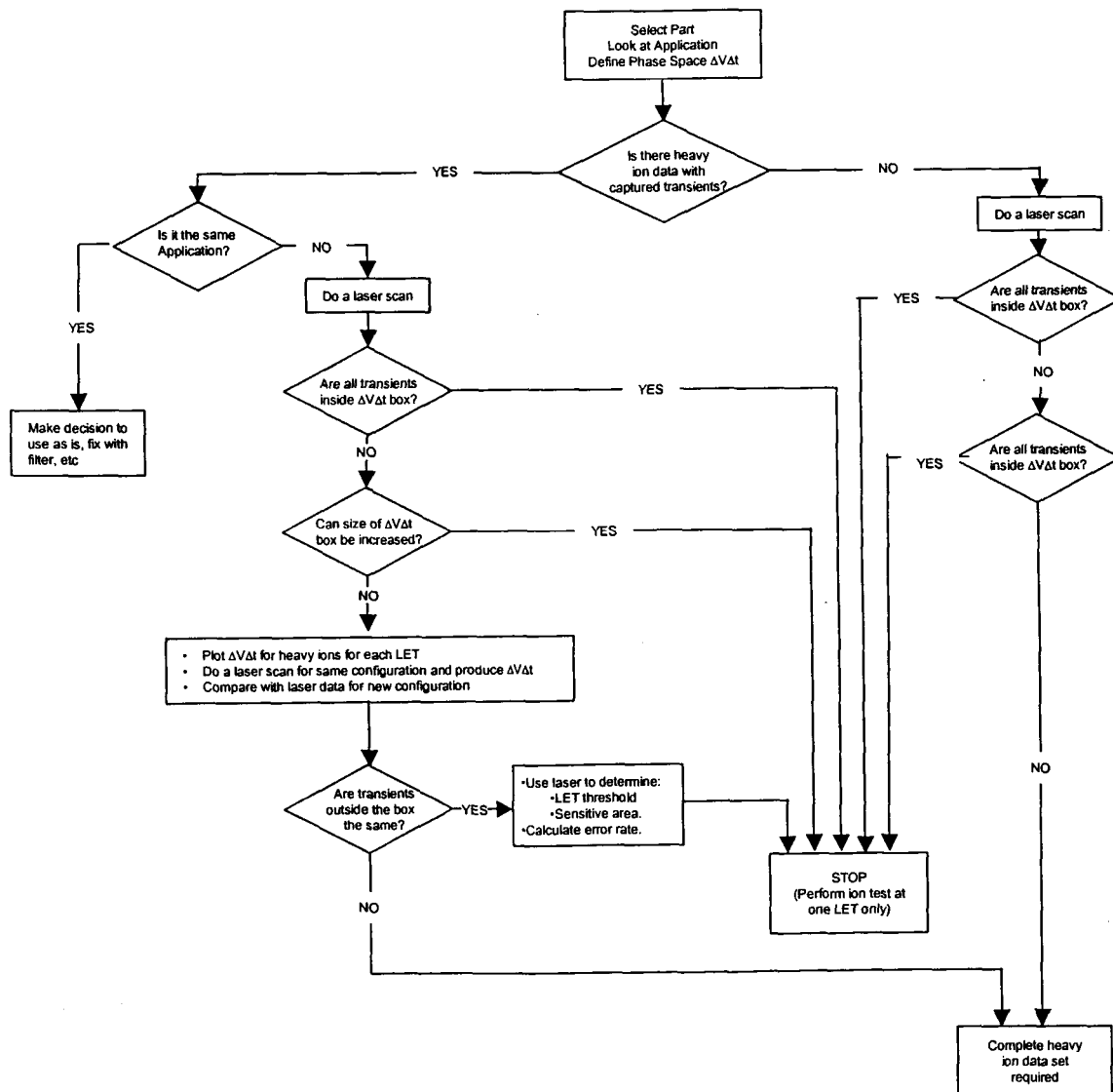

Fig. 70. Steps involved in using a pulsed laser to reduce the amount of testing for a linear device [BU04a].

The second point – that the ASET cross-section in some linear devices is very sensitive to operating conditions – presents another challenge for HA. Consider, for example, the ASET cross-section for a comparator, which exhibits a strong dependence on ΔV_{in}. It is clearly impractical to use heavy ions at an accelerator to measure the cross-section for all values of ΔV_{in} under all conditions of power supplies and load. This is where the pulsed laser could be used to obtain additional data to aid in the qualification.

A HA program requires that parts from the latest production lots be tested periodically to measure their ASET sensitivity to ensure that the levels have not changed. Rather than having to go back to an accelerator to do the testing, a pulsed laser could be used to monitor the sensitivity levels of all the transistors in the ICs. That part of the HA program would involve comparing the laser pulse energies needed to produce ASETs in the latest ICs with those needed for a standard IC that had previously been tested with both heavy-ions and pulsed laser light. If no change in the ASET sensitivity was detected, the part could be considered as having met the required levels of hardness assurance.

The pulsed laser could also be used to reduce the amount of heavy-ion testing needed to qualify parts. The process would involve collecting data on ΔV vs Δt for all ASETs [BU04]. **Fig. 70** shows the steps involved.

The first step is to determine whether there is any ASET data *for the operating configuration of interest*. Data should include plots of σ(LET) together with complete waveforms for all the captured ASETs for each value of ion LET. That data may be used to generate plots of ΔV vs Δt as described in Section 8.

In order to establish the minimum acceptable values of amplitude and width, it is necessary to consult a design engineer to determine the conditions under which SETs will propagate through the system. There are two options available, depending on the availability of ASET data.

9.1   No Heavy-Ion ASET Data Available

In the absence of ASET data, the first step would be to probe all the transistors on the chip using the laser to determine whether any of the ASETs lie outside the area in ΔV-Δt phase space defined by the threshold failure values of ΔV_{th} and Δt_{th}. If all the points lie inside the box, the part is deemed non-critical. To confirm that all SETs are within the area of non-transmission in ΔV-Δt phase, accelerator testing can be done using only ions that result in the worst-case ASETs. If some of the ASETs are outside this window, a design engineer should be consulted to determine whether the system can be modified to increase ΔV_{th} and/or Δt_{th} to prevent SET propagation. Such modifications may involve the addition of a filter, for example. If such changes can be made, the device should be tested in the worst case condition. If they cannot, a complete characterization with heavy ions is necessary.

9.2   Heavy-Ion ASET Data Available

There are two courses of action available when ASET data exist. One is for the case where the operating configuration is identical to the one of interest and all the ASETs are available. No further testing is required, and the decision on whether to accept the device is relatively straightforward. If the device meets all the requirements it may be used as is, but if it does not either some form of mitigation may used or the part is deemed unacceptable.

A different course of action is required if the available data are for a different operating configuration. The first step is to scan all the transistors using the pulsed laser to determine whether any SETs will propagate for the configuration of interest. If all the SETs have amplitudes and widths that are less than the threshold values for propagation, the part may be placed in the non-critical category. A limited accelerator test using ions that produce the worst case ASETs

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may be performed. If some of the measured transients have amplitudes and widths greater than the thresholds for propagation, the design engineer should be consulted to determine whether the propagation requirements on ΔV_{th} and/or Δt_{th} can be modified.

If the follow-on circuit cannot be modified to be tolerant of SETs, a scan of all the transistors using the pulsed laser should be performed for the same configuration as for the heavy-ion data. The laser and ion data for the original configuration are then combined in a single plot of ΔV versus Δt and compared with a similar plot for the new configuration. If the loci of $(\Delta V, \Delta t)$ points are different for the two configurations, the laser cannot be used, and a complete heavy ion test must be done to fully characterize the part. However, if the same transistors in both configurations are responsible for the $(\Delta V, \Delta t)$ points located beyond the minimum values for propagation, the pulsed laser can be used to obtain a rough measure of LET threshold and cross-section for the new configuration.

The threshold is determined by calibrating the laser energy needed to produce an ASET in the new configuration against that in the old configuration. This is done by placing the laser light on the transistor responsible for the $(\Delta V, \Delta t)$ points just outside the box in the old configuration and measuring the energy to produce that point. Then the device is placed in the new configuration and the energy measured at that same transistor to produce a $(\Delta V, \Delta t)$ point just outside the box. Since the ion LET threshold for the old configuration is known, it can be calculated in the new configuration by taking the ratio of the laser energies and multiplying by LET_{th} in the old configuration.

The saturated cross-section is easily measured by using the laser with high pulse energy to determine the sensitive area associated with every transistor that produces SETs that will propagate. Summing all those areas will give a measure of the saturated SET cross-section applicable to that particular application. Previous results have demonstrated that this approach works. [Koga93]

The availability of linear devices hardened to the effects of ASETs would be of great interest to the aerospace industry. This could not be accomplished without implementing a RHA program as described above, but the two main obstacles include the multitude of configurations in which op-amps are operated and the relatively small aerospace market that does not serve as an incentive to IC manufacturers. An alternate approach to a full-blown RHA program is to use the pulsed laser in a judicious manner to screen parts for specific applications, as described above. This approach is currently being used by NASA programs.

10.0 ASET Mitigation

Most linear ICs are Commercial-off-the-Shelf (COTS) parts that are manufactured without regard to performance degradation by radiation. A few manufacturers do produce linear ICs that are designated "radiation hard" or "radiation tolerant," but those designations usually refer to the effects of total ionizing dose and not to ASETs. There are a few linear ICs available that incorporate hardening methods to reduce the effects of transients. Options for ASET mitigation include modifications to the device, the circuit and the system.

10.1 ASET Mitigation at the Device Level

Hardening linear parts to ASETs at the device and circuit levels is the responsibility of circuit designers and manufacturers. This is seldom done because of the very limited market for space applications. There are two generally accepted ways of suppressing ASETs at the device level. The first is to increase the critical charge, Q_{crit}. This approach has proved successful in SEU-hardened SRAMs, which incorporate resistors, capacitors or additional transistors in the feedback loop. In linear devices, increasing the size of a transistor and raising the supply voltage are two options. These modifications come with penalties of increased circuit size and increased

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power. The second is to reduce the amount of collected charge, because Q_{col} is what ultimately causes the ASET. The widely accepted method for reducing Q_{col} is to build the device in a very thin epitaxial silicon layer, such as silicon-on-insulator (SOI). The reduction in the collected charge will result in small ASETs with narrow widths. An example of a linear device manufactured in SOI is the LMH6624, an ultra low noise wideband (1.5 *GHz*) operational amplifier. **Fig. 71** is an example of the type of ASET produced in the LMH6624 with a pulsed laser. Initial screening was done with a pulsed laser that showed ASETs with amplitudes no greater than 0.3 *V* and widths of the order of 10 ns when the maximum laser energy was used. A similar device, the LMH6702, was tested with heavy ions. At the highest LET of 96 MeV·cm^2/mg, the largest ASETs had amplitudes of less than 400 *mV* and durations of approximately 20 *ns*. Depending on the application, these ASETs may or may not be of consequence.
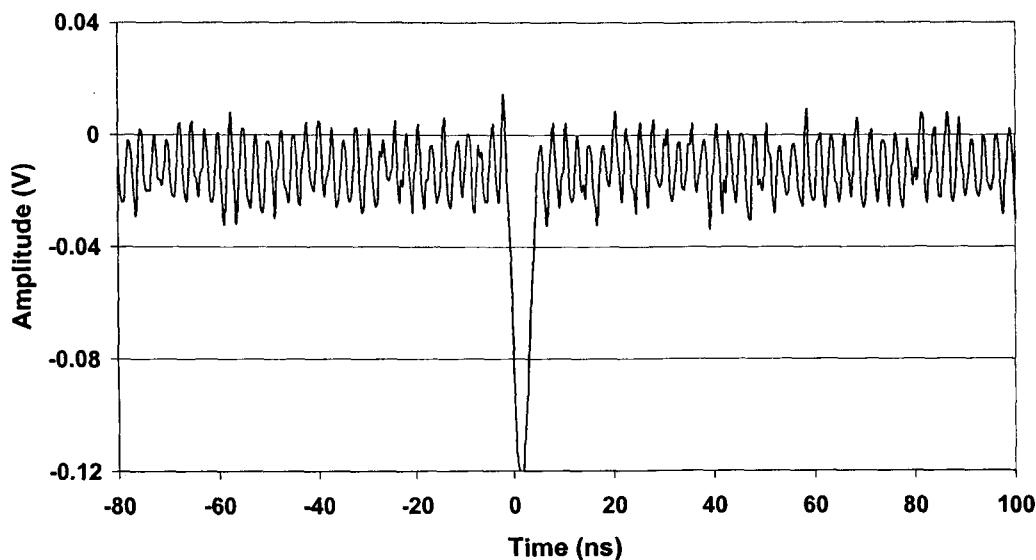

Fig. 71. ASET produced by pulsed laser light in the LMH6624 op-amp. The ASET has a small amplitude (<120 mV) and a short duration (5 ns).

10.2 ASET Mitigation at the Circuit Level

An effective way of reducing ASET sensitivity is to reduce the linear device's bandwidth so that all the fast transients are suppressed. An example of this approach was discussed in Section 8.1.2.1.

Another possible circuit level hardening approach is to use triple modular redundancy (TMR). This approach was adopted for the IS-139ASRH, a hardened version of the widely used LM139 comparator [VA01]. The part was designed and manufactured using a triply redundant architecture, in which a single comparator was replaced with three parallel comparators. The three comparator outputs drive a CMOS voting logic block that has been hardened to single event transients by using oversized transistors. **Fig. 72** shows a functional block diagram of the ASET hardened comparator.

The principle behind this hardening approach is that the majority voting logic produces an output that equals the state of two out of the three parallel comparators. If there is an ASET on one of the comparators, the two other comparators will be unaffected and the output will remain valid. The only way to get an erroneous output is for ASETs to be generated simultaneously in two of the parallel comparators. This is a highly unlikely scenario because of the low particle flux, but the probability is not zero. An ion traveling just below the semiconductor surface could

pass through ASET sensitive volumes in two adjacent comparators. In that case, two of the inputs to the voting logic would be in error, and that would result in an ASET at the output.
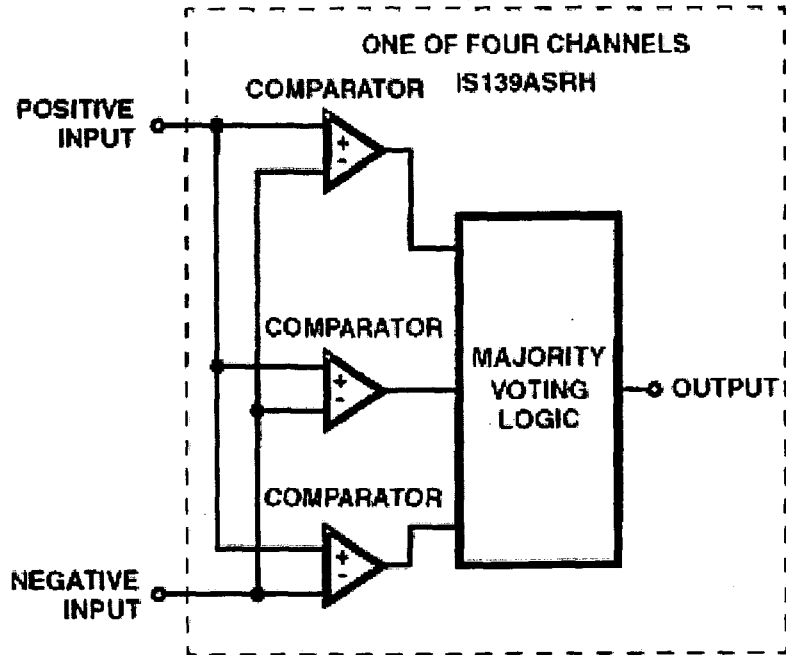

Fig. 72. Functional block diagram of the ASET-hardened IS-139ASRH voltage comparator [VA01].

To eliminate the possibility that an ion strike to a voltage reference would simultaneously affect all three redundant comparators, separate voltage references were used for each. Replacing one comparator with three parallel redundant comparators has penalties, including an increase of 60% in the size of the silicon chip and a 50% increase in power.

Heavy-ion testing showed that, as long as the input overdrive voltage (ΔV_{in}) was relatively large (~1V), the comparator operated as designed, i.e., no ASETs were observed for heavy-ion irradiation up to LET = 83.9 MeV·cm^2/mg. However, when the overdrive voltage was reduced to the point where it became comparable to the input offset voltage (5 mV), ASETs would be generated. The maximum overdrive voltage at which ASETs occurred was 5.8 mV, which is 0.8 mV above the input offset voltage. The explanation for this failure is given in term of the presence of input capacitance and resistance. An ion strike to an input diode on the IS-139ASRH caused a voltage transient that induced a voltage drop across the input resistor. All the inputs to the redundant comparators are connected together, so that a voltage transient on the input resistor propagates to all three inputs. The result is an ASET on the output. The magnitude of the overdrive at which ASETs no longer occur depends on both the input resistance and capacitance. **Fig. 73** shows how the minimum input overdrive for ASET-free operation as a function of input resistance for various values of input capacitance.
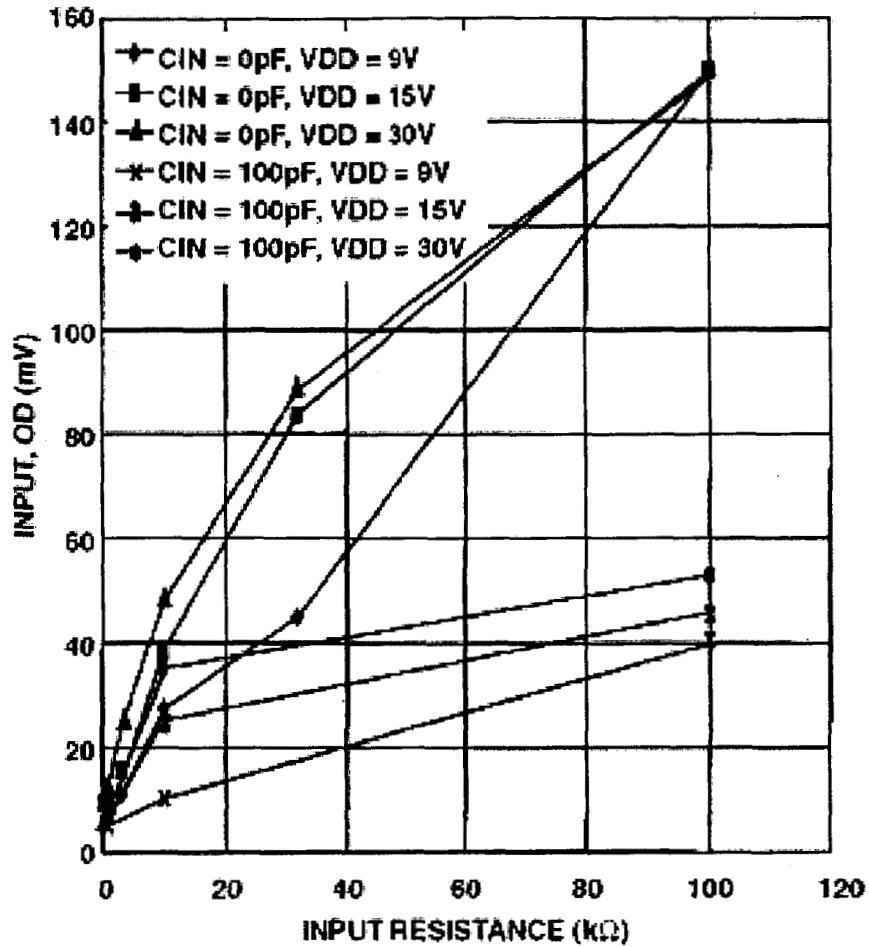
Fig. 73. Minimum input overdrive (ΔV_{in}) for SET-free operations as a function of input resistance, input capacitance, and supply voltage using Kr ions with an LET of 38 MeV·cm^2/mg [VA01].

10.3 ASET Mitigation at the System Level

System mitigation can be very effective at reducing ASETs. A common approach is to add a low bandpass filter to suppress the propagation of fast ASETs. The value of the bandpass filter is set by system bandwidth. An example of an actual exercise in hardening is presented below.

Fig. 74 shows a circuit designed for controlling and monitoring the power distribution inside a spacecraft [BO03]. The part is designed to prevent a battery on board a spacecraft from being overcharged or undercharged. Analysis of the system as a whole has determined that a system failure will occur if an ASET appears at the circuit output (Output 3) with an amplitude that exceeds 1.8 V for more than 3 μs.
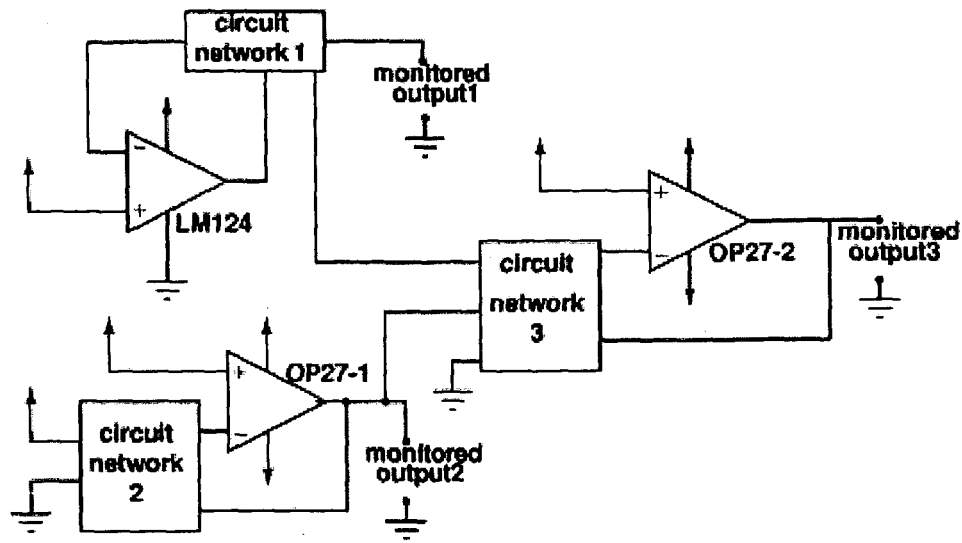
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Fig. 74. Simplified circuit schematic of a specific application that contains two OP27's and one LM124 [BO04A]. For proprietary reasons the remaining circuits are treated as black boxes.

Because of proprietary reasons, the details of the circuit were not revealed and were treated as "black boxes." The individual operational amplifiers were exposed to heavy ions and the ASETs produced were sampled at three different locations in the system. To validate the accuracy of the models used for computer simulation, "worst-case" ASETs were calculated both at the output of the IC being irradiated and at the system output (Output 3) and then compared with the actual ASETs obtained experimentally. Given that the LM124 and the OP-27 had been extensively modeled previously, it was not surprising that excellent agreement between pulse shapes was obtained. In fact this approach only works if the models have been validated by comparison with ASETs produced by heavy ions or pulsed-laser light.

Once the model for the whole circuit had been instantiated, ways of hardening the system were investigated. The restriction was that no new components could be added and the DC bias levels could not be changed. The first attempt at circuit hardening was to reduce the value of a resistor in "circuit network 1" from 1 kΩ to 100 Ω. The reduction in resistance strongly attenuated negative ASETs but not positive ones. Conversely, a reduction by an order of magnitude in the value of a resistor in "circuit network 2" attenuated positive ASETs but not negative ASETs. Finally, the values of two resistors in "circuit network 3" were reduced by a factor of five while keeping their ratio constant. The two resistors were in the feedback loop and a reduction in their values but not their ratio maintained a constant gain. This change was the most successful because both the positive and negative pulses were attenuated. Again, as for the case of the IS-138ASRH, changing the resistors came with a penalty – a factor of 3.5 increase in power consumption. This analysis shows how a combination of computer simulation, heavy-ion experiments and pulsed-laser experiments were used to harden a system to ASETs.

10.4 Explanation of ASETs on MAP

Now that the various factors affecting ASET sensitivity have been covered, it is possible to appreciate the analysis undertaken by NASA radiation effects engineers to identify the exact cause of the processor reset on board MAP.

Fig. 75 shows the reset circuit used on MAP. It consists of three LM139 voltage comparators. The voltage being monitored is the 5-V supply connected through a 3.6 kΩ resistor to the inputs of comparators #1 and #2. Because of the voltage drop across the 3.6 kΩ resistor, the voltage applied to the positive inputs of the two comparators is 2.9 V. With a reference voltage of

2.5 V, the differential input voltage is 400 mV. Since the voltages applied to the positive inputs of all three comparators are greater than to the negative inputs, the outputs of all three comparators are at 5 V. The outputs of comparator #1 and #3 are connected through a series of inverters to the reset pin of the processor. If the output voltage of either comparator #1 or #3 drops below 2.5 V, the processor resets.
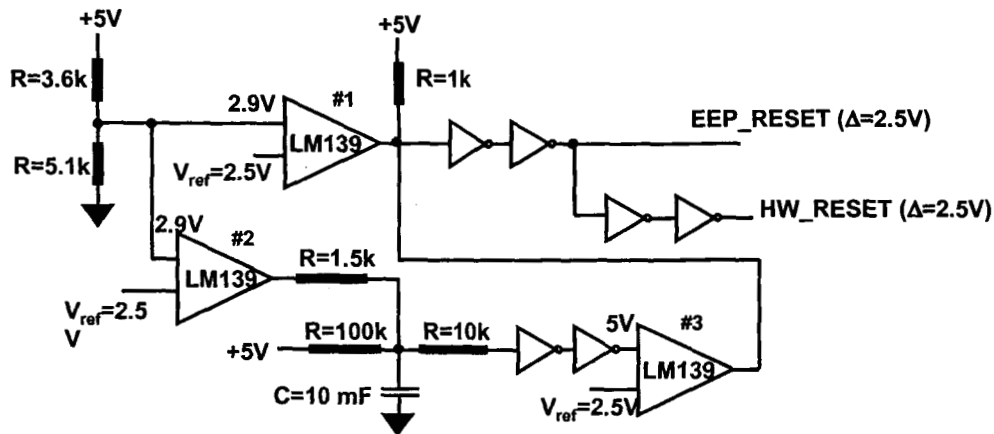

Fig. 75. Schematic of the reset circuit used on MAP [PO02].

Ground testing of the LM139 showed that the cross-section threshold shifts to higher LETs as the differential input voltage increases, and that for ΔV_{in} = 2.5 V the threshold is much greater than for ΔV_{in} = 400 mV. The saturated cross-section is also reduced for the higher differential input voltage. In addition, the data show that for a differential input voltage of 800 mV, many of the ASETs induced by ions having LET of 18.7 MeV.cm^2/mg have amplitudes as large as 10 V, which is more than sufficient to trigger the processor reset circuit.

Two out of the three comparators have some form of ASET mitigation. There is a low-pass filter on the output of comparator #2 and the differential input voltage for comparator #3 is 2.5 V. Both of these conditions lead to a reduction in the ASET sensitivity. In contrast, there is no filter on the output of comparator #1 and the differential input voltage is only 400 mV. Therefore, comparator #1 is the most sensitive to ASETs and is the cause of the two resets observed on MAP so far.

11.0 Summary and Conclusions

The purpose of this monograph is to discuss various aspects of ASETs in order to heighten the reader's awareness of the issues involved. To recapitulate, ASETs occur in all types of analog circuits and may take many different forms, from simple glitches to lost pulses. The best way to study ASETs is to use a combination of circuit simulation and experimental measurements that include broad-beam heavy-ion testing, focused ion beam testing and pulsed laser testing. Although circuit simulation requires a massive amount of work to obtain circuit parameters, the rewards are great because it is straight-forward to investigate factors affecting ASETs that cannot easily be studied experimentally. Broad-beam testing is necessary to obtain the ASET cross-section as a function of ion LET, but merely counting the number of ASETs is not adequate - an analysis of the waveforms is necessary to determine which transients actually pose a threat to a system. Only those that pose a threat should be included when calculating cross-section. The pulsed laser has proved to be a very useful technique for studying ASETs because of the spatial and temporal information it provides. Two-photon absorption makes it possible to measure ASETs by directing the light from the backside, a novel approach that is still in its infancy. Although ASETs are a potential threat to a system, there are ways to mitigate their deleterious effects.

Finally, when designing a space system it is imperative to ensure that all linear devices are checked for ASETs. Failure to do so could cause a serious unwanted spacecraft anomaly that would jeopardize the mission's success. The continued publication of papers concerning ASETs helps to widen out understanding, which is a good omen for the future.

12.0 Acknowledgements

13.0 References

[AD00] P. Adell, R. D. Schrimpf, H. J. Barnaby, R. Marec, C. Chatry, P. Calvel, C. Barillot, and O. Mion, "Analysis of Single Event Transients in Analog Circuits," *IEEE Trans. On Nucl. Sci.*, vol. 47, n°6, pp. 2616-2623, Dec. 2000.

[BA97] J. Barth, " Modeling Space Radiation Environments," 1997 IEEE NSREC short course.

[BE83] W. L. Bendel and E. L. Petersen, "Proton upsets in orbit", " IEEE Trans. Nucl. Sci., vol. 30, No. 6, pp. 4481-4485, Dec. 1983.

[BO02] Y. Boulghassoul, L.W. Massengill, A.L. Sternberg, R.L. Pease, S. Buchner, J.W. Howard, D. McMorrow, M.W. Savage, C. Poivey, "Circuit Modeling of the LM124 Operational Amplifier for Analog Single-Event Transient Analysis," *IEEE Trans. On Nucl. Sci.*, vol. 49, n°6, Dec. 2002.

[BO02a] Y. Boulghassoul, L.W. Massengill, T.L. Turflinger, and W.T. Holman, "Frequency Domain Analysis of Analog Single-Event Transients in Linear Circuits," IEEE Trans. Nucl. Sci., vol. 49, No. 6, pp. 3142-3147, Dec. 2002.

[BO03] Y. Boulghassoul, J. D. Rowe and L. W. Massengill, "Applicability of Circuit Macromodeling to Analog Single-Event Transient Analysis," IEEE Trans. Nucl. Sci., vol. 50, pp 2119 -2125, Dec 2003.

[BO04] Y. Boulghassoul, P. Adell, J. D. Rowe, L.W. Massengill, R.D. Schrimpf and A. L. Sternberg, "System-Level Design Hardening Based on Worst-Case ASET Simulations," IEEE Trans. Nucl. Sci., vol. 51, pp 2787 -2793, Oct. 2004.

[BO04a] Y. Boulghassoul, S. Buchner, D. McMorrow, V. Pouget, L.W. Massengill, P. Fouillat, W.T. Holman, C. Poivey, J.W. Howard, M. Savage and M.C. Maher, "Investigation of Millisecond-Long Analog Single-Event Transients in the LM6144 Op Amp," IEEE Trans. Nucl. Sci., vol. 51, pp. 3529-3536, Dec. 2004.

[BU87] S. Buchner, D. Wilson, K. Kang, D. Gill, J.A. Mazer, W.D. Raburn, A.B. Campbell, and A.R. Knudson, "Pulsed-Laser Induced SEU in Integrated Circuits: A Practical Method for Hardness Assurance Testing", IEEE Trans. Nuc. Sci., vol. 37, pp. 1825-1831, Dec. 1990.

[BU90] S. Buchner, K. Kang, W.J. Stapor, A.B. Campbell, A.R. Knudson, and P.T. McDonold, "Laser Simulation of Single Event Upsets", IEEE Trans. Nuc. Sci., vol. 34, pp. 1288-1233, Dec. 1987.

[BU96] S. Buchner, D. McMorrow, J. Melinger, A.B. Campbell, "Laboratory Tests for Single Event Effects," IEEE Trans. On Nucl. Sci., vol. 43, n°2, pp. 678-686, Apr. 1996.

[BU97] S. Buchner, M. Baze, D. Brown, D. McMorrow, and J. Melinger, "Comparison of Error Rates in Combinational and Sequential Logic", IEEE Trans. Nuc. Sci., vol. 44, pp. 2209-2216, Dec. 1997.

[BU01] S. Buchner, D. McMorrow, A. Sternberg, L. Massengill, R.L. Pease, M. Maher, "Single Event Transient (SET) Characterization of a LM119 Voltage Comparator: An

Approach to SET Model Validation Using a Pulsed Laser," RADECS 2001 Proceedings, 2001.

[BU01a] S. Buchner and M. Baze, "Single Event Transients in Fast Electronic Circuits" IEEE NSREC Short Course, Vancouver BC 2001.

[BU04] S. Buchner, J. Howard, C. Poivey, D. McMorrow, and R. Pease, "Pulsed-Laser Testing Methodology for Single Event Transients in Linear Devices," IEEE Trans. Nucl. Sci., vol. 51, No. 6, pp. 3716-3722, Dec. 2004.

[BU04a] S. Buchner, D. McMorrow, C. Poivey, J. W. Howard, Jr., R. L. Pease, M. Savage, L. W. Massengill and Y. Boulghassoul, "Comparison of Single-Event Transients in an Operational Amplifier (LM124) by Pulsed Laser Light and a Broad Beam of Heavy Ions", IEEE Trans. Nucl. Sci., vol. 51, No. 5, pp 2776-2781, Oct. 2004.

[CH02] A.M. Chugg, R. Jones, M.J. Moutrie, C.S. Dyer, C. Sanderson, and A Wraight, "Probing the Charge Collection Sensitivity Profile using a Picosecond Pulsed Laser at a Range of Wavelengths", IEEE Trans. Nucl. Sci. vol. 49 No.6, pp. 2969-2976, Dec. 2002.

[CR01] S.H Crain, J.E Mazur, R.B Katz, R. Koga, M.D. Looper, "Analog and Digital Single-Event Effects Experiments in Space," IEEE Trans. Nucl. Sci. vol. 48 No.6, pp. 1841-1848, Dec. 2001.

[CH03] W. Chen, V. Pouget, H. Barnaby, J. Cressler, G. Niu, P. Fouillat, Y. Deval, and D. Lewis, "Investigation of Single-Event Transients in Voltage-Controlled Oscillators," IEEE Trans. Nucl. Sci. vol. 50, No. 6, pp. 2081-2087, Dec. 2003.

[DA02] F. Darracq, H. Lapuyade, N. Buard, F. Mounsi, B. Foucher, P. Fouillat, M.C. Calvet, and R. Dufayel, Backside SEU Laser Testing for Commercial Off-The-Shelf SRAMs", IEEE Trans. on Nucl. Sci., vol. 49, no. 6, pp. 2977-2983, Dec. 2002.

[DU95] H. Dussault, J.W. Howard, R.C. Block, W.J. Stapor, A.R. Knudson, P.T. McDonald, and M.R. Pinto, "High-Energy Heavy-Ion-Induced Charge Transport Across Multiple Junctions," IEEE Trans. Nucl. Sci. vol. 42, pp-1780-1788, Dec. 1995.

[EC94] R. Ecoffet, S. Duzellier, P. Tastet, C. Aicardi, M. Labrunee, "Observation of Heavy Ion Induced Transients in Linear Circuits," *IEEE NSREC 94 Data Workshop Proceedings*, pp. 72-77, 1994.

[HA99] R. Harboe-Sorensen, F.X. Guerre, H. Constans, J. Van Dooren, G. Berger, and W. Hajdas, "Single Event Transient Characterization of Analog IC's for ESA's Satellites," *1999 Fifth European Conference on Radiation and Its Effects on Components and Systems (RADECS) Proceedings*, IEEE, Piscataway, NJ, pp. 573-581, 2000.

[HA01] R. Harboe-Sorensen, E. Daly, F. Teston, H. Schweitzer, R. Nartallo, P. Perol, F. Vandenbussche, H. Dzitko, and J. Cretolle, "Observations and Analysis of Single Event Effects On-board the SOHO Satellite," RADECS 2001 proceedings, 2001.

[HO03] J. Howard, Martin Carts, Kenneth LaBel, James Forney and Timothy Irwin, "Single Event Effects Testing of the Linfinity SG1525A Pulse Width Modulator Controller," 2003 IEEE Radiation Effects Data Workshop, pp. 133-140, Monterey CA., 2003.

[HTTP] http://www.st-andrews.ac.uk/~www_pa/Scots_Guide/audio/part8/Page1.html

[JO00] A.H. Johnston, G.M. Swift, T.F. Miyahira, L.D. Edmonds, " A model for Single Event Transients in Comparators," IEEE Trans. On Nucl. Sci., vol. 47, n°6, pp. 2624-2633, Dec. 2000.

[JO00a] R. Jones, A.M. Chugg, C.M.S. Jones, P.H. Duncan, C.S. Dyer, and C. Sanderson, "Comparison between SRAM SEE cross-sections from ion beam testing with those obtained using a new picosecond pulsed laser facility", IEEE Trans. Nucl. Sci. vol. 47 No.6, pp. 539-544, Dec. 2000.

[JO02] A.H. Johnston, T.F. Miyahira, L.D. Edmonds and F. Irom, "Single-Event Transients in High-Speed Comparators," IEEE Trans. on Nucl. Sci., vol. 49, no. 6, pp. 3082-3089, Dec. 2002.

[KN90]   Glenn. F. Knoll, "Radiation Detection and Measurement," pp. 32-33, John Wiley & Sons, 1989

[KO93]   R. Koga, S. D. Pinkerton, S. C. Moss, D. C. Mayer, S. Lalumondiere, S. J. Hansel, K. B. Crawford, W. R. Crain, "Observation of Single Event Upsets in Analog Microcircuits," IEEE Trans. On Nucl. Sci., vol. 40, No. 6, pp. 1838-1844, Dec. 1993.

[KO97]   R. Koga, S. H. Penzin, K.B. Crawford, W. R. Crain, S. C. Moss, S. D. Pinkerton, S. D. LaLumondiere, M. C. Maher, "Single Event Upset (SEU) Sensitivity Dependence of Linear Integrated Circuits (ICs) on Bias Conditions," IEEE Trans. On Nucl. Sci., vol. 44, No. 6, pp. 2325-2332, Dec. 1997.

[KO00]   R. Koga, S.H. Crain, K.B. Crawford, S.C. Moss, S.D. Lalumondiere, J.W. Howard, " Single Event Transient (SET) Sensitivity of Radiation Hardened and COTS Voltage Comparators," IEEE NSREC 2000 Data Workshop Proceedings, pp. 53-60, 2000.

[LA03]   R. Ladbury, H. Kim, "Heavy-Ion Latch-up and Transient and Laser Transient Test Results for the Analog Devices OP293 Operational Amplifier," NASA-GSFC test report, April 22, 2003.

[LA02]   Stephen D. LaLumondiere, Rocky Koga, Paul Yu, Michael C. Maher, and Steven C. Moss, "Laser-Induced and Heavy Ion-Induced Single-Event Transient (SET) Sensitivity Measurements on 139-Type Comparators," IEEE Trans. Nucl. Sci., vol. 49, No. 6, pp. 3121-3128, Dec. 2002.

[LE01]   D. Lewis, V. Pouget, F. Beaudoin, P. Perdu, H. Lapuyade, P. Fouillat, and A. Touboul, "Backside laser testing of ICs for SET sensitivity evaluation", IEEE Trans. Nuc. Sci., vol. 48, pp. 2193-2201, Dec. 2001.

[MA99]   P W Marshall and C J Marshall, "Proton Effects and Test Issues for Satellite Designers," IEEE NSREC Short Course Notes, Norfolk, VA, 1999.

[MA01]   R. Marec, C. Chatry, P. Adell, O. Mion, C. Barillot, P. Calvel, L. Cresciucci, "Towards a Single Event Transient Hardness Assurance Methodology," RADECS 2001 Proceedings, 2001.

[MC94]   D. McMorrow, J.S. Melinger, N. Thantu, A.B. Campbell, T.R. Weatherford, A.R. Knudson, L.H. Tran, and A. Peczalski, "Charge-Collection Mechanchisms of Heterostructure FETs", IEEE Trans. Nuc. Sci., NS-41, 2055 (1994).

[ME94]   J.S. Melinger, S. Buchner, D. McMorrow, W.J. Stapor, T.R. Weatherford, A.B. Campbell, H. Eisen, "Critical Evaluation of the Pulsed Laser Method for Single Event Effects Testing and Fundamental Studies," IEEE Trans. On Nucl. Sci., vol. 41, No. 6, pp. 2574-2584, Dec. 1994.

[MC00]   D. McMorrow, J.S. Melinger, S. Buchner, T. Scott, R.D. Brown, and N.F. Haddad, "Application of Pulsed Laser for Evaluation and Optimization of SEU-Hard Designs", IEEE Trans. Nuc. Sci., NS-47, pp. 559-565, Dec 2000.

[MC02]   D. McMorrow, W.T. Lotshaw, J.S. Melinger, S. Buchner, R. Pease, "Subbandgap Laser-Induced Single Event Effects: Carrier Generation via Two-Photon Absorption," IEEE Trans. On Nucl. Sci., vol. 49, No. 6, pp. 3002-3008, Dec. 2002.

[MC03]   Dale McMorrow, William Lotschaw, Joseph Melinger, Stephen Buchner, Younes Boulghassoul, Lloyd W. Massengill, and Ronald L. Pease, "Three-Dimensional Mapping of Single-Event Effects Using Two Photon Absorption," IEEE Trans. Nucl. Sci., vol. 50, No. 6, pp. 2199-2207, Dec. 2003.

[MC04]   D.McMorrow, S. Buchner, W.T. Lotshaw, J.S. Melinger, M. Maher, and Mark W. Savage, "Demonstration of Single-Event Effects Induced by Through-Wafer, Two-Photon Absorption", IEEE Trans. on Nuc. Sci., vol. 51, pp. 3553-3557, Dec. 2004.

[MC05]   Dale McMorrow, William T. Lotshaw, Joseph S. Melinger, Stephen Buchner, John D. Davis, Reed K. Lawrence, Nadim Haddad, James H. Bowman, Ron D. Brown Dave Carlton, Joseph Pena, Juan Vasquez, Kevin Warren, and Lloyd Massengill, "Single-Event Upset in Flip-Chip SRAM Induced by Through-Wafer, Two-Photon

Absorption", presented at NSREC 2005; IEEE Trans. Nucl. Sci., vol. 52, Dec. 2003, *submitted for publication.*

[MI04] F. Miller, A. Germain, N. Buard, R. Gaillard, P. Poirot, C. Chatry, T. Carriere, and R. Dufayel, "Interest of laser test facility for the assessment of natural radiation environment effects on integrated circuits based systems", *Proceedings of the 7th European Conference on Radiation and its Effects on Components and Systems, RADECS 2003*, ESA Publications Division, Noordwijk, pp. 199-210, 2004.

[MI04a] F. Miller, N. Buard, T. Carriere, R. Dufayel, R. Gaillard, P. Poirot, J.M. Palau, B. Sagnes, and P. Fouillat, "Effects of Beam Spot Size on the Correlation Between Laser and Heavy Ion SEU Testing", IEEE Trans. Nucl. Sci., vol. 51, pp. 3708-3715, Dec. 2005.

[MO95] S.C. Moss, S.D. LaLumondiere, J.R. Scarpulla, K.P. MacWilliams, W.R. Crain, and R. Koga, "Correlation of Picosecond Laser-Induced Latchup and Energetic Particle-Induced Latchup in CMOS Test Structures", IEEE Trans. Nuc. Science 42, pp. 1948-1955, Dec. 1995.

[NI96] D. K. Nichols, J.R. Coss, T.F. Miyahira, H.R. Schwartz, "Heavy Ion and Proton Induced Single Event Transients in Comparators," IEEE Trans. On Nucl. Sci., vol. 43, No.6, pp. 2960-2967, Dec. 1996.

[PE01] R. Pease, A. Sternberg, L. Massengill, R. Schrimpf, S. Buchner, M. Savage, J. Titus, T. Turflinger, "Critical Charge for Single-Event Transients (SETs) in Bipolar Linear Circuits," IEEE Trans. On Nucl. Sci., vol. 48, No. 6, pp. 1966-1972, Dec. 2001.

[PE02] R. Pease, A. Sternberg, Y. Boulghassoul, L. Massengill, S. Buchner, D. McMorrow, D. Walsh, G. Hash, S. Lalumondiere, and S. Moss, "Comparison of SETs in Bipolar Linear Circuits Generated with an Ion Microbeam, Laser Light and Circuit Simulation," IEEE Trans. On Nucl. Sci., vol. 49, No. 6, Dec. 2002.

[PE04] R. L. Pease, L. Massengill, Y. Boulghassoul, A. Sternberg, S. Buchner, C. Poivey, D. McMorrow and M. Savage, "Hardness assurance methodology for analog single event transients", submitted to the Journal of Radiation Effects Research and Engineering, 2004.

[PE04A] R. L. Pease, "Hardness assurance for commercial microelectronics", International Journal of High Speed Electronics and Systems, Vol. 14, No. 2 pp. 543-561, 2004.

[PE98] E. L. Petersen, "The SEU figure of merit and proton upset rate calculations", IEEE Trans. Nucl. Sci., vol. 45, No. 6, pp. 2550-2562, Dec. 1998.

[PN96] S.H. Penzin, W.R. Crain, K.B. Crawford, S.J. Hansel, J.F. Kirshman, R. Koga, "Single Event Effects in Pulse Width Modulation Controllers," *IEEE Trans. On Nucl. Sci.*, vol. 43, n°6, pp. 2968-2973, Dec. 1996.

[PO99] V. Pouget, D. Lewis, H. Lapuyade, R. Briand, P. Fouillat, L. Sarger, and M.C. Calvet, "Validation of Radiation Hardened Designs by Pulsed Laser Testing and SPICE Analysis", Microelectron. Reliab., vol. 39, pp 931-935, 1995.

[PO02] C. Poivey, J. Barth, J. McCabe, and K. LaBel, "A Space Weather Event on the Microwave Anisotropy Probe (MAP)," Presented at RADECS 2002.

[PO03] C. Poivey, S. Buchner, J. Howard and K. LaBel, "Testing and Hardness Assurance Guidelines for Single Event Transients (SETs) in Linear Devices," NASA GSFC, 30th June, 2003.

[PR02] B. E. Pritchard, G. M. Swift, A. H. Johnston, "Radiation Effects Predicted, Observed, and Compared for Spacecraft Systems," *IEEE NSREC 2002 Data Workshop Proceedings*, pp. 7-17, 2002.

[SA01] M.W. Savage, T. Turflinger, J.W. Howard, S. Buchner, "A Compendium of Single Event Transient Data," *IEEE NSREC 2001 Data Workshop Proceedings*, pp. 134-141, 2001.

[SA02]   M.W. Savage, "Heavy Ion Analog SET Test of LM111 and LM124," NAVSEA CRANE test report, Oct. 2002.

[SA04]   Mark W. Savage, Jeffrey L. Titus, Thomas L. Turflinger, Ronald L. Pease and Christian Poivey, "A Comprehensive Analog Single-Event Transient Analysis Methodology," IEEE Trans. Nucl. Sci., vol. 51, No. 6, pp. 3546-3552, Dec. 2004.

[SC81]   P.E. Schmid, "Optical Absorption in Heavily Doped Silicon", Phys. Rev. B, vol. 23, pp. 5531-5536, 1981.

[SE92]   F.W. Sexton, "Measurement of Single Event Phenomena in Devices and ICs," IEEE NSREC Short Course, New Orleans, LA 13th July, 1992.

[SE96]   F.W. Sexton, "Microbeam Studies of Single-Event Effects," IEEE Trans. Nucl. Sci. vol. 43, No.2, pp. 687-694, April, 1996.

[ST01]   A.L. Sternberg, L.W. Massengill, R.D. Schrimpf and P. Calvel, "Application Determinance of Single-Event Transient Characteristics in the LM111 Comparator," IEEE Trans. Nucl. Sci., vol. 48, No. 6, pp. 1855-1858 Dec. 2001.

[ST02]   A.L. Sternberg, L.W. Massengill, S. Buchner, R.L. Pease, Y. Boulghassoul, M. Savage, D. McMorrow, R.A. Weller, "The Role of Parasitic Elements in the Single-Event Transient Response of Linear Circuits," IEEE Trans. On Nucl. Sci., vol. 49, No. 6, pp. 3115-3120 Dec. 2002.

[ST02A] A.L. Sternberg, L.W. Massengill, R.D. Schrimpf, Y. Boulghassoul, H.J. Barnaby, S. Buchner, R.L. Pease, and J.W. Howard, "Effect of Amplifier Parameters on Single-Event Transients in an Inverting Operational Amplifier," IEEE Trans. Nucl. Sci., vol. 49, pp. 1496-1501, June 2002.

[VA01]   Nicolaas W. van Vonno and Brent R. Doyle, "Design Considerations and Verification Testing of an SEE-Hardened Quad Comparator," IEEE Trans. Nucl. Sci., vol. 48 No. 6, pp. 1859-1863, Dec. 2001.

[XA92]   M.A. Xapsos, "Applicability of LET to Single Events in Microelectronic Structures," IEEE Trans. Nucl. Sci. VOL. 13, PP. 1613-1621, Dec. 1992.