Recent Single Event Effects Results for Candidate Spacecraft Electronics for NASA

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***Abstract*—Vulnerability of a variety of candidate spacecraft electronics to proton and heavy ion induced single event effects is studied. Devices tested include digital, linear bipolar, and hybrid devices.**

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***Index Terms*—Single Event Effects, spacecraft electronics, digital, linear bipolar, and hybrid devices.**

I. Introduction

As spacecraft designers use increasing numbers of commercial and emerging technology devices to meet stringent performance, as well as economic budgets and schedule requirements, ground-based testing of such devices for susceptibility to single event effects (SEE) has assumed ever greater importance.

The studies discussed here were undertaken to establish the sensitivities of candidate spacecraft electronics to heavy ion and proton-induced single event upsets (SEU), single event latchup (SEL), and single event transient (SET). Note: For proton displacement damage (DD) and total ionizing dose (TID) results see a companion paper entitled "Recent Total Ionizing Dose and Displacement Damage Results for Candidate Spacecraft Electronics for NASA" by Cochran, et al. that is also being submitted to IEEE NSREC [1].

II. Test Techniques and Setup

A. Test Facilities

All SEE tests were performed between February 2004 and February 2005. Heavy Ion experiments were conducted at the Brookhaven National Laboratories' (BNL) Single Event Upset Test Facility (SEUTF) [2], at Texas A&M University Cyclotron (TAMU) [3], and at the Single-Event Effects Test Facility (SEETF) at the National Superconducting Cyclotron Laboratory (NSCL) at Michigan State University (MSU) [4]. The BNL SEUTF uses a twin Tandem Van De Graaf accelerator while the TAMU facility uses an 88" Cyclotron. The NSCL MSU facility uses tandem K500 and K1200 cyclotrons to deliver on target ions with energies up to 125 MeV/n. All three facilities are suitable for providing a variety of ions over a range of energies for testing. At all facilities, test boards containing the device under test (DUT) were mounted in the test area. For heavy ions, the DUT was irradiated with ions with linear energy transfers (LETs) ranging from 0.59 to 120 MeV•cm^2/mg. Fluxes ranged from 1x10^2 to 5x10^5 particles/cm^2 per second, depending on the device sensitivity. Representative ions used are listed in Table I. LETs between

the values listed were obtained by changing the angle of incidence of the ion beam on the DUT, thus changing the path length of the ion through the DUT and the "effective LET" of the ion [5]. Energies and LETs available varied slightly from one test date to another.

Proton SEE tests were performed at the Indiana University Cyclotron Facility (IUCF) [6]. Proton test energies incident on the DUT are listed in Table II. Proton SEE tests were performed in a manner similar to heavy ion exposures. However, because protons cause SEE via indirect ionization of recoil particles, results are parameterized in terms of proton energy rather than LET. Because such proton-induced nuclear interactions are rare, proton tests also feature higher cumulative fluence and particle flux rates than do heavy-ion experiments.

Laser SEE tests were performed at the pulsed laser facility at the Naval Research Laboratory (NRL) [7] [8]. The laser light had a wavelength of 590 nm resulting in a skin depth (depth at which the light intensity decreased to 1/e - or about 37% - of its intensity at the surface) of 2 μm. A nominal pulse rate of 100 Hz was utilized.

TABLE I: HEAVY ION TEST FACILITIES AND TEST HEAVY IONS

	Ion	Energy, MeV	Surface LET in Si, MeV•cm²/mg (Normal Incidence)	Range in Si, μm
BNL	Br^{79}	305	36.9	38.7
	I^{127}	321-370	59.7-60.1	31-34.3
TAMU	† Ne^{20}	266-270	2.7-2.8	261-267
	† Ar^{40}	496-497	8.7 - 9	174-175
	† Cu^{63}	944	17.8-21.5	172
	† Kr^{84}	912-916	25.4-29.3	116-170
	† Ag^{109}	1634	38.5-44.2	96.8-156
	† Xe^{129}	1215-1934	47.3-55.3	94.2-156
	† Au^{197}	1883-2247	53.9-85	100-155
	* Ne^{20}	545	1.7	799
	* Xe^{29}	3197	37.9	286
	‡ O^{16}	880	0.59	3607
	‡ Ar^{40}	1980	3.0	1665
	† 15 MeV per nucleon tune * 25 MeV per nucleon tune ‡ 55 MeV per nucleon tune			
MSU	Kr^{78}	9438	6.8	4440
	Xe^{124}	17360	14.1	~ 3300

TABLE II: PROTON TEST FACILITIES AND PARTICLES

Facility	Particle	Particle Energy, (MeV)
Indiana University Cyclotron Facility (IUCF)	Proton	54-197

TABLE III: OTHER TEST FACILITIES

Naval Research Laboratory (NRL) Pulsed Laser SEE Test Facility Laser: 590 nm, 1 ps pulse width, beam spot size ~1.2 μm

B. Test Method

Unless otherwise noted, all tests were performed at room temperature and with nominal power supply voltages.

1) SEE Testing - Heavy Ion:

Depending on the DUT and the test objectives, one or more of three SEE test methods were used:

Dynamic – the DUT was exercised continually while being exposed to the beam. The errors were counted, generally by comparing DUT output to an unirradiated reference device or other expected output. In some cases, the effects of clock speed or device modes were investigated. Results of such tests should be applied with caution because device modes and clock speed can affect SEE results.

Static – the DUT was loaded prior to irradiation; data were retrieved and errors were counted after irradiation.

Biased – the DUT was biased and clocked while I_{CC} (power consumption) was monitored for SEL or other destructive effects. In some SEL tests, functionality was also monitored.

In SEE experiments, DUTs were monitored for soft errors, such as SEUs and for hard errors, such as SEL. Detailed descriptions of the types of errors observed are noted in the individual test results. [9]

SET testing was performed using a high-speed oscilloscope. Individual criteria for SETs are specific to the device being tested. Please see the individual test reports for details. [9]

Heavy ion SEE sensitivity experiments include measurement of the saturation cross sections and the Linear Energy Transfer threshold (LET_{th}). The LET_{th} is defined as the maximum LET value at which no effect was observed at an effect fluence of $1x10^7$ particles/cm^2. In the case where events are observed at lower fluences for the smallest LET tested, LET_{th} will either be reported as less than the lowest measured LET or determined approximately as the LET_{th} parameter from a Weibull fit.

2) Pulsed Laser Facility Testing

The DUT was mounted on an X-Y-Z stage in front of a 100x lens that produced a spot size of about 1.2 μm full-width half-maximum (FWHM). The X-Y-Z stage could be moved in steps of 0.1 μm for accurate positioning of SEU sensitive regions in front of the focused beam. An illuminator together with a charge coupled device (CCD) camera and monitor were used to image the area of interest, thereby facilitating accurate positioning of the device in the beam. The pulse energy was varied in a continuous manner using a polarizer/half-waveplate combination and the energy was monitored by splitting off a portion of the beam and directing it at a calibrated energy meter.

III. Test Results Overview

Abbreviations for principal investigators (PIs) are listed in Table IV, SEE test result categories are summarized in Table V, abbreviations and conventions are listed in Table VI, Device Category Abbreviations are listed in Table VII, SEE results are summarized in Table VIII, and SE: results are featured in Table IX. Unless otherwise noted, all LETs are in MeV•cm^2/mg and all cross sections are in cm^2/device. This paper is a summary of results. Complete test reports are available online at http://radhome.gsfc.nasa.gov [9].

TABLE IV: LIST OF PRINCIPAL INVESTIGATORS

Principal Investigator (PI)	Abbreviation
Steve Buchner	SB
Jim Howard	JH
Scott Kniffin	SK
Ken LaBel	KL
Ray Ladbury	RL
Tim Oldham	TO
Christian Poivey	CP
Anthony (Tony) Sanders	TS

TABLE V: LIST OF CATEGORIES

Following ground SEE irradiation, devices generally are categorized into "useability" categories for spacecraft interest. Recommendations for SEE are color coded according to the following key:

Category 1:	Recommended for usage in all NASA/GSFC spaceflight applications
Category 2:	Recommended for usage in NASA/GSFC spaceflight applications, but may require mitigation techniques
Category 3:	Recommended for usage in some NASA/GSFC spaceflight applications, but requires extensive mitigation techniques or hard failure recovery mode (may require latent damage screening)
Category 4:	Not recommended for usage in any NASA/GSFC spaceflight applications
RTV:	Research Test Vehicle - Please contact the P.I. before utilizing this device for spaceflight applications

TABLE VI: ABBREVIATIONS AND CONVENTIONS:

H = heavy ion test
P = proton test (SEE)
L = laser test
LET = linear energy transfer (MeV•cm^2/mg)
LET_{th} = linear energy transfer threshold (the maximum LET value at which no effect was observed at an effective fluence of $1x10^7$ particles/cm^2)
SEE = single event effect
SEU = single event upset
SEL = single event latchup
SET = single event transient
SEFI = single event functional interrupt
SEB = single event burnout
SEGR = single event gate rupture
SES = - single event snapback
BERT = bit error rate test
< = SEE observed at lowest tested LET
> = No SEE observed at highest tested LET
σ = cross section (cm^2/device, unless specified as cm^2/bit)
σ_{SAT} = saturation cross section at LET_{max} (cm^2/device, unless specified as cm^2/bit)
LDC = lot date code
DUT = device under test
P.I. = principal investigator
Samp. = sample
HI = Heavy Ion
P = Proton
ADC = analog to digital converter
ALU = arithmetic logic unit
ASIC = application specific integrated circuit
BERT = bit error rate test or tester
CCD = charge collection device
CLB = configuration logic block
CMOS = complementary metal oxide semiconductor
DAC = digital to analog converter
FET = field effect transistor
FPGA = field programmable gate array
IAμE = NASA Institute of Advanced Microelectronics
MSB = most significant bits
NVM = non-volatile memory
Op Amp = operational amplifier
PROM = programmable read-only memory
PWM = pulse width modulator
RAM = random access memory
SRAM = static random access memory
SSPC = solid state power controller

TABLE VII: DEVICE CATEGORY ABBREVIATIONS:

P = Processor Component
TC = Test chip
MX = Mixed Signal
A = Analog
M = Memory
H = Hybrid
L = Logic or I/O

TABLE VIII: SUMMARY OF SEE TEST RESULTS

Device Category (Prime)	Device Category (Sub)	Part Number	Manufacturer	LDC	Device Function	Process	Particle: (Facility) P.I.	Test Results LET in MeV-cm^2/mg σ in cm^2/device, unless otherwise specified	SEE Usage Category.	Supply Voltage	Samp. Size	Test Report
Processor Components:												
P	–	CULPRiT C8051	IAµE	No LDC (Test Chip)	Microcontroller, (Ultra Low Power)	CMOS	H: (TAMU) JH	H: SEL LETth >85; SEU and SEFI LETth >20	RTV	0.5	2	See tns05_Howard [10]
P	–	P80C3224	Intel	L251PC28F	Microcontroller, 80C32	CMOS	H: (TAMU) JH; P: (IU) JH	H: 12< SEL LET_{th} <29; SEU and SEFI LET_{th} < 2.8 P: No SEL; SEU & SEFI observed	3	5	H: 2 P: 9	See tns05_Howard [10]
P	–	DS80C320	Dallas Semiconductor	0233	Microcontroller, 80C32	CMOS	H: (TAMU) JH; P: (IU) JH	H: 29< SEL LET_{th} <41; SEU and SEFI LET_{th} < 2.8 P: No SEL; SEU & SEFI observed	3	5	3	See tns05_Howard [10]
Analog Devices:												
A	–	OPA128	Burr-Brown	Z number no LDC	Op Amp	CMOS FET	H: (TAMU) SK/KL	SEL LET_{th} >53.8; SET LET_{th} <53.8; SET σ ~1x10^{-4}cm^2	3	±10	2	T022404_IFN423_OPA128 [11]
A	–	IFN423	InterFet Corp.	9638	N-channel transistor	Bipolar	H: (TAMU) SK/KL	SEL LET_{th} >53.8; SET LET_{th} >53.8	1	.7 & 2.3	2	T022404_IFN423_OPA128 [11]
A	–	SG1526	Linfinity/ Microsemi	0219	PWM	Bipolar	H: (BNL) SB	SEL LET_{th} <120; SET LET_{th} ~5; SET σ_{SAT} = 2x10-4 @ LET 120	1	10	2	No test report available for SG1526 (data analysis in progress)
Test Chips:												
TC	M	LXA0387 Test Chip – G12 Process	LSI Logic	0414	512Kbit SRAM ASIC	0.18µm CMOS - bulk	H: (TAMU; MSU) CP L: (NRL) CP	H: (TAMU) 13.5< SEL LETth <29; SEU LET_{th} <2.8; H: (MSU) 14.1< SEL LET_{th} <29; SEU σ ~3.5x10^{-8} @LET 41 L: SEL sensitive areas were identified	3	1.8	4	(no report available – request info from P.I.)
TC	P	LXA0381 Test Chip – G12 Process	LSI Logic	0412	64-bit ALU ASIC	0.18µm CMOS - bulk	H: (TAMU) CP; L: (NRL) CP	H: (TAMU) SEU σ ~1.12x10^{-9} @ LET 2.8; Micro latch- observed @ LET 2.8; L: SEL sensitive areas were identified; power cycle necessary to recover functionality	4	1.8 (Core); 2.5, 3.3 (I/O)	4	(no report available – request info from P.I.)
TC	M	Si Nano-Crystal Test Chip	Freescale	No LDC (Test Chip)	NVM 4Mb Flash EEPROM	CMOS	H: (TAMU) TO	SEU LET_{th} <8; Possible SEGR @ LET 85	RTV	Gate 8.2 (write), -7 (erase), 3.3 (read); Drain 6.2, 5.5, 2.3	8	T060304_freescale-nvm.pdf [12], T121804_freescale-nvm.pdf [13] Oldham_tns05 [14], NVM04 [15], nsrec04 [16], and T022204_Motorola [17]

Device Category	Device Category	Part	Manufacturer	LDC	Device Function	Process	Particle: (Facility) P.I.,	Test Results	SEE Usage Category.	Supply Voltage	Samp. Size	Test Report
Hybrid Devices:												
H	–	LS2805S	International Rectifier	0449	DC-DC Converter	Hybrid	H: (TAMU) CP/SB	SEL and SEB LET_{th} >90; SET LET_{th} < 53.9; SET σ = 1.6x10^{-3} @ LET 90 (worst case); In rush current condition LET_{th} < 53.9 and σ = 1.5x10^{-4} @ LET 90	2	22; 28; 35	2	T082604_LS2805S [18]
H	–	RP21002; RP21005; RP210010	Data Device Corporation	RP21002, 0342; RP21005, 0343/0418; RP210010, 0444/0507	SSPC	Hybrid	H: (TAMU) CP/SB	Switch On: SEL LET_{th} > 77; SET LET_{th} <2.8; SET σ = 1x10^{-3} @LET 78; (extremely sensitive to SET; output switch permanently turned off in some cases); Switch Off: SEB @ LET 29.9 with V_{out}=50V	4	22; 34	4	T121804_RP21005 [19]
H	–	53278	Micropac	No LDC (Test Chip)	28VDC SSPC	Hybrid	H: (TAMU) SB/CP	SEL LET_{th} > 54; SET LET_{th} > 54;	1	15	2	T121804_53278 [20]
Mixed Signal Devices:												
MX	–	LTC1419	Linear Technology	No LDC (Test Chip)	14-bit ADC	CMOS	H: (TAMU) SB/CP	SEL LET_{th} > 78.2; No SEFIs observed; SEU LET_{th} < 2.8; SEU σ_{SAT} = 1x10^{-3}	3	0.512; 1.19; 2.12	3	T060304_LTC1419 [21]
MX	–	7872	Maxwell	No LDC (Test Chip)	14-bit ADC	CMOS	H: (BNL) SB	SEL LET_{th} >60; SEU LETth ~1; SEU σ ~4x10-3 (with out 9 MSB used)	2	±5	2	B012605_7872 [22]
MX	–	MAX529	Maxim	0126	8-bit DAC	CMOS	H: (TAMU) CP/RL	SEL LET_{th} > 84; SET LET_{th} <54; SET σ_{SAT} ~3x10^{-5}	2	5	3	T060304_MAX529 [23]
Logic or I/O Devices:												
L	P	Virtex II Pro XC2VP7	Xilinx	No LDC (Test Chip)	FPGA	CMOS	H: (TAMU/ MSU) JH	SEL LET_{th} >53.9; SEU/SEFI LET_{th} <1	3	3.3	3	powell_mapld04_VirtexIIPro [24]
L	–	54ACTQ16245	National Semiconductor	0334	16-bit Transceiver	CMOS	H: (TAMU) SK	SEL LET_{th} >53.9; SET LET_{th} >59.3; SET σ = 1x10^{-7} @LET 59.3	1	5	3	T060504_54ACTQ16245 [25]
L	–	Stratix EP1S25	Altera	0401	FPGA	FPGA	H: (TAMU) TS/KL	SEL LET_{th} < 2.8; SEU LETth < 2.8	4	3.3	2	T122004_Altera_EP1S25 [26]; T031405_Altera_ EP1S25 [27]
L	–	UT54LVDS031	Aeroflex	0443/0335	Transmitter	CMOS	H: (BNL) SB	SET LET_{th} > 84.96	1	3.3; 5	2	B112304_ UT54LVDS031_32 [28]
L	–	UT54LVDS032	Aeroflex	0433/0333	Receiver	CMOS	H: (BNL) SB	SET LET_{th} > 84.96	1	3.3; 5	1	B112304_ UT54LVDS031_32 [28]
Memory Devices:												
M	–	28C010	Maxwell	No LDC (Test Chip)	EEPROM	CMOS	H: (BNL) SB	SEL LET_{th} >60; SEU LET_{th} ~20; SEU σ ~3.5	2	5	3	B012605_28C010 [29]
M	–	HN58V1001	Renesas	0433	EEPROM	CMOS	H: (BNL) SB	SEL LET_{th} >60; SEU LET_{th} >120	1	5	3	B012605_HN58C1001 [30]

TABLE IX: SUMMARY OF SEL TEST RESULTS

Device Category (Prime)	Device Category (Sub)	Part Number	Manufacturer	LDC	Device Function	Process	Particle: (Facility) P.I.)	Test Results LET in MeV·cm^2/mg σ in cm^2/device, unless otherwise specified	SEE Usage Category.	Supply Voltage	Samp. Size	Test Report
Memory Device:												
M	–	SDRAM Test Chip	Maxwell	No LDC (Test Chip)	256M SDRAM	CMOS	H: (TAMU) RL/CP	H: SEL 73> LETth >63 (at 30°C); SEL 56> LETth >43 (at 85°C); SEL sSAT ~1.5x10-3 @ LET 108 (at 30°C and 85°C	3	3.3	2	T031205_SDRAM_TestChip [31]

IV. Test Results and Discussion

As in our past workshop compendia of GSFC test results, each DUT has a detailed test report available online at http://radhome.gsfc.nasa.gov [9] describing in further detail, test method, SEE conditions/parameters, test results, and graphs of data. This section contains a summary of testing performed on a selection of featured parts.

1) Virtex II Pro XC2VP7 FPGA from Xilinx:

The Xilinx Virtex-II Pro is a SRAM-based platform FPGA that embeds multiple microprocessors within the fabric. The FPGA used was the commercial Xilinx Virtex-II Pro XC2VP7-6FG456C device. This device includes a single embedded PowerPC processor, 4.4 million configuration bits, 792 kB of BlockRAM, 8 RocketIO™ Multi-Gigabit Transceivers (MGT), 4 Digital Clock Managers (DCM), and 44 dedicated 18x18 multipliers [32]. The package used will be the wire-bond 456-pin ball grid array (FG456).

The objective of this coarse Single Event Effect (SEE) test was to determine the suitability of the commercial Virtex-II Pro family for use in spaceflight applications. To this end, this test was primarily intended to determine any Single Event Latchup (SEL) susceptibilities for these devices. Secondly, this test was intended to measure the level of Single Event Upset (SEU) susceptibilities and in a general sense, where they occur.

The coarse SEE test used a commercial-off-the-shelf (COTS) Virtex-II Pro evaluation board provided by Memec. This board is the Memec DS-KIT-2VP7FG456 (Fig. 1), which contains one soldered FPGA along with external RAM, PROMs, RS-232 port, JTAG connectors, MGT drivers and connectors, oscillators, power converters, and various user switches. Also included with this board was a prototyping daughter card (DS-KIT-P160-PROTO), which was populated with RS-422 line drivers to generate discrete pulses that indicate detected upsets. The FPGA on this board is replaced with a delidded device and partially covered with a shield. During SEU testing, this shield was placed on the device to only expose certain portions of the logic, routing, configuration memory resources, MGTs, or PowerPC.

The FPGA circuitry that underwent SEE testing included the following Virtex-II Pro functional elements: (a) the PowerPC processor, (b) MGTs, (c) BlockRAM, (d) dedicated multipliers, (e) CLBs, and (f) configuration RAM. These functional elements were tested using the combination of the BERT reference application and standalone test structures. The Xilinx Bit Error Rate Test (XBERT) reference application, which was modified to accommodate this board and test, tested the operation of the processor and the MGTs. For testing purposes, the MGT cables were hooked up in loopback (i.e. TX -> RX). This allows the transmitted pseudo-random data to be compared at the receiver, and detect any bit errors.

The XBERT application consists of: (a) a FPGA image containing processor peripherals and MGT support circuitry, (b) embedded software running on the PowerPC processor, and (c) user interface software running on a standalone PC. This PC communicates with the Memec board via a RS-232 interface. Using this application, MGT upset events are observed as bit errors or link failures, which are displayed on the user interface log window. Processor errors are detected as software malfunctions, also indicated on the user interface log window (i.e., corrupted RS-232 communications, software hanging, etc.).

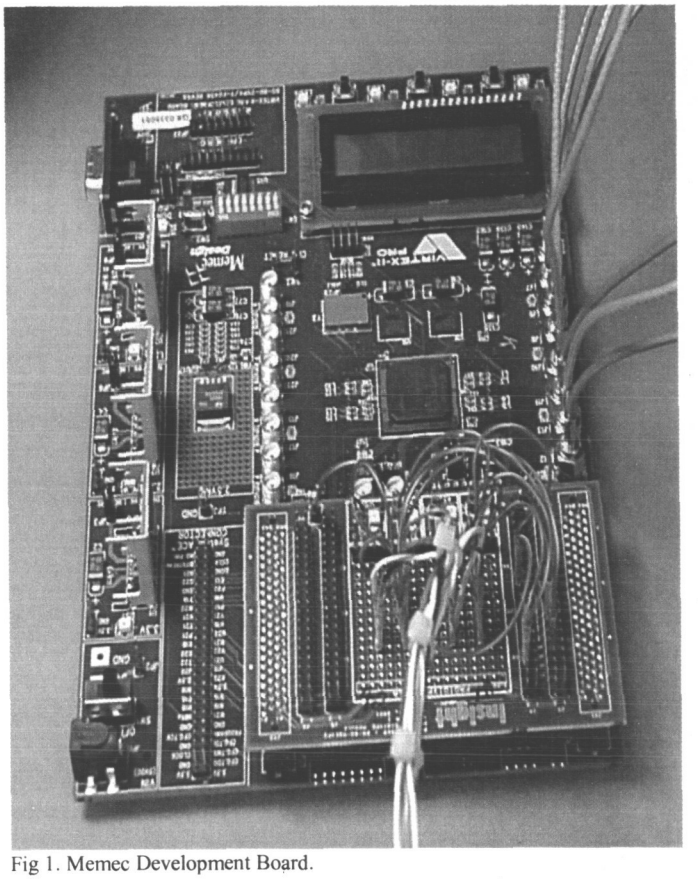

Fig 1. Memec Development Board.

The BlockRAM, multipliers, configuration RAM, and CLBs were tested with a dedicated test structure. This test structure, which is depicted in Fig. 2, consists of dual sets of circuitry, with one set in the exposed area and the other in the shielded area. Both are driven with a pseudo-random data generator. The outputs of these sets of circuitry are then compared. If detected, the comparators generate error pulses indicating upsets in the exposed circuitry.

This test structure can either be integrated with the BERT application, resulting in a single FPGA image, or programmed as a standalone function. During testing, this will enable the flexibility to isolate different functionality of the FPGA, or run all logic at once. By floorplanning the designs accordingly, different parts of the device/design can be shielded to suppress any unwanted SEEs.

Two onboard oscillators were used by the FPGA to derive the internal clock frequencies using DCMs. A 100 MHz oscillator was connected to one DCM that used this as a reference to supply the PowerPC with a 200 MHz clock and

the FPGA fabric with a 50 MHz clock. The other DCM was connected to a 125 MHz oscillator, which controlled the MGT reference clock that derived the data rate. The MGTs were set to run at 2.5 Gbps.

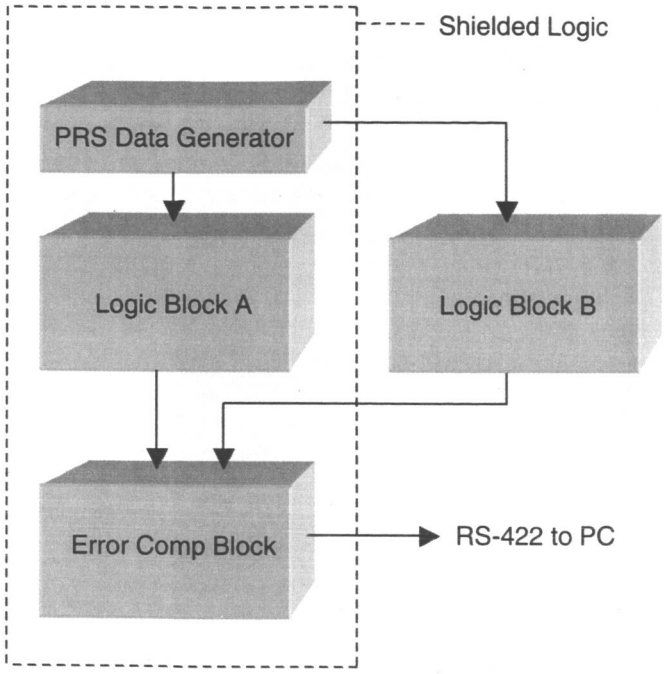

Fig 2. SEU Comparison Logic.

a) Virtex II Pro XC2VP7 - SEL Testing

The main goal of the coarse SEE test for the Virtex-II Pro was to determine if the device will enter a latch-up state under radiation conditions. When testing at the cyclotron facilities at Texas A&M or Michigan State Universities, no destructive SEL event was observed to a LET of 53.9 MeV•cm^2/mg and a fluence of 10^7 ions/cm^2.

During SEL testing, some interesting observations were made. While the device was irradiated the internal current (I_{CCINT}) slowly rises at a constant rate, which is a function of the radiation characteristics. The increased current is most likely the result of the configuration bits turning "on" causing internal bus contentions. However, once a current of ~ 3.4 A is reached, the current drops to 0 A, jumps back up to nominal, and then continues to ramp. It was determined that the device was being reprogrammed via on-board PROMs.

As shown in Fig. 3, the current cycling is symmetric and the core voltage (V_{CCINT}) does not sag. An existing 40-pin remote-sensing power cable was extended with custom 12-inch fly-leads to accommodate the Memec board. Although not shown on the plot, due to the modified power delivery and measurement setup, V_{CCINT} actually sagged at higher currents. V_{CCINT} was falling below the minimum voltage required to properly power the device due to a small IR drop across the fly-lead extension. This caused a power-on reset (POR) sequence to occur in the FPGA.

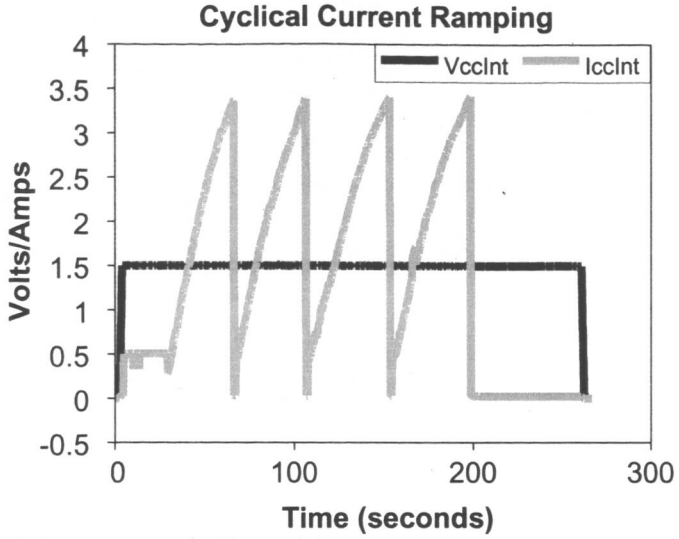

Fig 3. Current Ramping Characteristic.

b) Virtex II Pro XC2VP7 - SEFI Testing

The purpose of this testing phase was to document any observed event that would be classified as a Single Event Functional Interrupt (SEFI) such as a failure in a MGT link or the PowerPC log data getting corrupted, skipping instructions, or halting. The main objective was to focus on the PowerPC operation. For this case, the mask was used to approximately cover the PPC. Although the exact location of the PowerPC resources are unknown, the mask placement served as a rough estimate for initial testing purposes.

Fig. 4. shows the SEFI data collected. When testing with the PowerPC core exposed, the flux of the beam was turned down very low as the PPC was extremely sensitive. Therefore, collecting statistically significant SEFI data was very difficult and time consuming.

c) Virtex II Pro XC2VP7 - Configuration Bit SEU Testing

During the SEL testing, a configuration readback was performed after each run to determine the number of upset configuration bits. This was simply performed by clicking the 'Verify' command in the Xilinx ISE 6.1i iMPACT tool. This command counts the number of differences found in the configuration data. Fig. 5 shows the results of this data. Note that there are ~ 4.4 million configuration bits for this particular part.

To make an attempt to account for the MGT configuration bits, a mask was placed on the FPGA to allow only four MGTs to be exposed. The cross section was reduced by approximately a factor of 10. This agrees with the fact that about 90% of the die was shielded from the radiation.

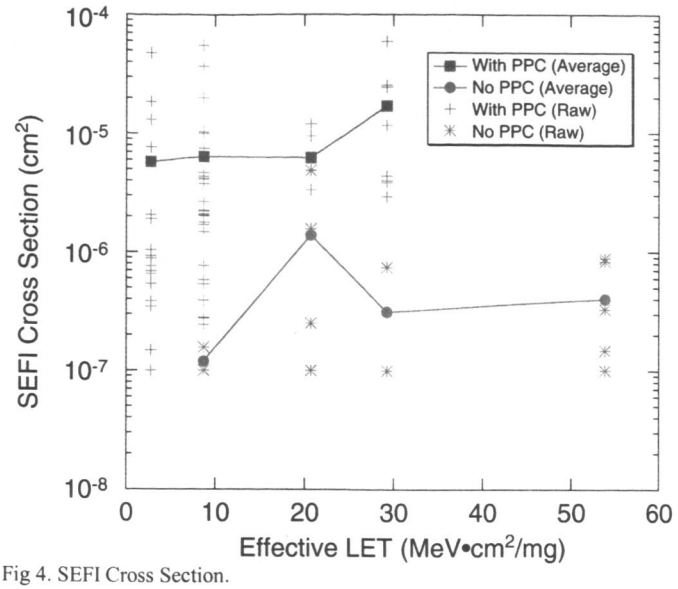

Fig 4. SEFI Cross Section.

After each test run, the configuration bit errors were counted and the action required to reestablish the functionality of the device was documented. During SEL testing, over 400,000 configuration bit errors (>10%) were recorded twice and the JTAG link failed twice. Both types of occurrences were probably due to configuration errors in the JTAG circuitry.

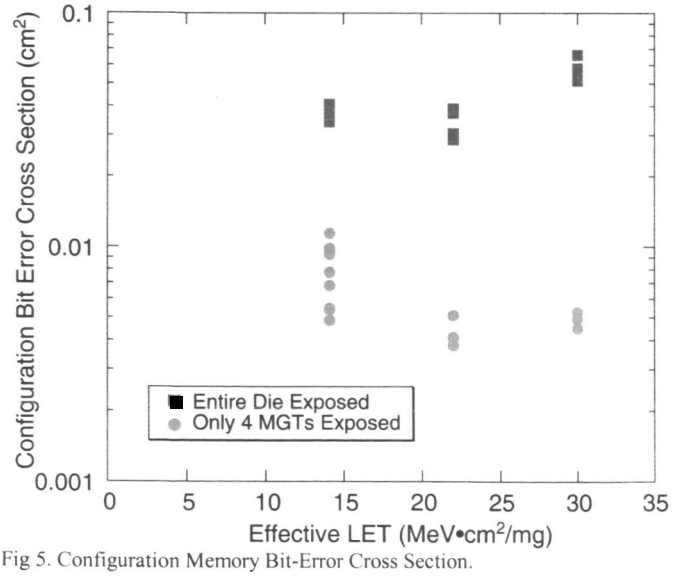

Fig 5. Configuration Memory Bit-Error Cross Section.

d) Virtex II Pro XC2VP7 - MGT SEU Testing

The goal of this test was to gather upset data on the MGTs. The data pattern used to drive the MGT transmit ports was a pseudo-random pattern of $1+X^6+X^7$. The MGTs were running at a date rate of 2.5 Gbps. The shield configuration used when testing for MGT SEEs masked off the DUT except for the area containing one MGT, specifically MGT6 on the XC2VP7.

For each run, the number of MGT bit errors was recorded. This data was extracted from the PowerPC log file. The run was terminated upon MGT link failure. Fig. 6 shows the cross section data collected with a Weibull fit to that data. The threshold LET was found to be about 0.1 MeV•cm²/mg and the saturation cross section was approximately 2.6×10^{-5} cm².

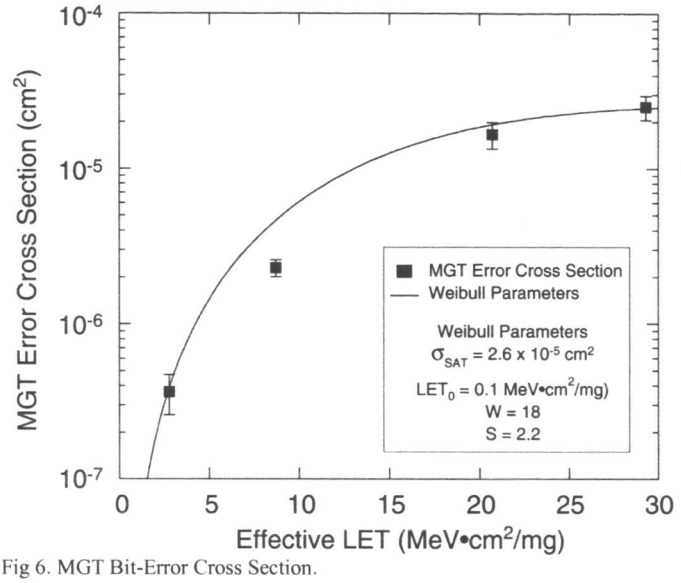

Fig 6. MGT Bit-Error Cross Section.

e) Virtex II Pro XC2VP7 - Summary

The commercial-grade Virtex-II Pro did not enter a latch-up state during these tests. However, a preliminary conclusion is that the MGTs and embedded PowerPC have a high susceptibility to the heavy ion radiation since SEFIs occurred too quickly to collect substantial data. Due to the limitations on isolating the PowerPC with a shield configuration, new test methods need to be developed in order to gather more conclusive data on its operation.

The Memec board was a good test bed for the coarse SEE test, however, in order to allow more flexibility for future tests, another board more suited for radiation testing is needed. [24]

2) 28VDC Solid State Power Controller RP21000 series from DDC:

The RP21000 series are 28VDC Solid State Power Controller (SSPC) rated from 2 through 25A. They are hybrid devices. Fig. 7 shows a picture of a de-lidded device. The SSPC uses five active integrated circuits that may be potentially sensitive to Single Event Effects (SEE). All the active components are located sufficiently far apart from one another that they cannot all be irradiated at the same time. Two different device areas were irradiated in order to check the SEE sensitivity of all active parts. Fig. 7 shows the two areas that were irradiated. The picture shows a 5A device (RP21005). All devices used the same control circuitry. The only difference is that they used a different number of power MOSFETs to draw the rated current. The 2A device (RP21002) only uses one transistor. The 5A devices use 2 transistors, as shown in the figure. The 10A device (RP21010) uses four transistors.

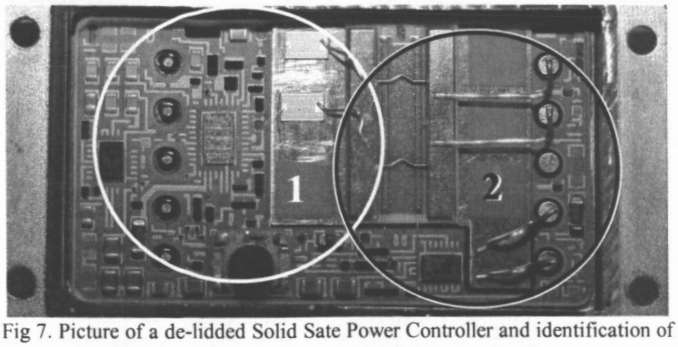

Fig 7. Picture of a de-lidded Solid Sate Power Controller and identification of the two irradiated areas.

Four different devices, two RP21005, one RP21002, and one RP21010 were irradiated. The device bias supply voltage was set at 5V. The DUTs were irradiated with the output switch in the on state (control input at high level) and in the off state (control input at low level). In the on state, different output voltages were applied ranging from 22V to 40V, and different load conditions were applied ranging from 10% to 100% of maximum load. In the off state, two different voltages, 40V and 50V, were applied to the device output. 40V corresponds to the maximum recommended value, and 50V corresponds to the absolute maximum rating.

The output of the DUT was monitored with an oscilloscope. As soon as the DUT output exceeded a given trigger level set below the nominal value, the resulting waveform, termed a SET, was captured on the oscilloscope and subsequently stored on a PC.

No SEE was observed when the area 2 was irradiated up to the maximum tested LET of 77 MeV•cm^2/mg. When area 1 was irradiated with the device in the on mode, the device showed a very high sensitivity to SETs at the device output. The switch may be turned off very easily. When the switch was turned off, it was generally coming back to the on state after a period varying from 200 to 500 µs. However, in some cases, the switch stayed in the off state. When the switch is turned off, the control input should go back to the low level and then to the high level to turn the switch on again. Fig 8 shows a typical transient at the device output. Fig 9 shows an example where the switch was turned off and needs a control input command to be turned back on. The device is sensitive to SET down to lowest test LET of 2.8 MeV•cm^2/mg. The SET cross section at the maximum tested LET is about 1x10^{-3} cm^2/device. Fig 10 shows the SET cross section curve. No destructive condition was observed up to the maximum tested LET of 77 MeV•cm^2/mg in the on mode. In the off mode, destructive conditions, output power MOSFET Single Event Burnout (SEB), were observed down to a LET of 29.9 MeV•cm^2/mg. [19]

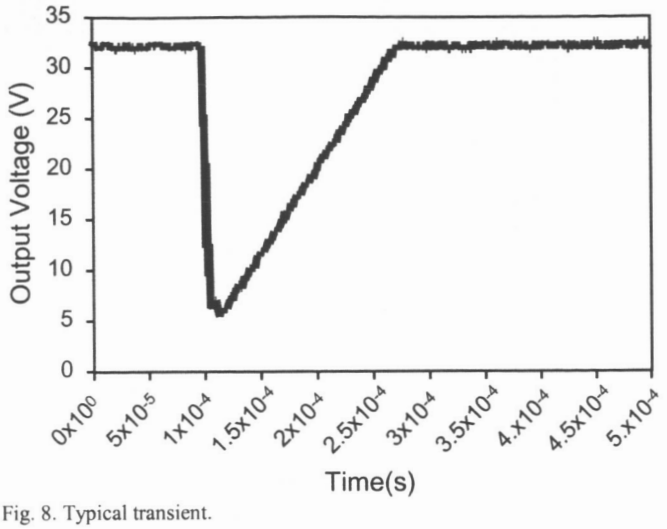

Fig. 8. Typical transient.

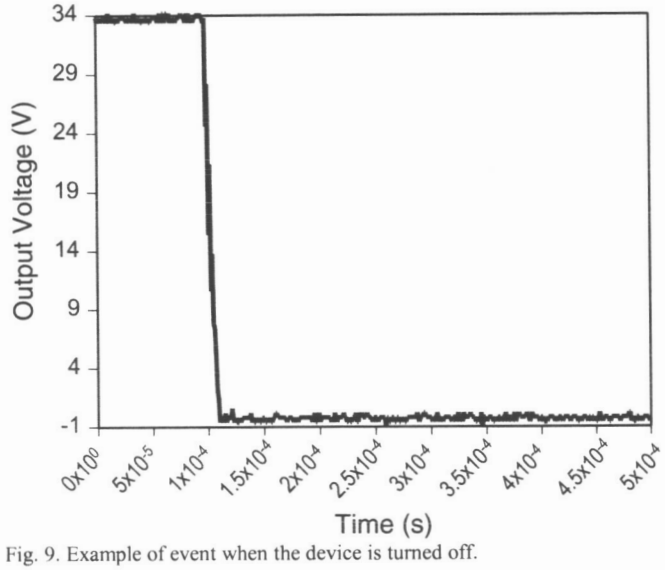

Fig. 9. Example of event when the device is turned off.

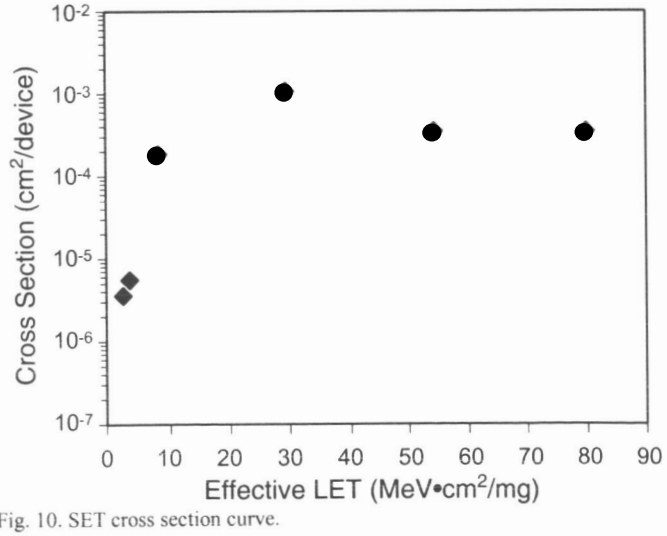

Fig. 10. SET cross section curve.

V. Summary

We have presented recent data from SEE on a variety of mainly commercial devices. It is the authors' recommendation that this data be used with caution. We also highly recommend that lot testing be performed on any suspect or commercial device.

VI. Acknowledgment

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