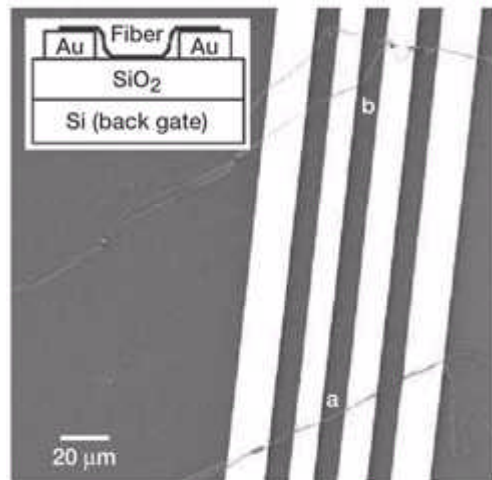


# Field Effect Transistor Behavior in Electrospun Polyaniline/Polyethylene Oxide Demonstrated

Novel transistors and logic devices based on nanotechnology concepts are under intense development. The potential for ultra-low-power circuitry makes nanotechnology attractive for applications such as digital electronics and sensors. For NASA applications, nanotechnology offers tremendous opportunities for increased onboard data processing, and thus autonomous decisionmaking ability, and novel sensors that detect and respond to environmental stimuli with little oversight requirements. Polyaniline/polyethylene oxide (PANi/PEO) nanofibers are of interest because they have electrical conductivities that can be changed from insulating to metallic by varying the doping levels and conformations of the polymer chain.

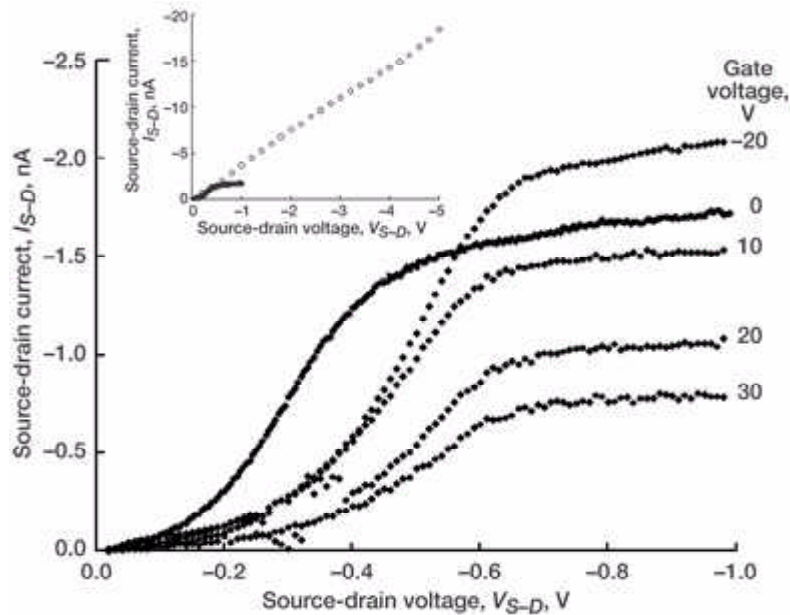


*Scanning electron microscope image of electro-spun PANi/PEO fibers over a prepatterned Si/SiO<sub>2</sub> substrate.*

Long description. The device is made up of just two fibers (a and b) contacting the two inner electrodes. Inset: Schematic cross section of the device showing a fiber bridging the gap between the source and drain gold electrodes.

At the NASA Glenn Research Center, we have observed field effect transistor (FET) behavior in electrospun PANi/PEO nanofibers doped with camphorsulfonic acid. The nanofibers were deposited onto Au electrodes, which had been prepatterned onto oxidized silicon substrates. The preceding scanning electron image shows the device used in the transistor measurements. Saturation channel currents are observed at surprisingly low source/drain voltages (see the following graph). The hole mobility in the depletion regime is  $1.4 \times 10^{-4} \text{ cm}^2/\text{V}\cdot\text{sec}$ , whereas the one-dimensional charge density (at zero gate bias) is calculated to be approximately 1 hole per 50 two-ring repeat units of polyaniline, consistent with the rather high channel conductivity ( $\sim 10^{-3} \text{ S/cm}$ ). Reducing or eliminating the PEO content in the fiber is expected to enhance device parameters. Electrospinning is

thus proposed as a simple method of fabricating one-dimensional polymer FET's.



*Current-voltage characteristics of the FET device. Inset: Current-voltage characteristics of the device with no applied back gate voltage.*

Long description. Graph of source-drain current in nanoamperes versus source-drain voltage for gate voltages of -20, 0, 10, 20, and 30 volts. The device is made up of two nanofibers (with lengths of 12 and 18 micrometers and diameters of 300 and 120 nanometers, respectively, bridging the source-drain contacts) at different back gate voltages. Accumulation and depletion modes are shown. Inset: Ohmic behavior (open symbols) does not change with back gate voltage. Saturation behavior (solid symbols) does change with back gate voltage.

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**Headquarters program office:** OAT

**Programs/Projects:** DDF, Space Science--such as Magnetospheric Constellation, Deep Space Probes(e.g., missions to Mars and Jupiter)