METAL-FERROELECTRIC-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR NAND GATE SWITCHING TIME ANALYSIS

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ABSTRACT

Previous research investigated the modeling of a NAND gate constructed of Metal-Ferroelectric-Semiconductor Field-Effect Transistors (MFSFETs) to obtain voltage transfer curves. The NAND gate was modeled using n-channel MFSFETs with positive polarization for the standard CMOS n-channel transistors and n-channel MFSFETs with negative polarization for the standard CMOS p-channel transistors. This paper investigates the MFSFET NAND gate switching time propagation delay, which is one of the other important parameters required to characterize the performance of a logic gate. Initially, the switching time of an inverter circuit was analyzed. The low-to-high and high-to-low propagation time delays were calculated. During the low-to-high transition, the negatively polarized transistor pulls up the output voltage, and during the high-to-low transition, the positively polarized transistor pulls down the output voltage. The MFSFETs were simulated by using a previously developed model which utilized a partitioned ferroelectric layer. Then the switching time of a 2-input NAND gate was analyzed similarly to the inverter gate. Extension of this technique to more complicated logic gates using MFSFETs will be studied.

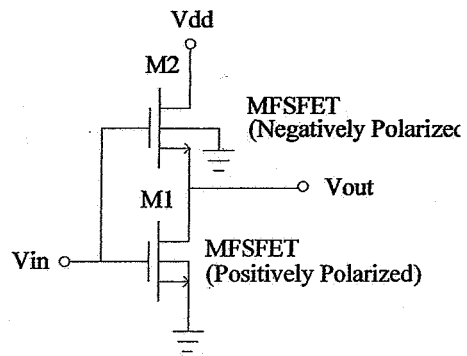* Author to whom correspondence should be addressed.

Vdd

M2

MFSFET
(Negatively Polarized)

Vout

M1

Vin

MFSFET
(Positively Polarized)

Figure 1: MFSFET Inverter Circuit

Vdd

M3

MFSFET
(Neg. Polarized)

M4

MFSFET
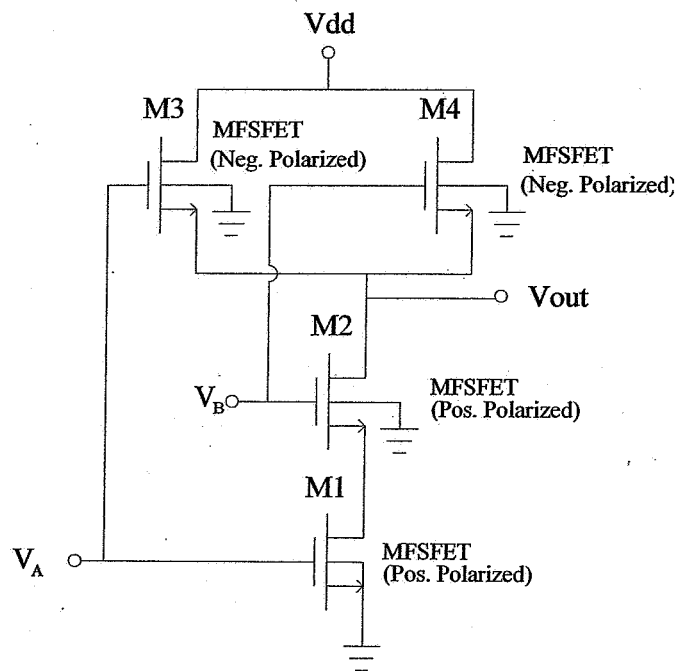(Neg. Polarized)

Vout

M2

V_B

MFSFET
(Pos. Polarized)

M1

V_A

MFSFET
(Pos. Polarized)

Figure 2: 2-Input MFSFET NAND Gate