

Single-Event Upset and Scaling Trends in New Generation of the Commercial SOI PowerPC Microprocessors

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35-WORD ABSTRACT:

SEU from heavy-ions is measured for SOI PowerPC microprocessors. Results for 0.13 μ m PowerPC with 1.1V core voltages increases over 1.3V versions. This suggests that improvement in SEU for scaled devices may be reversed.

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Session Preference: Radiation Effects on Electronic and Photonic Devices and Circuit

Presentation Preference: Oral

I. INTRODUCTION

In recent years there has been interest in the possible use of unhardened commercial microprocessors in space because of their superior performance compared to hardened processors. However, unhardened devices are susceptible to upset from radiation space. More information is needed on how they respond to radiation before they can be used in space. Only a limited number of advanced microprocessors have been subjected to radiation tests, which are designed with lower clock frequencies and higher internal core voltage voltages than recent devices [1-6]. However the trend for commercial Silicon-on-insulator (SOI) microprocessors is to reduce feature size and internal core voltage and increase the clock frequency. Commercial microprocessors with the PowerPC architecture are now available that use partially depleted SOI processes with feature size of 90 nm and internal core voltage as low as 1.0 V and clock frequency in the GHz range.

Previously, we reported SEU measurements for SOI commercial PowerPCs with feature size of 0.18 and 0.13 μm [7, 8]. The results showed an order of magnitude reduction in saturated cross section compared to CMOS bulk counterparts.

This paper examines SEUs in advanced commercial SOI microprocessors, focusing on SEU sensitivity of D-Cache and hangs with feature size and internal core voltage. Results are presented for the Motorola SOI processor with feature sizes of 0.13 μm and internal core voltages of 1.3 and 1.1 V. These results are compared with results for the Motorola SOI processors with feature size of 0.18 μm and internal core voltage of 1.6 and 1.3 V.

The final paper will include SEUs in D-Cache and hangs for the newest generation of SOI PowerPC microprocessors with feature size of 0.09 μm from IBM and Motorola.

II. EXPERIMENTAL PROCEDURE

A. Device Descriptions

The Motorola 7457 PowerPC is fabricated with SOI technology. It uses a partially depleted technology without body ties. It has a feature size of 0.13 μm with a silicon film thickness of 55 nm and internal core voltage of 1.3 V. A low-power version of this processor operates with an internal core voltage of 1.1 V.

The older Motorola 7455 PowerPC has a feature size of 0.18 μm and internal core voltage of 1.6 V. A low-power version of this processor operates with an internal core voltage of 1.3 V.

It is important to note that the core voltage used in our tests is the specific core voltage designed by the manufacturer for the specific product. We do not know what specific changes have been made to the processor design or the design of the internal transistors to produce devices that will work reliably with such low voltages.

Table I. Summary of Motorola's PowerPC Family of SOI Processors.

SOI PowerPC	Feature Size (μm)	Core Voltage (V)	Maximum Operating Frequency (MHz)
7455	0.18	1.6	1000
7455*	0.18	1.3	800
7457	0.13	1.3	1000
7457†	0.13	1.1	1000
7448	0.09	0.9	1500

* This is a special low power version of the Motorola SOI PowerPC7455.

† This is a special low power version of the Motorola SOI PowerPC 7457.

Table I shows the recent SOI generations of the PowerPC. The feature size of the SOI Motorola PowerPC has been reduced from 0.18 to 0.09 μm , with the core voltage reduced from 1.6 to 1.0 V.

B. Experimental Methods

Radiation testing was done at the Texas A&M University cyclotron. This facility produces the long-range ions needed for SEU testing through thick materials. Particularly, the 40 MeV/amu beams are quite penetrating, and it is possible to do irradiations in the air rather than in vacuum. Undegraded ion beam used in our measurements are listed in Table II. Both ions have enough range to penetrate the die. The LET range of 1.7 to 15 MeV-cm²/mg was covered in the measurements. All irradiations were done using ions with normal incidence. Because of the "flip-chip" design of the Motorola PowerPC, irradiation was done from the back of the wafer (package top), correcting the LET to account for energy loss as the beam traversed the silicon. The thickness of the die is about 850 μm .

Radiation testing was done in the air using the "Sandpoint" development board. This eliminated the engineering effort required to design a custom test board for the processor, and also provided a basic PROM-based system monitor instead of a complex operating system. This provides better diagnostics and control of processor information during SEU testing compared to more advanced operating systems. The external communication channel on this board is a simple serial connection used as a terminal and a JTAG port.

The test methodologies used to measure upsets errors in the D-cache memory and hangs are discussed in detail in [1, 7, and 8] and briefly described in the following; Tests were performed on two to three parts for each processor type.

1- D-cache measurement

The cache was initialized under specified condition prior to irradiation and then disabled. Then a clearly recognizable pattern, designed to be distinctly different from contents of the cache, was placed in the external memory space covered by

the cache. Comparing the cache contents after irradiation provided verification of the cache contents. Upsets in the cache were counted with special post beam software.

Table II. List of the ion beams used in our measurements

Ion	Energy per Nucleon (MeV/amu)	Initial LET (MeV-cm ² /mg)	Range (μm)
²⁰ Ne	40	1.7	1648
⁴⁰ Ar	40	3.8	1070

2- Hangs measurement

We define hang as a complex functional errors where the processor operation is severely disrupted during the irradiation. We detected hangs by applying an external interrupt after the irradiation was ended; if the processor responded to the interrupt, it was still operational to the point where normal software could likely restore operation. If the interrupt could not restore operation, then the status was categorized as a hang. In nearly all cases, it was necessary to temporarily remove power from the device in order to recover and reboot the device.

We calculated the hang cross section defined as the number of times the processor would not respond to the external interrupts divided by the total fluence to which the processor had been exposed, including runs with no observed hangs. This was done for each LET.

III. TEST RESULTS

A. Data Cache

Fig. 1 compares results of the SEU measurements on the Motorola PowerPC 7457 with core voltage of 1.3 V to the results of the Motorola PowerPC 7457 with a core voltage of 1.1 V. The clock frequency for both measurements was 400 MHz. The SEU measurement for the part designed with lower operating voltage, 1.1 V, is slightly larger than the one for the operating voltage of 1.3 V.

Fig. 2 compares the results of the previous measurements on the Motorola PowerPC 7455 with a core voltage of 1.6 V with the results of the Motorola PowerPC 7455 with a core voltage of 1.3 V. The clock frequency for both measurements was 800 MHz. Contrary to the new results for SEU measurements for the Motorola 7457, there is no change in the SEU cross section for D-Cache of the older device.

The large number of storage locations within the data cache allows more statistically significant numbers of errors to be measured, decreasing the error bars due to counting statistics. The error bars in figures 1 and 2 are ~2 sigma and result from Poisson statistics. For the data points where statistical error bars are not shown, they are smaller than the size of the plotting symbols.

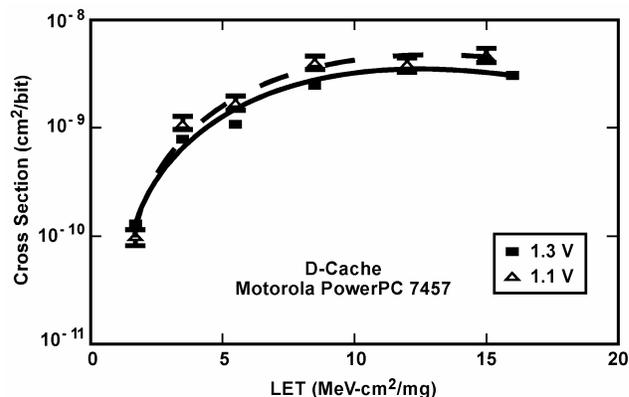


Fig. 1 Comparison of SEU cross sections for D-Cache for Motorola PowerPC 7457 with clock frequency of 400 MHz for internal core voltage of 1.3 and 1.1V [8]. The dashed and solid curves are only guides for the eye.

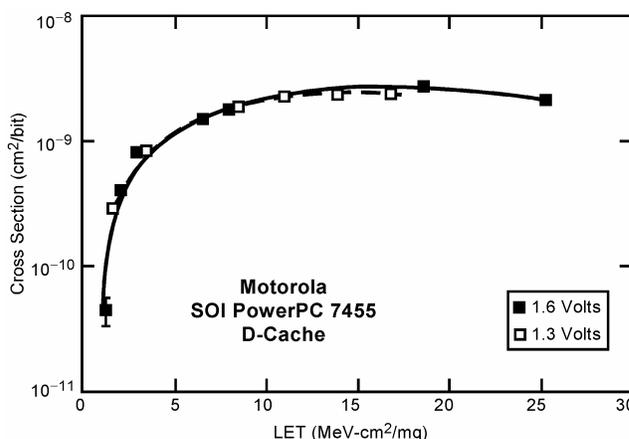


Fig. 2 Comparison of SEU cross sections for D-Cache for Motorola PowerPC 7455 with clock frequency of 800 MHz for internal core voltage of 1.6 and 1.3V [8]. The dashed and solid curves are only guides for the eye.

B. Functional Errors (“Hangs”)

Figure 3 compares estimated cross sections for hangs for two internal core voltage specifications during heavy-ion SEU measurements of the PowerPC 7457. The clock frequency for both measurements was 400 MHz. It is interesting to note that the hangs SEU cross section for the part designed with the lower operating voltage, 1.1 V, is larger than the hangs SEU cross section for the part designed for operating voltage of 1.3 V by a about a factor of 20.

Figure 4 compares the results of the estimated cross section for hangs for the Motorola PowerPC 7455 with core voltage of 1.6 V to those for a special version of the Motorola PowerPC 7455 that operates with a lower internal core voltage of 1.3 V. The clock frequency for both measurements was 800 MHz. These data has been published previously [8]. Contrary to the Motorola 7457, there is little difference between results of two measurements.

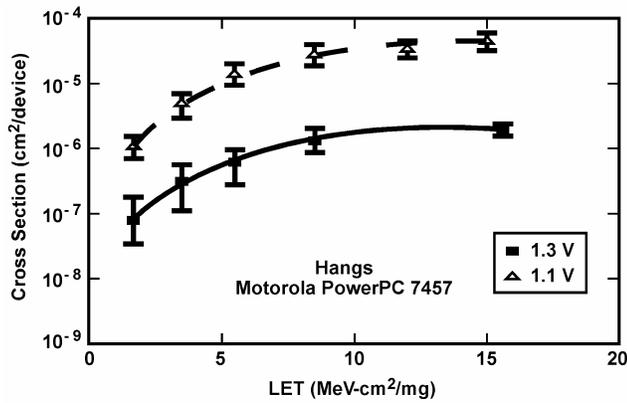


Fig. 3 Comparison of SEU cross sections for “hangs” for Motorola PowerPC 7457 with clock frequency of 400 MHz for internal core voltage of 1.3 and 1.1 V. The dashed and solid curves are only guides for the eye.

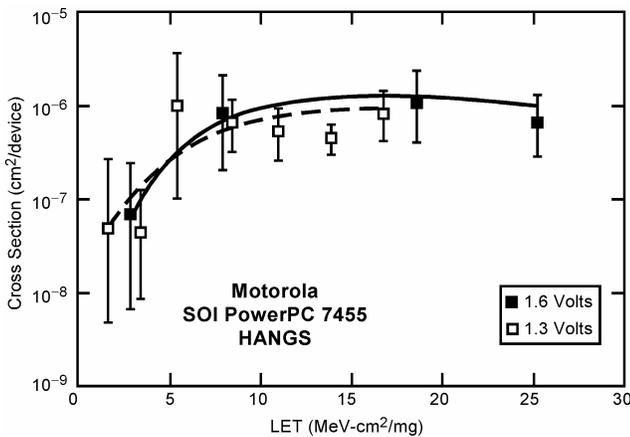


Fig. 4 Comparison of SEU cross sections for hangs for Motorola PowerPC 7455 with clock frequency of 800 MHz for internal core voltage of 1.6 and 1.3 V [8]. The dashed and solid curves are only guides for the eye.

For convenience in comparison, in Fig. 5, we display the results of the D-cache SEU measurements on the Motorola SOI PowerPCs for three internal core voltages of 1.1, 1.3 and 1.6 V on the same graph. Figure 6 displays estimated cross sections for hangs for the Motorola SOI PowerPCs for three internal voltages of 1.1, 1.3 and 1.6 V on the same graph.

IV. DISCUSSION

Feature sizes, silicon film thickness and internal core voltages are critical factors for single-event upset in SOI. Scaling for high-performance technologies depend heavily on reducing feature size, but also requires a reduction in internal core voltage [10]. The effect of scaling on partially depleted SOI structures is a far more difficult problem. The main advantage of SOI is a marked reduction in the thickness of the silicon region for charge collection. To first order, this should decrease the collected charge. However, charge amplification from the parasitic bipolar transistor that is inherent in partially depleted SOI increases the charge by a significant factor. Furthermore, considerable work has been done showing that the critical charge for SOI devices with low internal core voltages is expected to be lower for more highly scaled

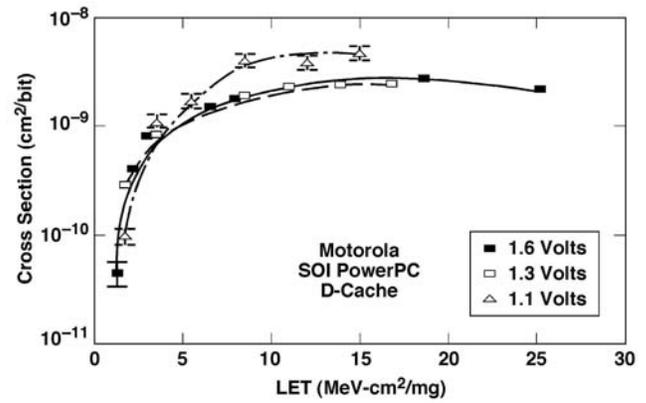


Fig. 5 Comparison of D-Cache for Motorola SOI PowerPCs for three different internal core voltages.

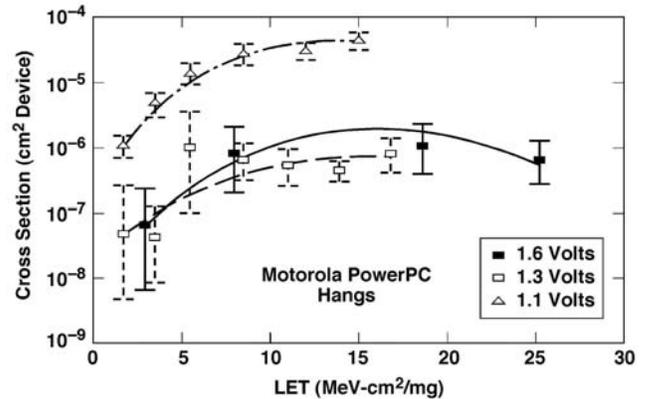


Fig. 6 Comparison of hangs for Motorola SOI PowerPCs for three different internal core voltages.

devices [11]. This might lead to the conclusion that SEU will be far more severe for highly scaled devices with lower internal core voltages. However, this has not been observed for high-performance devices such as microprocessors [12]. Other factors cause less charge to be collected as devices are scaled to smaller feature size.

Charge collection may also be lower when feature sizes are reduced below about 0.25 μm because the lateral distribution of charge from the ion track will extend beyond the active area. The decrease in critical charge is compensated for by a smaller area along with decreased charge collection efficiency.

For the Motorola PowerPC 7455 with feature size of 0.18 μm , the data shows (Figs. 3 and 4) no significant difference in D-Cache and hangs occurring between internal core voltages of 1.3 and 1.6 V. However, for the Motorola PowerPC 7457 with feature size of 0.13 μm , the data shows (Figs. 1 and 2) a significant difference in D-Cache and particularly in hangs between internal core voltages of 1.3 and 1.1 V. This suggests that reduction of the internal core voltage beyond a limit causes the improvement in SEU for highly scaled SOI commercial PowerPC microprocessors to be reversed. Because of the trend in scaling, feature size and internal core voltage are constantly decreasing, and the concern about SEUs is becoming an important factor, and it should be investigated in more detail.

The threshold LET of commercial processes has changed very little with scaling, and is only slightly influenced by the concerns of mainstream manufacturers with atmospheric radiation. However, the saturation cross-section has steadily decreased with smaller feature size. Fig. 7 shows how the cross section for D-cache has changed over several generations of the PowerPC family. [The abscissa is a logarithmic (base 2) inverse of scale reflecting the approximate doubling of feature size over various generations of CMOS devices.] The dashed lines show a slope of minus one half, reflecting the assumed dependence of area on the square of the feature size. There is a decrease of nearly a factor of ten in cross section with the transition to SOI processes.

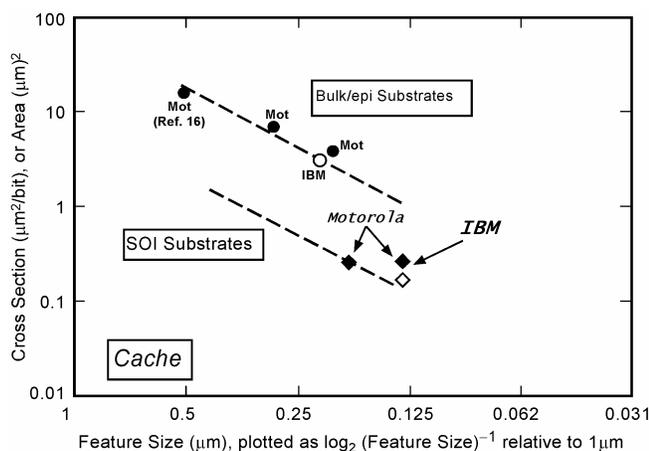


Fig. 7 Scaling trends for upset in D-cache (and basic SRAM designs) for PowerPC processors.

There is not a change in SEU cross section for the SOI processors with feature sizes of 0.13 and 0.18- µm. These results suggest that scaling between 0.18 and 0.13- µm feature size has little effect on SEU sensitivity. However, one might expect to see reduction in saturated cross section when there is a drastic change in feature size e.g. 0.09 µm. For SOI processors with the same feature size and silicon film thickness, but with different internal core voltage specifications, no significant changes were observed in upset rates. The upset rates of these devices are low enough to allow their use in space applications where occasional upsets can be tolerated.

The final paper will include SEU measurements of the new generation of commercial SOI PowerPC microprocessors with feature size of 0.09 µm from the Motorola and IBM. It would be interesting to study the effect of scaling on partially depleted SOI structures by comparing data for 0.09µm PowerPCs with our previous results for feature sizes of 0.13 and 0.18 µm. IBM recently has introduced PowerPC 970FX with feature size of 0.09 µm and a core voltage of 1.0 V [13]. Also, Motorola has introduced PowerPC 7448 with feature size of 0.09 µm and a core voltage of 0.9 V.

V. CONCLUSION

This paper has evaluated SEU cross section at internal core voltages as low as 1.1 V. The SEU cross section increases at lower internal core voltage of 1.1 V compared to results at internal core voltage of 1.3 V. More drastic results were obtained for estimated cross section for “hangs.” The estimated cross section is higher by more than an order of magnitude for the results at internal core voltage of 1.1 V.

Further reduction in internal core voltage together with increases in clock frequency may become serious factors in the overall impact of SEU rates for future generations of commercial SOI microprocessors.

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