

Radiation Characterization of a 0.11 μm Modified Commercial CMOS Process

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To be presented by Christian Poivey at the 2006 Single Event Effects Symposium (SEESYM), April 10, 2006 to April 12, 2006 in Long Beach, CA.



Outline

- Background – Introduction
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Background - Introduction

- **2004:**
 - Evaluation of LSI Logic 0.18 μm standard process
 - Evaluation of 0.18 μm modified process with a buried layer
 - No SEL up to a LET of 75 MeVcm^2/mg
 - High SEU sensitivity
- **2005:**
 - Evaluation of LSI Logic 0.11 μm standard process
 - 0.11 μm drawn bulk process with Small Trench Isolation (STI)
 - 1.2V core voltage, up to 3.3V I/O voltage
 - Up to 70 million logic gates on a chip
 - High density embedded SRAM
 - and two different versions of a modified process with buried layer

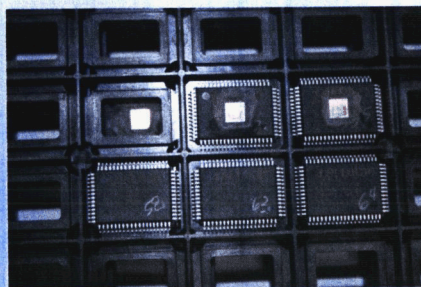
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Test Vehicles

- **SRAMs**
 - 4 Mbit (512K*8) made with standard embedded cells
 - RAM249, high speed design
 - RAM187, high density design
 - I/O voltage = 2.5V
 - 64 PQFP



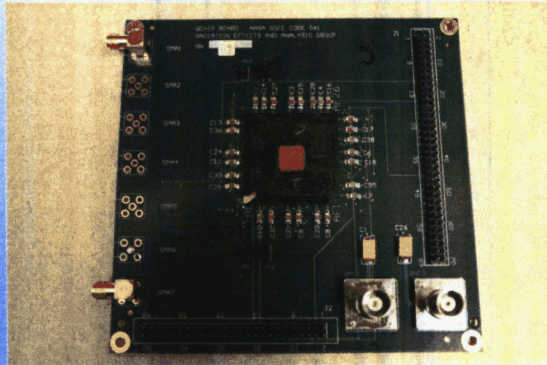
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Test Vehicles

- **Logic chip**
 - Made of 384 64-bit ALUs with registered inputs, outputs, and function control signals
 - Scan D type flip-flop with set and clear
 - I/O voltage = 3.3V
 - 492 EPBGA



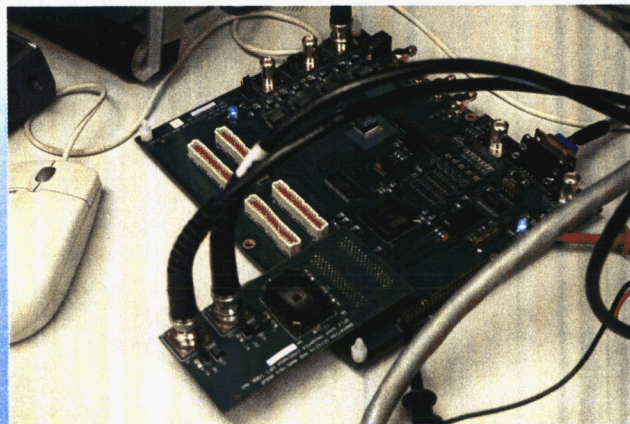
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Test conditions

- Used NASA-GSFC low cost digital tester (LCDT)
- SRAM: static and dynamic (10MHz clock cycle)
- Logic chip: test in scan mode (6 shift register chains of 200 flip-flop each) at 2 to Mhz clock speed.

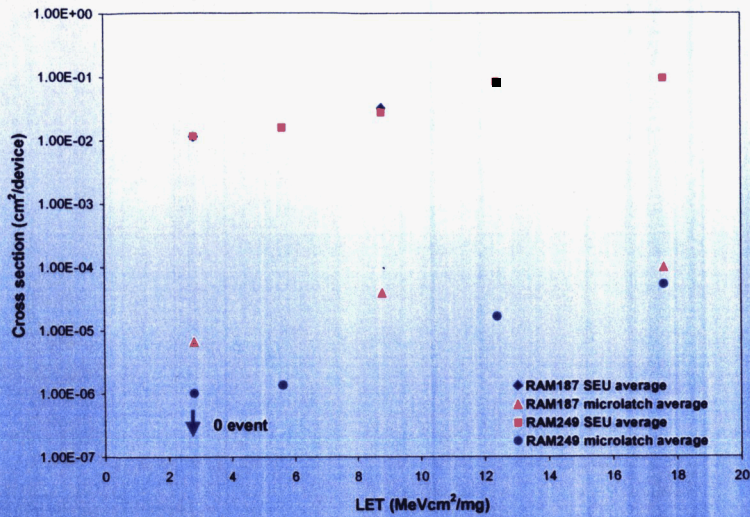


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Test results – SRAM standard process

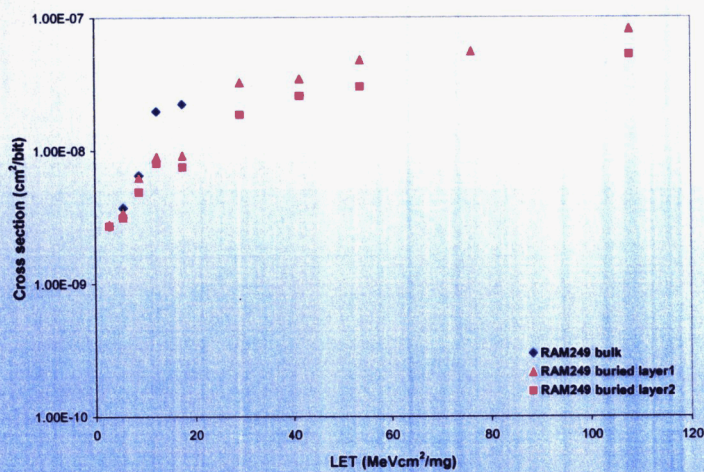


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Test results SRAM, RAM249, SEU, all processes

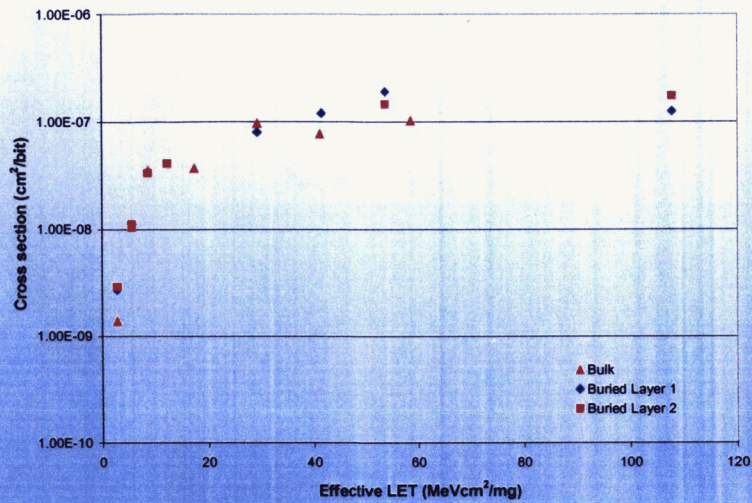


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Test results Logic chip, SEU



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Conclusion

- **0.11 μm process with 1.2V core voltage may still be sensitive to SEU/SEL**
- **SRAM cells have a very low LET threshold**
- **Significant diffusion effect at high LET**
- **Significant transient sensitivity even at low speed**

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