Application of RADSAFE to Model Single Event Upset Response of a 0.25 μm CMOS SRAM

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ASTRACT:

The RADSAFE simulation framework is described and applied to model SEU in a 0.25 μm CMOS 4Mbit SRAM. For this circuit, the RADSAFE approach produces trends similar to those expected from classical models, but more closely represents the physical mechanisms responsible for SEU in the SRAM circuit.

INTRODUCTION

Over the past two decades a series of publications ([1-15], for example) giving experimental and simulation evidence that show that Single Event Effects (SEE) analysis techniques akin to the rectangular parallelepiped (RPP) model [16] fail to provide accurate reliability/survivability estimates for certain technologies. The key to this is the recognition by many researchers that today's technologies have been scaled to dimensions where new phenomena challenge some of the basic simplifying assumptions of these radiation effects models, which were developed for technologies fabricated in the late 70's and early 80's.

The underlying physical mechanisms for Single Event Effect (SEE) response are: 1) ionizing radiation-induced energy deposition within the device, 2) initial electron-hole pair generation 3) the transport of the charge carriers through the semiconductor device and 4) the response of the device and circuit to the electron-hole pair distribution and subsequent transport. Each of these occurs on its own timescale and they are often assumed to be sequential, i.e., energy deposition determines the initial electron-hole pair generation, which in-turn impacts device and circuit response.

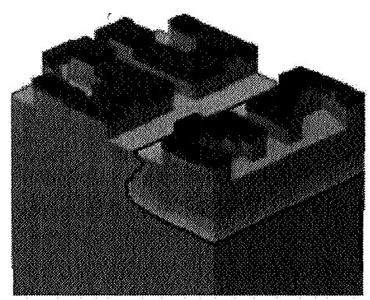

Fig. 1: TCAD model of entire SRAM cell. Red areas indicate n-type dopants, blue indicate p-type dopants.

The goal of the RPP model is to provide a simple, approximate model for the processes described above. This approach has been very successfully applied to space missions over several decades. In this work we describe a new modeling approach aimed at overcoming some of the limitations of the RPP model. We call this concept RADSAFE.

This summary describes the RADSAFE concept and demonstrates the approach by applying it to the problem of modeling Single Event Upsets (SEUs) in a commercial 0.25 μm CMOS SRAM observed during ground-based testing.