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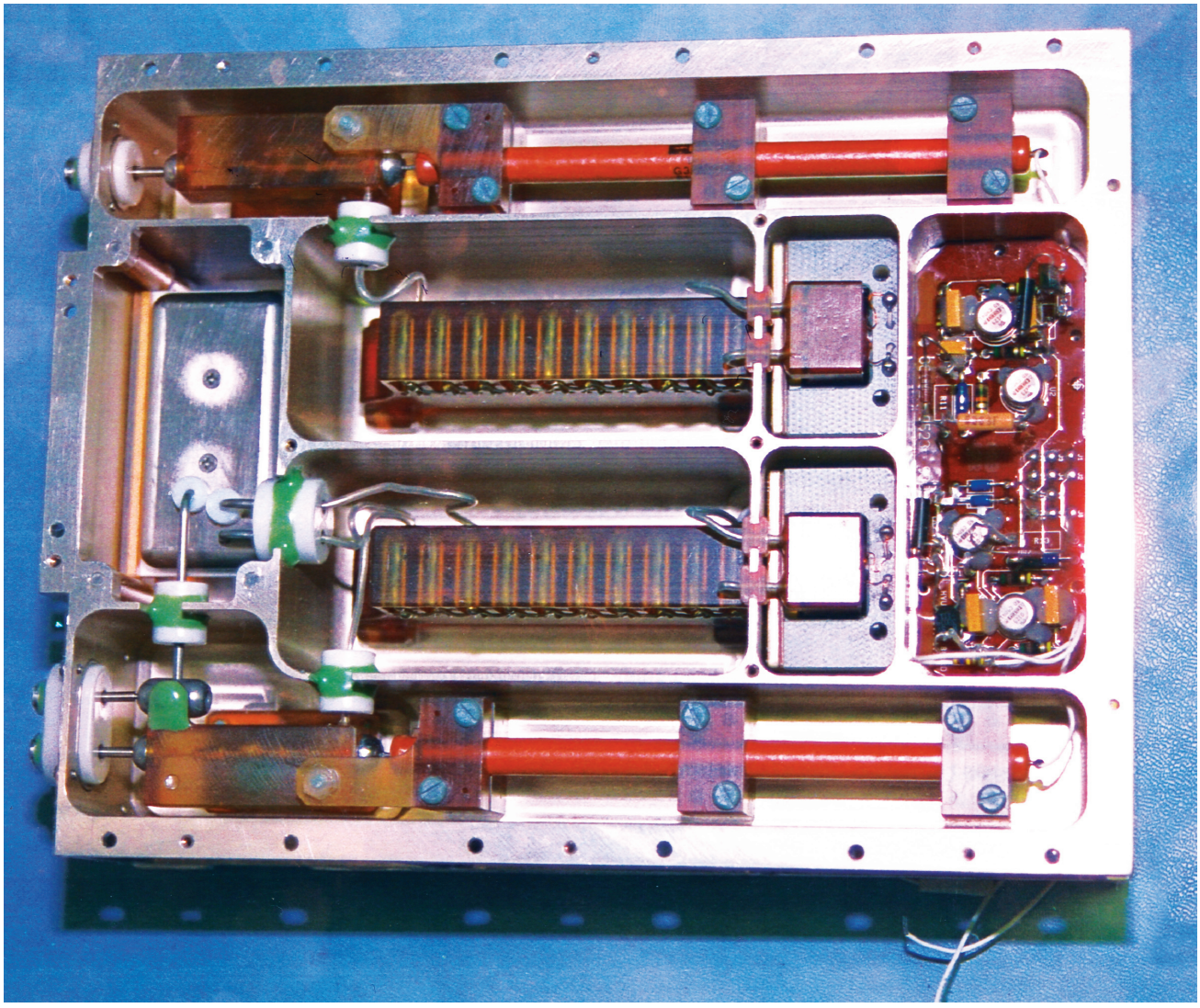
High Voltage Power Supply Design Guide for Space

Renate S. Bever, Arthur P. Ruitberg, Carl W. Kellenbenz, and Sandra M. Irish



July 2006

COVER CAPTION

Modular construction of the Cassini/Cassini Plasma Spectrometer (CAPS) power supply showing the combination of solid potted, conformal coated, and bare construction. The supply has both a +16 kV and –16 kV output and both are commandable from 0–16 kV. A +1.2 kV output floats on top of the commandable –16 kV output.

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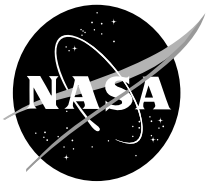

High Voltage Power Supply Design Guide for Space

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The authors wish to honor the memory of Mr. John L. Westrom, who initiated and inspired the engineering effort at NASA's Goddard Space Flight Center to design and build high voltage power supplies. The authors wish to acknowledge the efforts of, and express gratitude to, the many engineers, scientists, and technicians—especially Kenneth M. Young and Carroll Clatterbuck—who worked in high voltage power supply design and construction, for space use. The documentation of their experiences have helped, to a large degree, to make this High Voltage Power Supply Design Guide possible.

Appreciation is due to Dr. George Gloeckner and his team at the Space Physics Department at the University of Maryland, for supplying information on the CHEM/AMPTE High Voltage Power Supply.

A special thanks goes to Rogenia Burton-Pendergast who typed the manuscript and put it onto a CD, with great good spirit and much patience.

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PREFACE

Voltage breakdown continues to be a problem in high voltage power supplies that are constructed for use in the vacuum of space. The physics, and especially the electrical insulating properties, of gases, solids, and even liquids needs to be understood by electronic designers in order to prevent these breakdowns.

In 1975, a document was published by NASA, namely "Spacecraft High Voltage Power Supply Construction," by J.F. Sutton and J.E. Stern, NASA TN D-79, April 1975. This document is now out of print and the plates for the text were destroyed. It is with the idea of replacing and updating this former document that this present one has been written. Some of the basic physics tables and figures have been reproduced from the former document in the first few chapters. Obviously, the examples of power supplies are new.

The organization of this High Voltage Guide is such that each chapter has its own references at its end, before its appendices, rather than at the end of the entire book. There are more references listed as reading material than specifically referred to in a given chapter.

Throughout the book, and especially in Chapter 4, "High Voltage (HV) Parts," the mention of manufacturers' names is simply a report of the part's use by Goddard Space Flight Center and does not constitute a recommendation of one manufacturer over another.

EDITOR'S NOTE

This document was written and compiled over the course of more than a decade with different authors and researchers supplying data, verbiage, figures, and photographs. These and many other factors contribute to the complexity of this document. The factors include the length of the document itself, the original media in which much of the document components were supplied, and the different writing styles used by not only the authors of the document itself, but also the authors of the appendices. (A number of the appendices were previously published elsewhere, but have been included here to make it easier for readers to gain a complete understanding of the issues at hand.)

Because of these complexity issues, except for obvious typographical, grammatical, punctuation, or consistency errors, this document is being published *as submitted* by the authors. For example, nonstandard ways of depicting common symbology, such as "°K" for Kelvin instead of the standard "K," is being allowed in this document—at the authors' insistence—to avoid confusion with the K symbol being used elsewhere. In addition, because of the established conventions in this scientific discipline, both standard and metric units are used.

As mentioned above, the appendices in this document were previously published by various authors. The text of these appendices refers to the original figure or table numbers used in the original publication. To clarify numbering for the readers of this document and for those who wish to reference them, however, the editor has added unique sequential numbers in square brackets after each original number. As an example, in Chapter 3, there are two appendices labeled "Appendix I" and "Appendix II." Although each references a "Figure 1," the one in Appendix I would read "Fig. 1 [3.A.I.1]", while the one in Appendix II would read "Fig. 1 [3.A.II.1]".

When referring to these figures in future publications, please use the unique numbering scheme (i.e., Fig. 3.A.I.1, Fig. 3.A.II.1, etc.) in the square brackets, rather than the original numbers used in the text. Using the unique numbers will avoid confusion and ambiguity on the part of those people wanting to look at these figures at a later date.

Thank you.

TABLE OF CONTENTS

Chapter 1: General Information

I. Use of High Voltage Power Supplies, in Space

In space, high voltage bias is needed on the following types of instruments (most are DC biases):

- Vidicon Camera Tubes (IUE, –15 kV DC)
- Digicon Detectors (HRS on HST, –23 kV DC, 1% ripple)
- Image Intensifiers (FOC on HST, –26 kV DC also Ultraviolet Detector, +13 kV DC, 1% ripple)
- "Inch-Worm" piezoelectric mechanical devices (500 V DC)
- Deflection plates (1 V→10 kV steppers, 1% ripple, slew rate is ± 1 kV/ms)
- Mass Spectrometers
- Electronic Focusing Devices
- Photodetectors
- Photomultipliers (1.5–2.5 kV)
- Channeltrons (2→4 kV, <20 mV ripple)
- Spiratrons
- Particle Acceleration Devices, Electron Beam Ejectors
- Spark Chambers/Cloud Chambers (3–5 kV, 2% ripple)
- X-ray detectors (1–4 kV, <20 mV ripple)
- Gamma-ray detectors (2–6 kV, <50 mV ripple)
- Particle detectors in general, for protons, α and β rays (1–10 kV)
- Faraday Cup Modulator (150 V to 8 kV, 1% ripple, ± 10 kV/ms slew rate)

The above power supplies are for biasing purposes and usually are very high impedance supplies, capable of only delivering currents of the order of tens of microamperes or almost no power. Some of these devices are very noise-sensitive, e.g., x-ray detectors. The noise specifications must be supplied by the projects, e.g., no greater than 10 mV spikes.

A second class of need for high voltage power supplies are:

- Radar Technology
- Traveling Wave Tube Amplifiers, that is for TWTAs (communications satellites such as TDRSS)
- Klystrons/Magnetrons
- Laser Technology

Except for lasers, these are also DC supplies, drawing tens of milliamperes of current. Thus power is delivered, some of it being dissipated within the power supply, most of it in the device however. The heat generation thus becomes an additional problem, as to how to get rid of it. Noise sensitivity here is not critical.

The Cassini/CAPS power supply of ± 16 kV was commanded ON after several years of flight to planet Saturn, and it is performing well. Also, in orbit now are –26 kV power supplies on the Hubble Space Telescope (HST), and the –13 kV supply on IUE has had many years of life. Amazingly, more problems occur with supplies in the range up to 1.5 kV DC because designers do not take the high voltage problems seriously in the initial design. High voltage for space use means anything above 200 V, which is approximately the Paschen minimum voltage for *gaseous* breakdown.

II. Symptoms and Causes of High Voltage Failures in Space

Symptoms of failure are:

a. The performance of the power supply and the instrument is intermittent.
b. Data output from the instrument is "strange" that is, unexpected zeros and high spikes.
c. Performance degrades at high and low extremes of temperature or of high voltage or both.
d. More and more "noisiness" with time of usage.
e. The voltage and current output of the supply becomes erratic, varies wildly, and finally ends in zero output voltages or complete breakdown.

What are the most common causes of failure?

A. Marginal Electronic Design

This means that the electronic operation of the circuit depends too sensitively on a very narrow range of parts parameters. As soon as the circuit warms up, the parts parameters change and get outside the range where the circuit operates (e.g., HSP on ST—the high voltage transformers heated up a little and the current input rose above operating range—then the supply shut itself off). This is an example of the least common failure mode.

B. Electrical Insulation Problems

- Defect sites in dielectric solids, that is, voids and bubbles.
- Cracks in dielectric potting or in ceramics.
- Delaminations at interfaces between different materials and around parts.
- Presence of trapped gas at intermediate pressures, that is, between about 100 torr to 10^{-3} torr, that is, in the "Paschen minimum" range.
- Impurities inside dielectric solids, that is, metal flakes, etc.
- Contaminated, flawed surfaces.
- Thermal expansion causes mechanical stresses, which is due to differential thermal expansion of differing neighboring materials.
- Bad adhesion between neighboring materials causing delamination.
- Too high localized electric fields at sharp points on the outside of small diameter wires. Although only in small localities, that is where trouble starts.
- Bad geometries and too small spacing on average overall, causing too high electric fields, that is (>30 V/mil).
- Use of defective parts.
- Influx of streams of ionizing, high energy particles or radiation from cosmic bodies; or sometimes returning after circular path, originally ejected from the satellite itself.
- Choice of wrong insulating materials which have too low a dielectric strength or too low a volume resistivity or too low an arc resistance or do not machine well, that is, form microcracks during machining, or have too high a coefficient of thermal expansion compared to the other materials in contact with them.

The above causes are the most common causes of HV failures. As can be seen, this involves the knowledge of electric and physical properties of insulating solids and gases. Especially the understanding is important of *gaseous* behavior under electric fields and at varying pressures, all the way from atmospheric (760 torr) down to very high vacuum (10^{-12} torr) in order to grasp the *extra* problems of high voltage in space, over and above the problems on the ground.

It is generally accepted that above 200 V DC, high voltage practices and packaging need to be used in space. If, however, the flight path of the satellite or rocket carrying the electronics, instruments, and batteries is over the Earth's poles, the South Atlantic anomaly, or the "Radiation Belts"—all areas where there is a large concentration of energetic ions and electrons—then high voltage practices need to be used from as low as 100 V on up.

Chapter 2. General Background on Electrical Insulation

General Background on Electrical Insulation

Construction of high voltage power supplies for use in space requires an extensive knowledge of electrical insulation. Gaseous and solid insulation are of greatest interest for space, but not insulating liquids. These are omitted here. The behavior of gaseous discharges or gaseous breakdown in various degrees of vacuum (represented as pressures of so-and-so many millimeters of mercury, or torr) produces the extra problems of high voltage in space. Also, the small size and small weight imposed as a constraint on the designer of space high voltage power supplies adds to the extra problems over and above what one would have to solve if the supply was for use on the ground and at atmospheric pressure.

I. Gaseous Insulation

If one mounts two plane-parallel electrodes at the ends of a gas-filled tube, then the gas changes from being a good insulator to a conducting medium when a larger and larger potential difference is applied, in volts, between the electrodes. Or, one can talk about this in terms of applying higher and higher field strength, which is the potential difference divided by the length of the gas column between the electrodes, in volts/meter or in volts/mil (volts/meter = newton/coulomb, or force per unit charge).

This progression from insulator to conductor of a gas is pictured in Figure 2.1. The voltage axis is purposefully left blank because it depends numerically on pressure and electrode spacing and geometry. The theoretical analysis of the ionization of the gas, the Townsend coefficients, and the avalanche breakdown can be read elsewhere (see References), but the useful result is Paschen's Law which says that for any gas the breakdown voltage is a function of the product of the gas pressure p, times the electrode spacing d. The Paschen curves for various gases can be obtained experimentally, as in Figure 2.2, where the product $p\,d$ is plotted logarithmically on the x-axis. Or in Figure 2.3, all for air, a whole family of curves at various electrode spacings is plotted with the pressure in torr, given logarithmically on the x-axis and breakdown voltage logarithmically on the y-axis. One can see that for a 1 cm gap of air, breakdown at the atmospheric pressure of 760 torr would occur at about 30 kV, whereas at the pressure of 0.6 torr, it would require only about 300 V DC or AC peak. The part of the curve where breakdown is so easy is called the Paschen minimum, or the corona region because one can visually observe this breakdown as a colored glow (blue for air, orange-red for neon, etc.). Another way of looking at this is to realize that at high gas pressures or gas density, the mean free path of an electron between collisions is very short and the electron has gained too little energy to produce much ionization. At very low gas pressures, the mean free path is good and long, and an electron can pick up much kinetic energy, but it meets too few gas molecules to produce much of an avalanche of ions and electrons. But there is an optimum pressure in between where a great many charged particle pairs are produced and breakdown is easy. That is the Paschen minimum.

To summarize, one can see that at a product of $p\,d$ about 1 torr-cm, a minimum of about 250–300 V occurs in the Paschen curve and this, of course, varies slightly depending on gas composition, electrode shape, presence of cosmic ray fluxes, etc. By looking at Table 1 of Earth Atmosphere data, one can see that spacecraft instruments, which must operate while passing through altitudes of 30–65 km, are particularly prone to corona problems. But even higher up where the gas pressure is a "safe" 10^{-5} or 10^{-6} torr or even in deep space at 10^{-12} torr, the pressure ***within*** a high voltage power supply box ***within*** the spacecraft equipment compartment may well still be at 10^{-1} torr. The shielding ***box*** usually has very small venting gaps for the residual air and outgassing vapors to escape into the high vacuum of space. Thus, the pressure right at the high voltage soldering points and terminals within the box may well linger near the Paschen minimum for several days or even weeks after launch, and turn-on of the input power to the supply should be delayed. This is also the reason why the high voltage parts and all high voltage metal should be either solid potted or at least

coated with insulating resin, and why these resins must have extremely low outgassing and low vapor pressure. See references [26], [27], and [29].

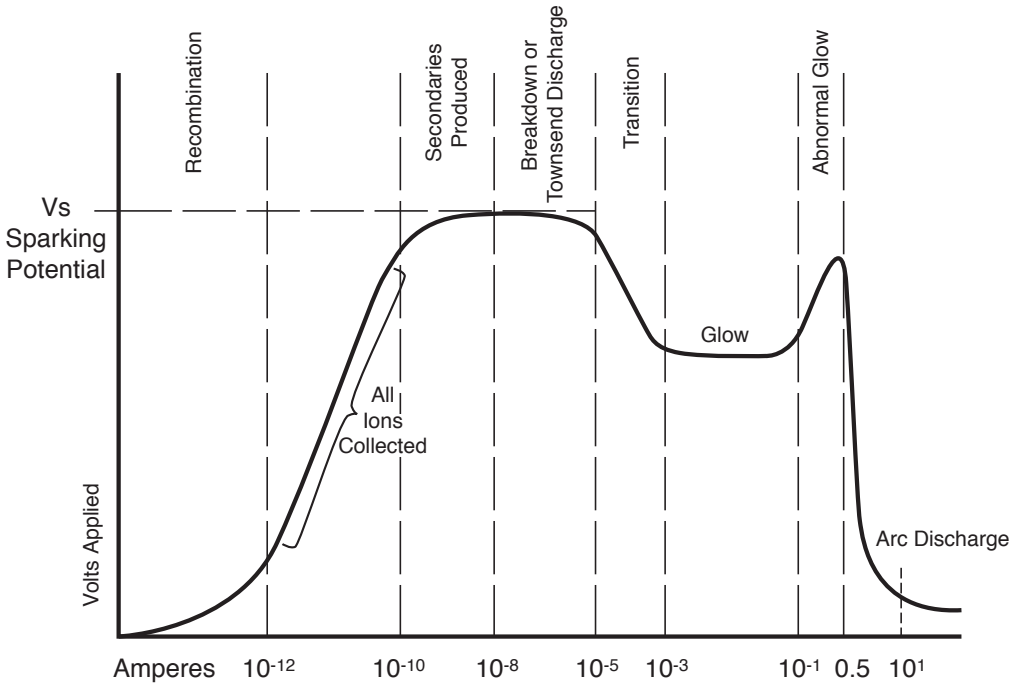


Figure 2.1. Gaseous discharge, Voltage vs. Current Characteristic, after Refs. [1], [23]

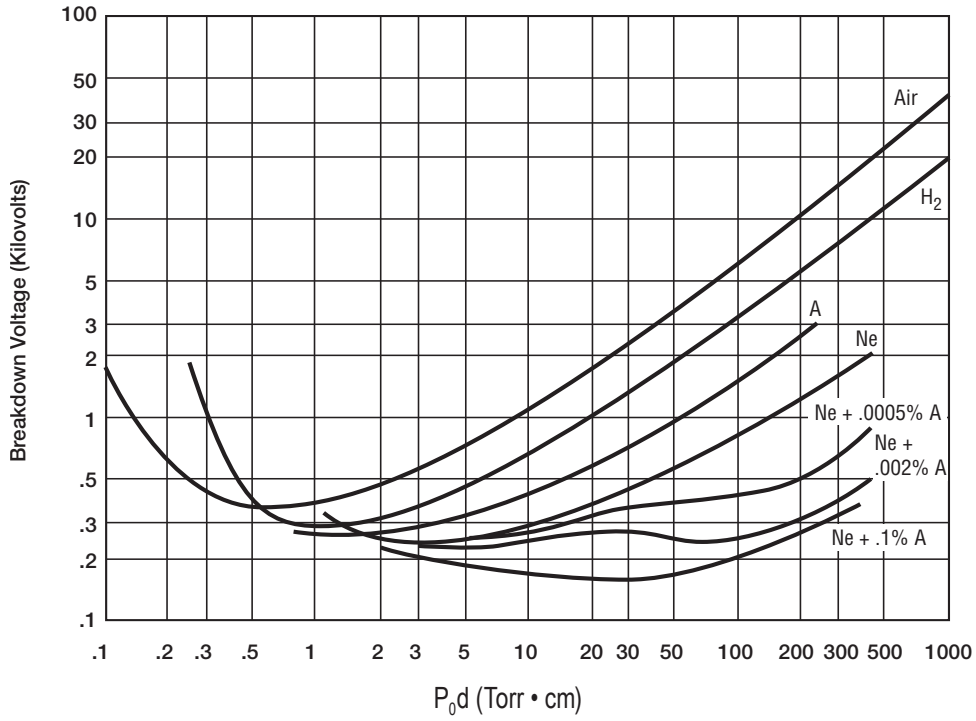


Figure 2.2. Typical Paschen curves for different gases; after Druyvesteyn and Penning (courtesy American Institute of Physics), Refs. [12], [13]

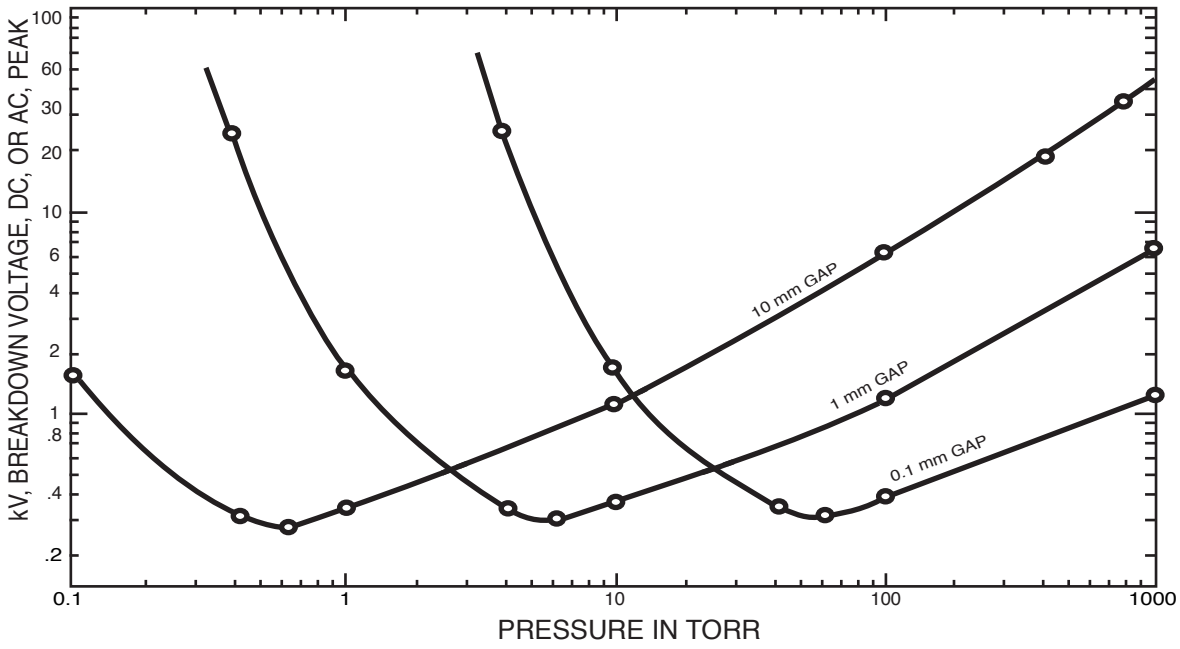


Figure 2.3. Paschen's original curves; breakdown voltage in air as a function of pressure (Iron Electrodes).

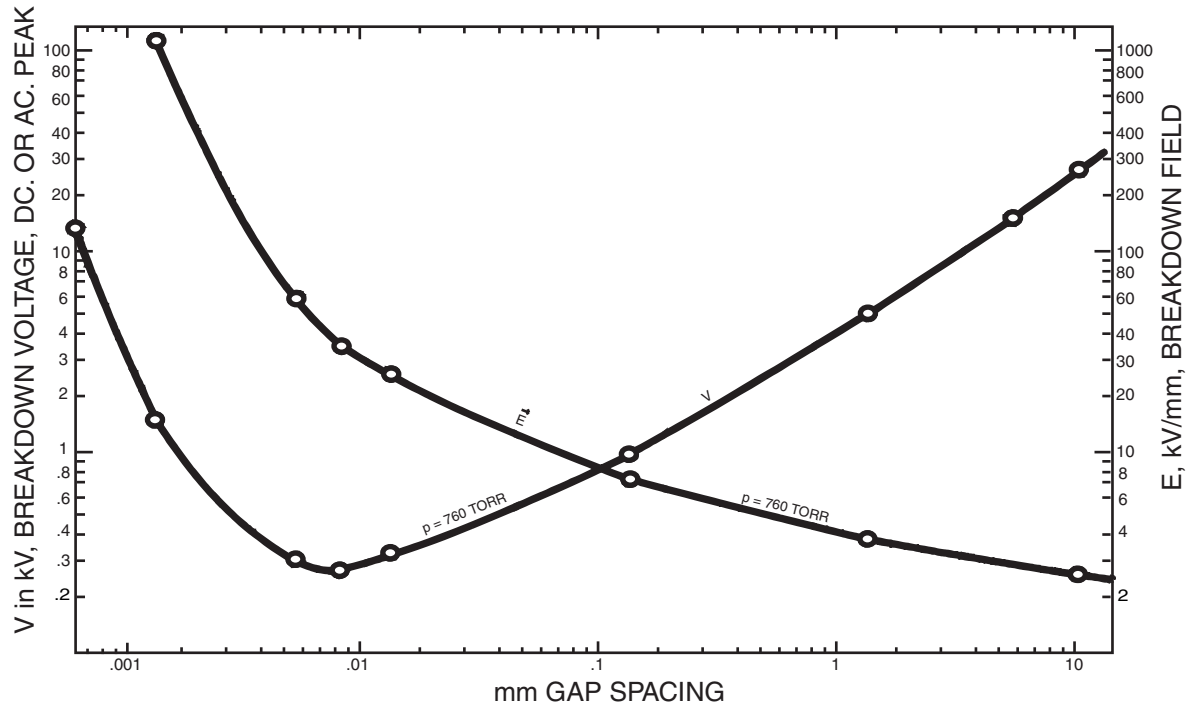


Figure 2.4. Paschen's curve, V; field strength curve, E. (Iron Electrodes); Ref [25].

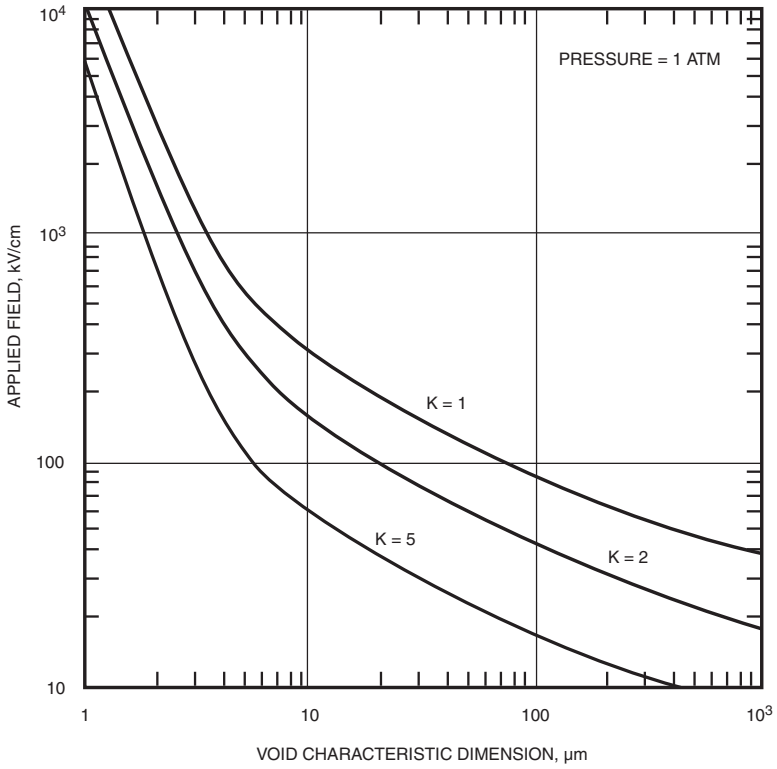


Figure 2.5. Corona inception stress versus void size, for a cylindrical void (©1975 IEEE), Ref. [25]. (Reprinted with permission from the Institute of Electrical and Electronics Engineers.)

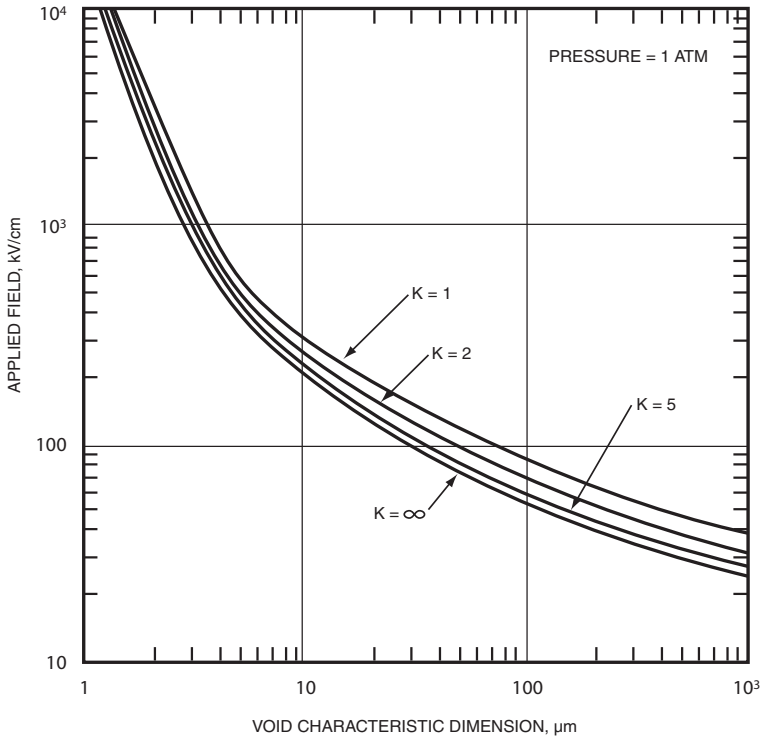


Figure 2.6. Corona inception stress over the insulation versus void size, for different dielectric constants. These curves are for a spherical void, ©1975 IEEE, Ref. [25]. (Reprinted with permission from the Institute of Electrical and Electronics Engineers.)

Table 2.1. Earth Atmosphere Data, from Ref. [6]

Altitude km above sea level	Pressure in mm Hg or torr	Mean Free Path of N_2 molecule, in cm	T °K for molecules of mean M=29 (from velocity calculations)
0	760	6.5×10^{-6}	
10	210	1.9×10^{-5}	
20	42	8.6×10^{-5}	210
30	9.5	4.2×10^{-4}	235
40	2.4	1.8×10^{-3}	260
50	0.75	6.1×10^{-3}	270
60	0.21	2.1×10^{-2}	260
70	5.4×10^{-2}	6.6×10^{-1}	210
80	1.0×10^{-2}	3.2×10^{-1}	190
90	1.9×10^{-3}	2.0	210
100	4.2×10^{-4}	10.0	240
110	1.2×10^{-4}	40	270
120	3.5×10^{-5}	150	330
130	1.5×10^{-5}	400	390
140	7×10^{-6}	1000	450
150	3×10^{-6}	2500	510
160	2×10^{-6}	5000	570

As an aside, the term “corona” is often understood to encompass all forms of low current gas discharge or glow discharge. In its strictest usage, corona applies to *partial* discharge transients or breakdown caused by high fields at one electrode, but no current bridges the total gap between the metal electrodes all the way.

The Paschen curve can be plotted, instead of volts on the *y*-axis, by putting field strength in kilovolts/millimeter instead, such as in Figure 2.4. One can also draw derived graphs such as Figures 2.5 and 2.6. These are for breakdown of bubbles or voids buried in a dielectric of dielectric constant K and of varying void size, to see at what externally applied field strength in the dielectric the bubble would break down and give a transient current or corona pulse.

The reader is reminded here that an electric field equal to voltage/spacing is only numerically correct for an electric field between plane parallel metal plates. If electrodes are spherical or cylindrical wires, then the fields are higher than that, and in fact increase significantly the closer one gets to the electrodes. For calculations *at the surfaces* of spherical or cylindrical conductors where the field is *maximum,* the formulae in Table 2.2 are supplied. At the surface of very tiny diameter wires or spheres, the field strength is extremely high, and therefore, a bubble buried near a sharp point or a tiny wire is very likely to break down.

Table 2.2. Maximum Field Strength, E, with a Potential Difference, U, Between the Electrodes, for Several Electrode Configurations (Refs. [12], [7]). Reprinted with permission by Phillips Research Institute.

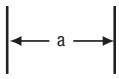
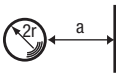
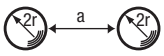
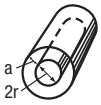
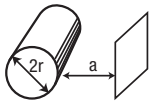
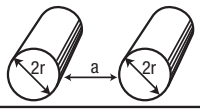
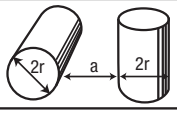
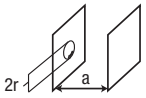
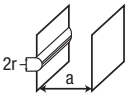
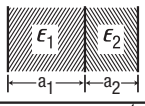
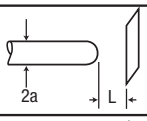
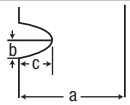
Configuration		Formula for E	Example
Two parallel plane plates		$\frac{U}{a}$	U = 100 kV, a = 2 cm, E = 50 kV/cm
Two concentric spheres		$\frac{U}{a} \cdot \frac{r+a}{r}$	U = 150 kV, r = 3cm, a = 2 cm, E = 125 kV/cm
Sphere and plane plates		$0.9\ \frac{U}{a} \cdot \frac{r+a}{r}$	U = 200 kV, r = 5 cm, a = 8 cm, E = 58.5 kV/cm
Two spheres at a distance from each other		$0.9\ \frac{U}{a} \cdot \frac{r+a/2}{r}$	U = 200 kV, r = 5 cm, a = 12 cm, E = 33 kV/cm
Two coaxial cylinders		$\frac{U}{2.3\ r\ \lg \frac{r+a}{r}}$	U = 100 kV, r = 5 cm, a = 7 cm, E = 22.9 kV/cm
Cylinders parallel to plane plate		$0.9\ \frac{U}{2.3\ r\ \lg \frac{r+a}{r}}$	U = 200 kV, r = 5 cm, a = 10 cm, E = 32.8 kV/cm
Two parallel cylinders		$0.9\ \frac{U/2}{2.3\ r\ \lg \frac{r+a/2}{r}}$	U = 150 kV, r = 6 cm, a = 20 cm, E = 11.5 kV/cm
Two perpendicular cylinders		$0.9\ \frac{U/2}{2.3\ r\ \lg \frac{r+a/2}{r}}$	U = 200 kV, r = 10 cm, a = 10 cm, E = 22.2 kV/cm
Hemisphere on one of two parallel plane plates		$\frac{3U}{a}$; (a>>r)	U = 100 kV, a = 10 cm, E = 30 kV/cm
Semicylinder on one of two parallel plane plates		$\frac{2U}{a}$; (a>>r)	U = 200 kV, a = 12 cm, E = 33.3 kV/cm
Two dielectrics between plane plates ($a_1 > a_2$)		$\frac{U\varepsilon_1}{a_1\varepsilon_2 + a_2\varepsilon_1}$	U=200 kV, ε_1 = 2, ε_2=4, a_1=6cm, a_2=5cm, E = 11.8 kV/cm
Point and plane $\frac{L}{a}=160$		$\frac{0.605\ U}{a}$	U = 1 kV, L = 160 cm, a = 1 cm, E = 605 volts/cm. Compare parallel plate capacitor with E = 6.25 volts/cm
Ellipsoidal boss on one of two parallel planes		$\frac{U}{a} \times \beta$ $\beta=[n(\coth^{-1}n - 1/n)(n^2-1)]^{-1}$ where $n=c(c^2-b^2)^{1/2}$	$\frac{c}{b} = 10, \beta \approx 50$

Table 2.3. Minimum Sparking Constants * At Paschen Minimum Pressures, Ref. [17]

GAS	V_b minimum volts	pd, mm Hgx cm	L/pd
Air	327	0.57	1.7×10^{-5}
A	137	0.9	1.1×10^{-5}
H_2	273	1.15	1.6×10^{-5}
He	156	4.0	0.74×10^{-5}
CO_2	420	0.5	1.2×10^{-5}
N_2	251	0.67	1.4×10^{-5}
N_2O	418	0.5	1.4×10^{-5}
O_2	450	0.7	
Na (vapor)	335	0.04	
SO_2	457	0.33	1.4×10^{-5}
H_2S	414	0.6	1.0×10^{-5}

* J.J. Thomson & G.P. Thomson, “Conduction of Electricity thru Gases” Vol. 2, 1933

V_b = Spark Breakdown Voltage
p = Pressure
d = Gap Length
L = Kinetic Theory mean free path at 760 mm Hg.

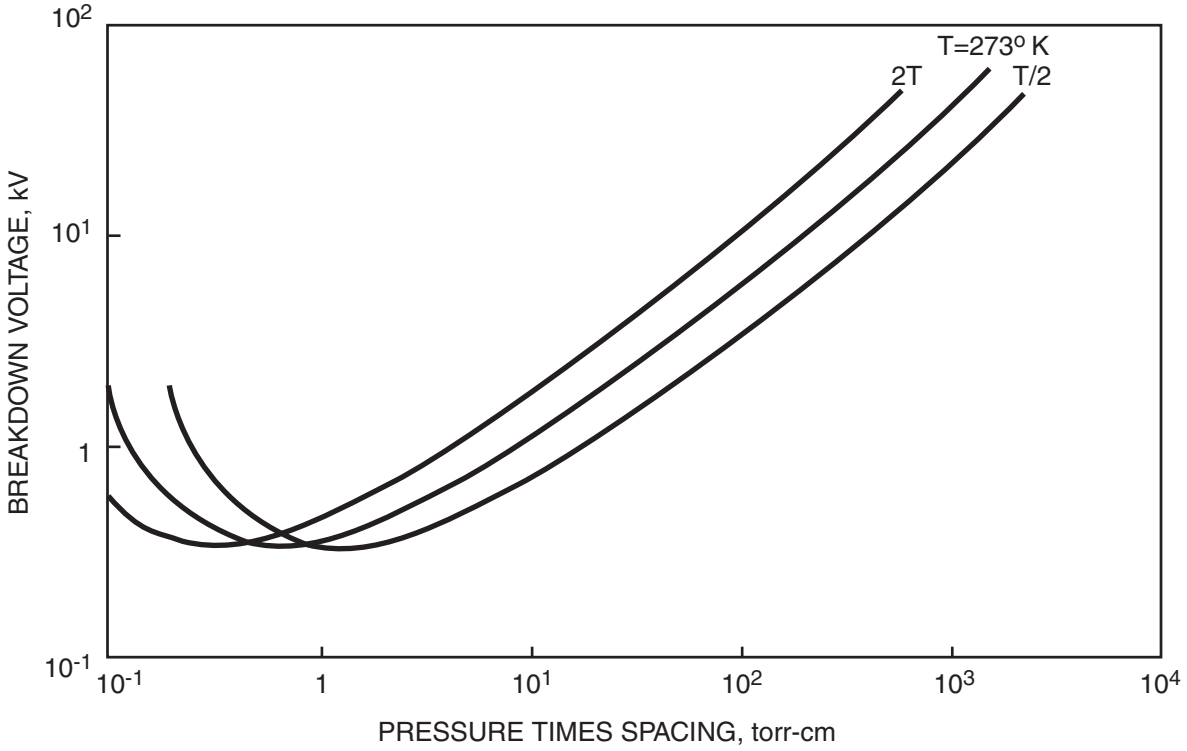


Figure 2.7. Effect of temperature on Paschen curve, Ref. [1].

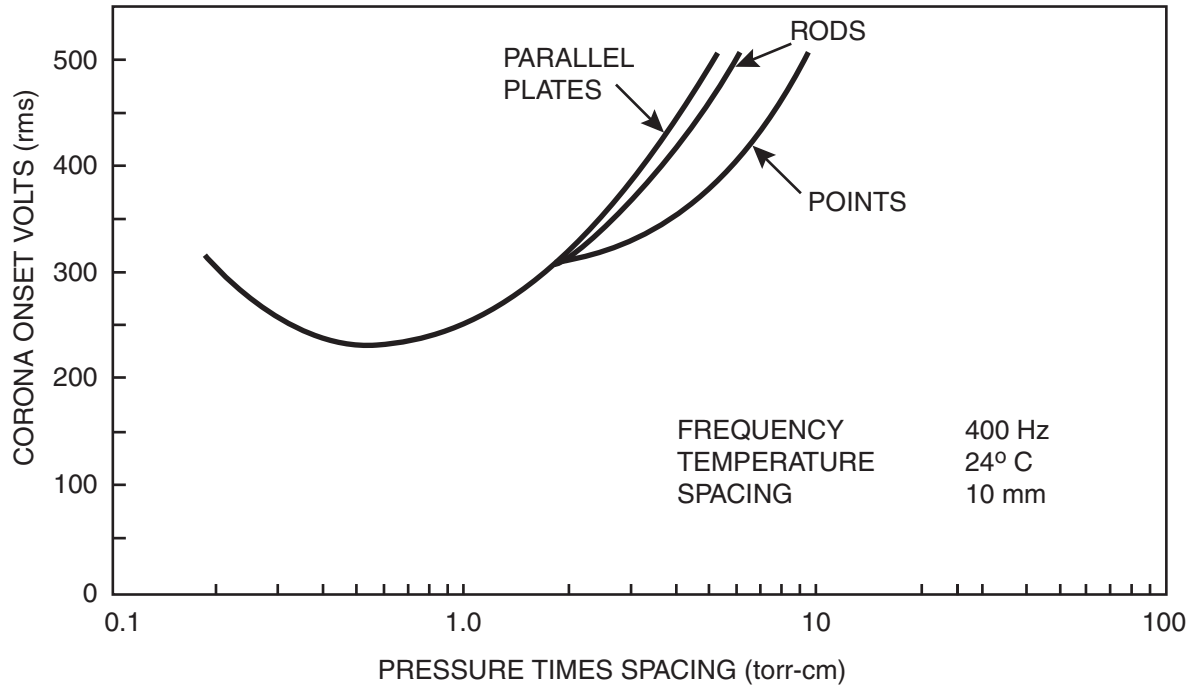


Figure 2.8. Effect of electrode geometry on breakdown characteristic in air, Ref. [1].

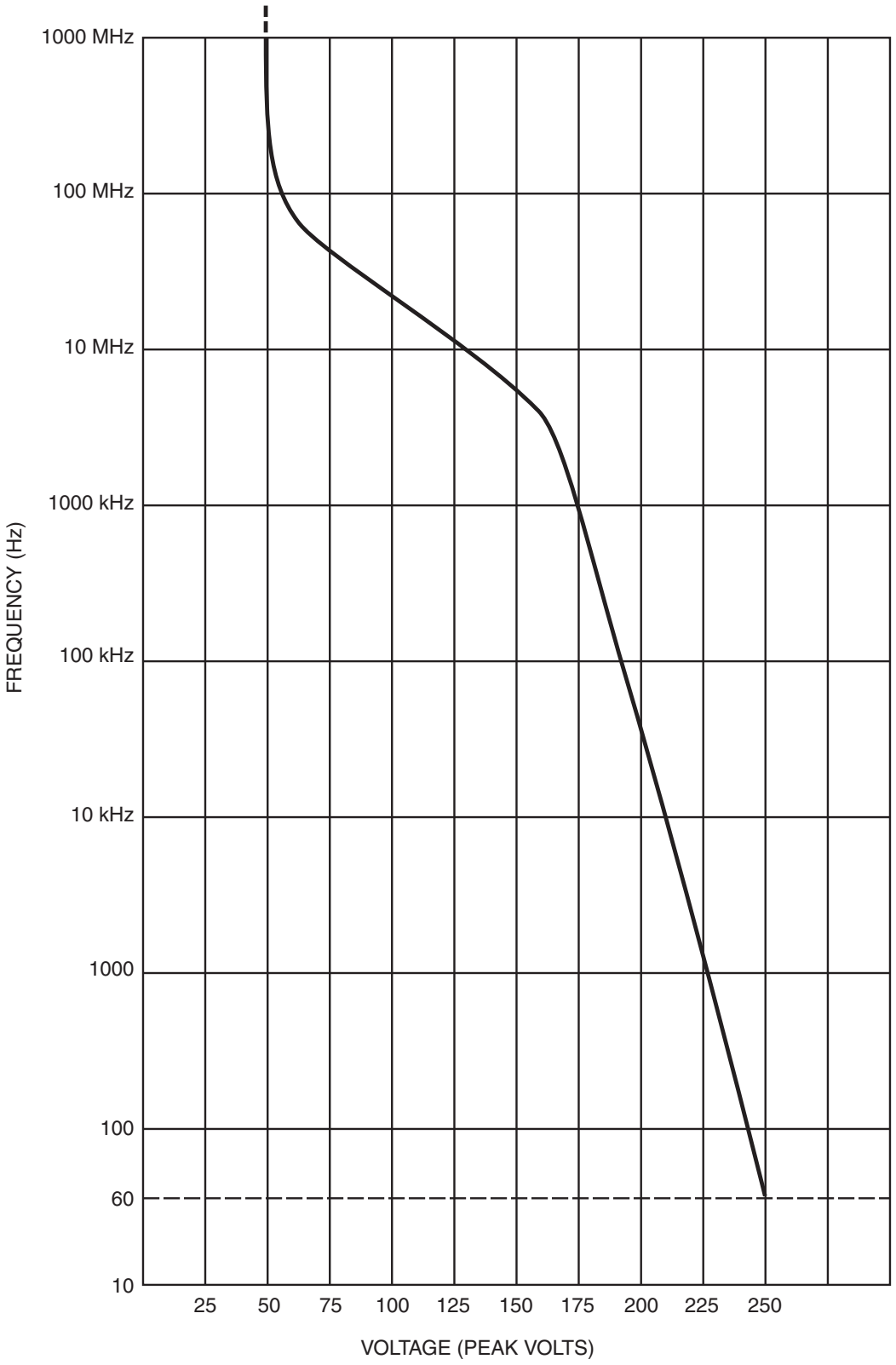


Figure 2.9. Lower voltage breakdown limit or Paschen minimum vs. frequency, (air), Refs. [1], [30], [31].

Another useful table in terms of the Paschen minimum is Table 2.3, which shows that the minimum occurs at different voltages for different gases; for helium it is at 156 V as compared to air where it occurs at 327 V.

There are many other perturbations on the basic Paschen curves. For instance, at a particular pressure, the breakdown voltage depends very much on what type of metal the electrodes are made of, e.g., Breakdown volts for copper electrodes, 1 mm apart is 37 kV, but for steel it is 120 kV, according to Ref [9].

Effects of temperature and of electrode geometry are shown in Figures 2.7 and 2.8. Figure 2.9, from the Jet Propulsion Lab documents in references [30] and [31], shows that the Paschen minimum voltage depends on the frequency of the applied voltage in the case of AC. Apparently, the higher the AC frequency above 60 Hz, the lower the Paschen minimum.

Another very important influence on breakdown is whether a dielectric solid surface bridges the gap between the electrodes, in other words, gas/solid interface effects. Water vapor absorbed at the dielectric surface can drastically lower the gas breakdown near the surface. Also, slow development of conductive paths or tracks can lead to permanent short circuiting of the high voltage. Table 2.4 is a listing of the arc resistances (in seconds) and other characteristics of some materials commonly used in fabrication of electronic devices.

A. Pressurization and Electronegative Gases

This paragraph is quoted from Ref. [1]:

"Normally, high voltage power supplies employed on spacecraft take advantage of the high values of breakdown voltage V_b available at low pressures. It is also possible to take advantage of the high V_b values at the other end of the Paschen curve by pressurization. For example, as shown in Figure 2.10, it is possible to double V_b by pressurization to ~350 kN/m^2 (~50 psig) with air or CO_2 or N_2. A better approach is the use of an electronegative gas, especially SF_6. Molecules of SF_6 readily capture electrons and form heavy negative ions with much lower mobility than the electrons. In addition SF_6 is stable below 423°K (150°C), is nontoxic, and does not burn. Figures 2.11 and 2.12 illustrate the improvement in V_b with SF_6 as in [Ref 14]." A 100 kV power supply has been successfully designed using pressurization with SF_6 for a *Sounding Rocket* experiment in the early 1970s, by F. Scherb, University of Iowa. He followed design practices developed for Van de Graaf generators."

B. Pressure Units

For ease of calculations or comparisons of graphs from different sources, the equivalences of Pressure Units are printed below:

1 atm = 760 mm Hg = 760 torr = 1.0133 bar = 14.696 lb/in^2 (psig)
= 1.0133×10^6 dyn/cm^2

1 dyn/cm^2 = 10^{-1} N/m^2 = 10^{-1} Pa

1 atm = 1.0133×10^5 Pa

1 bar = 0.987 atm = 14.50 lb/sq inch = 1.00×10^6 dyn/cm^2

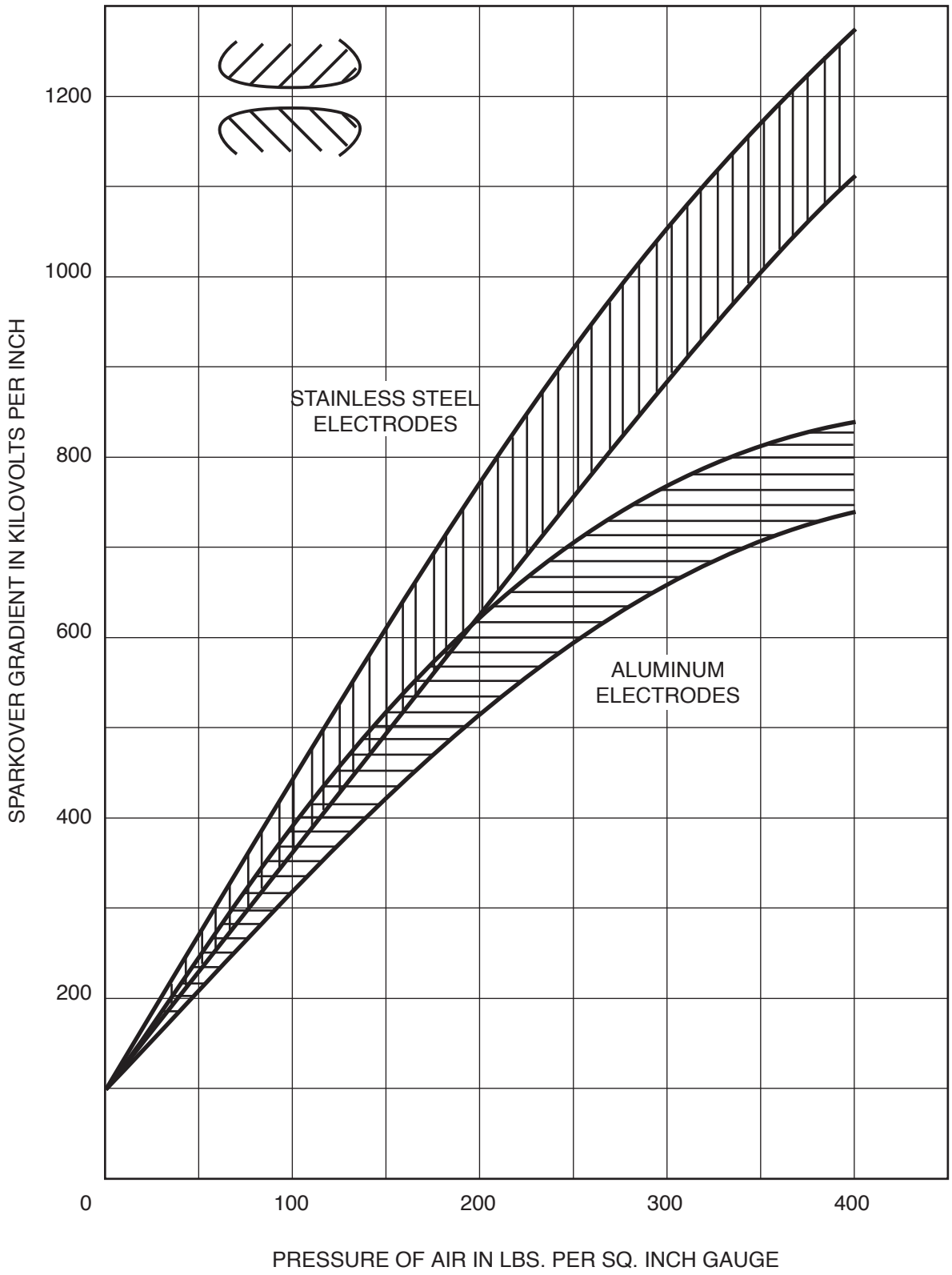


Figure 2.10. Insulating strength in compressed air with stainless steel and with aluminum electrodes producing uniform fields over ¼-, ½- and ¾- gaps, Ref [10]. (Courtesy of American Institute of Electrical Engineers.)

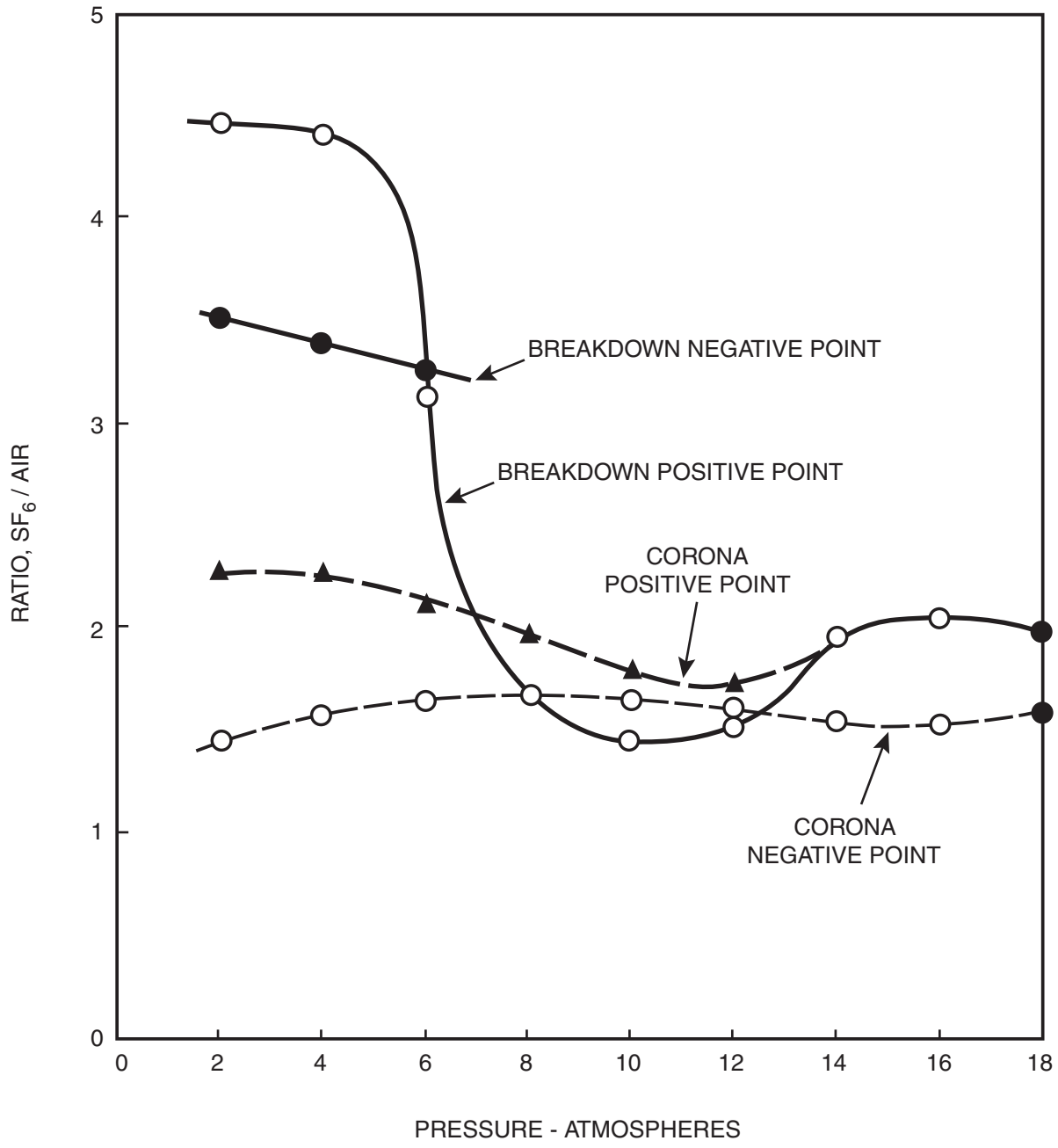


Figure 2.11. Ratio of corona and breakdown voltage for air and SF_6 as a function of testing conditions in nonuniform fields, Refs. [1], [14].

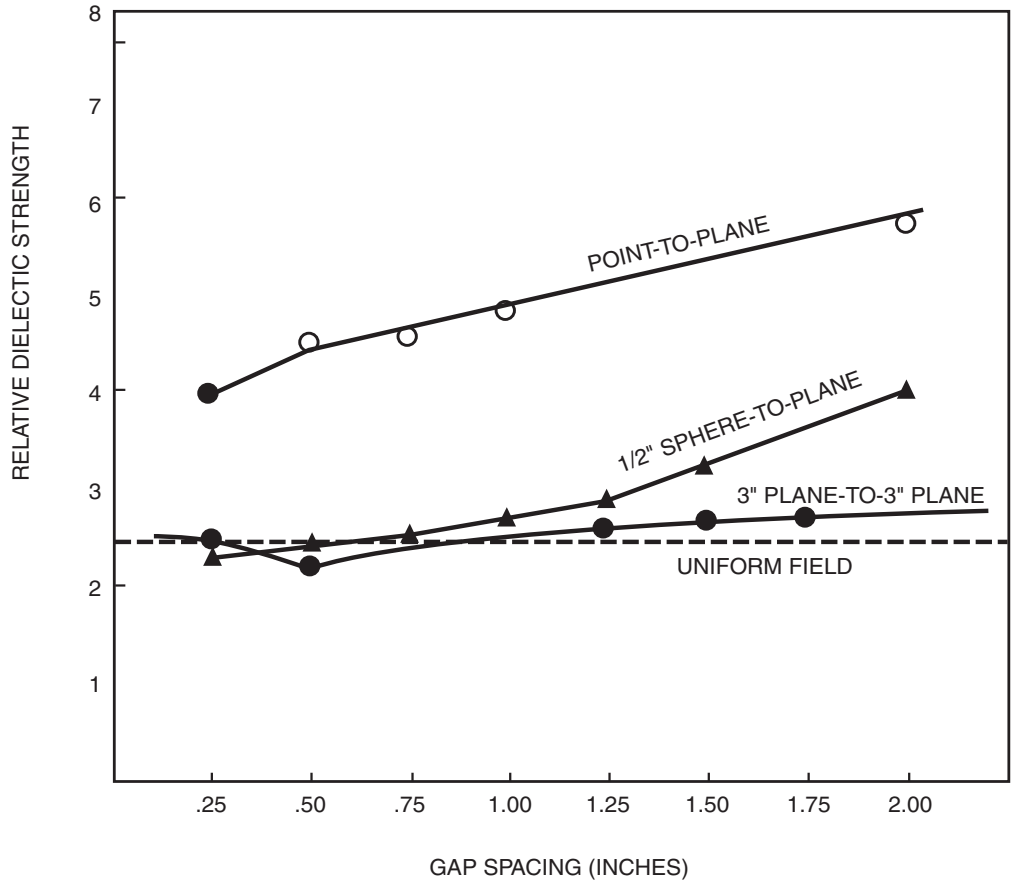


Figure 2.12. 60 Hz relative strength of SF_6 to dry air as a function of configuration and spacing of electrodes. Gases at 25°C and atmospheric pressure, Refs. [1], [14].

II. Solid Insulation

This summary of solid insulation and its breakdown is divided into the following subheadings: General, Intrinsic Breakdown, Corona Degradation or Erosion Breakdown, Thermal Breakdown, Surface Flash-Over, Thermomechanical Crack Propagation, Mechanical Breakdown (other than due to thermal stresses).

A. General

One can categorize solid insulation into three classes: organic (from living organisms), inorganic materials, and synthetic polymers.

The most useful of the above are inorganic materials and the synthetic polymers. Among the latter are the thermoplastics which melt in the range of 100–120°C and are flexible enough to be molded and extruded and are used for cable insulation. Thermosetting plastics cure upon heating and develop considerable mechanical strength and hardness. High voltage potting and coating compounds belong in this category (later chapter). The most obvious desirable characteristics of solid insulation are (1) high dielectric strength in volts per millimeter (V/mm), (2) high resistivity, (3) low power factor to reduce heating effects. Table 2.4 gives some of these electrical characteristics. The arc resistance (measured in seconds) is also given. This is important because "slithering" surface breakdown occurs much more often than puncture through the bulk of an insulating material. Machinability is good for epoxies, Ultem 1000 by GE Plastics and for Vespel, but poor for Noryl, a polyurethane (EN-265).

Table 2.4. Dielectric strength and arc resistance for selected insulation materials suitable for molding, extrusion, or casting,* Ref. [1].

Material	Arc Resistance (seconds)	Dielectric Strength (volts per mil)	Volume Resistivity Ω - cm	Dielectric Constant
Acetal resin copolymer	240	500-2100	10^{14}	
Acetal resin homepolymer	129-240 (burns)	500-1210	$1–6x10^{14}$	
Acrylic resins	no tracks	400-500	$2x10^{16}$	
Acylonitril Butadiene-Styrene	71-82	310-460	10^{16}	
Alkyd molding compound	180+	375	10^{14}	5.8-6.2
Cellulose acetate	50-310	230-365	$10^{10}–10^{14}$	3.5-4.0
Cellulose acetate butyrate	unknown	250-400	$10^{10}–10^{15}$	3.6-6.4
Chlorinated Polyether	unknown	400	10^{15}	
Ethyl cellulose	60-80	800	$10^{12}–10^{15}$	
Delrin	125-190	400	$10^{15}–10^{16}$	2.7-3.7
Deallyl phthalates	105-140	350-400	$3.9x10^{12}–1.8x10^{16}$	6.2
Expoxies	45-300	300-550	$10^{12}–10^{17}$	3.3-5.5
Ethylene	unknown	525-550	$10^{8}–10^{9}$	
Fluorinated ethylene and propylene (copolymer)	>300	500-600	$>2x10^{18}$	
Kel–F	>360	~500-1000	$2.5–4x10^{16}$	
Melamine with glass fibers	180	170	10^{11}	
Mica–glass bonded	240-300+	350-400	$10^{12}–10^{17}$	
Neoprene	unknown	150-600	10^{11}	
Nylons	130-140	342-470	$1.5x10^{11}–4x10^{14}$	3.9-7.6
Nylons with glass fibers	92-148	400-580	$3.0–5.5x10^{14}$	
Phenolic molding compound	tracks	300-400	$10^{11}–10^{12}$	
Phenolic molding compound with glass fibers	0.4 to 150	100-450		
Oxide Resins	unknown	500-550	10^{17}	
Phenylene oxide resins with glass fibers	70-120	1020	10^{17}	
Polycarbonate	120	400	$2–1x10^{16}$	3.1
Polychlor otrifluoroethylene	>360	530	$1.2x10^{18}$	
Polyethylene, irradiated	unknown	2500	$>10^{15}$	2.25-3.2
Polimides	230	560	$10^{16}–10^{17}$	
H film (5 mil)	183 tracks	3600	10^{18}	
Polypropylene	unknown	750-800	$>10^{16}$	
Polypropylene with glass fibers	73-77	317-475	$1.7x10^{16}$	
Polystyrene (heat resistant)	60-135	400-600	$10^{16}–10^{17}$	
Polysulfones	122	425	10^{16}	
Polyetrfluoroethylene	>300	480	$>10^{18}$	
Polyvinyl chloride (Flexible)	unknown	250-800	$10^{11}–10^{14}$	12.0
Polyvinyl chloride (Rigid)	60-80	425-1300	$>10^{16}$	2.4
Polyvinylidene fluoride	>50	260-1280	$2x10^{14}$	
Silicon, Mineral filled	230	390	$5x10^{13}$	4.8
Styrenes with glass fibers	28-41	354-424	$3.2-3.7x10^{16}$	
Ultem 1000, GE	unknown	830	$6x10^{17}$	3.1
Urethanes	unknown	6.7-7.5 (60 Hz)	$2x10^{11}$	
Viton, fluoroelastomer	unknown	500	$2x10^{13}$	
Vespel	230	400	$10^{16}–10^{17}$	3.0-3.5

* These values are obtained under standard test conditions and may not be obtained in engineering applications.

B. Intrinsic Breakdown Strength

If one were to analyze the binding energies of electrons and spacings of ions in a perfect crystalline lattice, or of a polymer chain of an insulating solid, and calculate the electric fields necessary to tear electrons out of this lattice, one would calculate of the order of 1 to 30 MV/cm (0.01 to 0.3 V/Å) or (2,500 to 75,000 V/mil). This inherent strength is a bulk property, and since it is dependent only on chemical composition and dielectric properties of the perfect material, it is called its intrinsic electric strength. It is more commonly measured in the laboratory, but only under carefully controlled conditions and especially prepared electrodes: (1) making a specimen with spherical recesses on both sides and depositing electrodes directly onto material by evaporation, then submerging the entire specimen in a dielectric liquid; (2) making thin slabs of the material and placing them between 1" spheres in a dielectric liquid; (3) using two needles of a known radius of curvature at the end and known separation, and then casting resin or solid potting the entire assembly. The dielectric fluid of immersion in (1) and (2) should have a dielectric constant greater than the solid to be measured. The intrinsic strength can also be calculated from various quantum mechanical theoretical formulae which appear in texts such as O'Dwyer, Ref. [16].

Practical electrical breakdown strengths found in actual insulation systems where the special precautions above are *not* taken are much lower, however, than above. Practical breakdown strengths are more around 200 kV/cm (500 V/mil) and so it must be concluded that practical insulation systems fail due to processes other than freeing electrons or ions from the lattice by pure electrical overstress. Some of these processes are briefly presented below.

C. Corona Degradation or Chemical Erosion Breakdown

All *real* insulation has imperfections. These are most often gas filled cavities or voids left in the insulation during manufacturing. The electric field, in disc shaped gaseous voids in a dielectric, is enhanced by the ratio (K dielectric/K gas) during AC applied voltage or during ramp-up of DC voltages. The letter K here stands for dielectric constant. Partial discharges, also called "corona discharges," will occur across the gaseous void when its peak electric stress equals the breakdown voltage of the gas. The partial discharges will deliver energy to the inside of the cavity wall where they impinge and will gradually cause chemical deterioration of the wall. The problem is especially serious with AC applied voltages where the discharges repeat every half cycle. In fact, the erosion upon AC applied voltage and in those geometries which give rise to nonuniform fields, advances in channels that are branched. This is called "electrical treeing." A continuous channel finally reaches from metallic electrode to electrode causing catastrophic breakdown. The important subject of partial discharge is treated separately in a later chapter.

Above, we have just discussed the case of an air-void in solid dielectric. The reverse is a disc-shaped solid in a gaseous gap and the voltage distribution is again governed by the dielectric constants K of the two materials. The voltage across the air space (where d is the thickness) is

$$V_{\text{Air}} = V_{\text{Total}} \bullet \frac{1}{1 + \dfrac{K_{\text{Air}} \bullet d_{\text{Solid}}}{K_{\text{Solid}} \bullet d_{\text{Air}}}}$$

This works out to yield an increase in average electric stress across the air gap, and one has to be sure that it can still withstand the full voltage at the reduced thickness after the solid disc is inserted.

Practical dielectric strength measurements show that, in volts/mil, the dielectric strength decreases with increasing thickness d as roughly $1/\sqrt{d}$, rather than staying constant. This can be explained on the basis that the larger the thickness or volume of the dielectric, the greater the probability of flaws and bubbles and inhomogeneities. Thus, the practical dielectric strength is lower, and this further reinforces the idea that processes other than intrinsic ones cause the failure. Figures 2.13 and 2.14 illustrate this point.

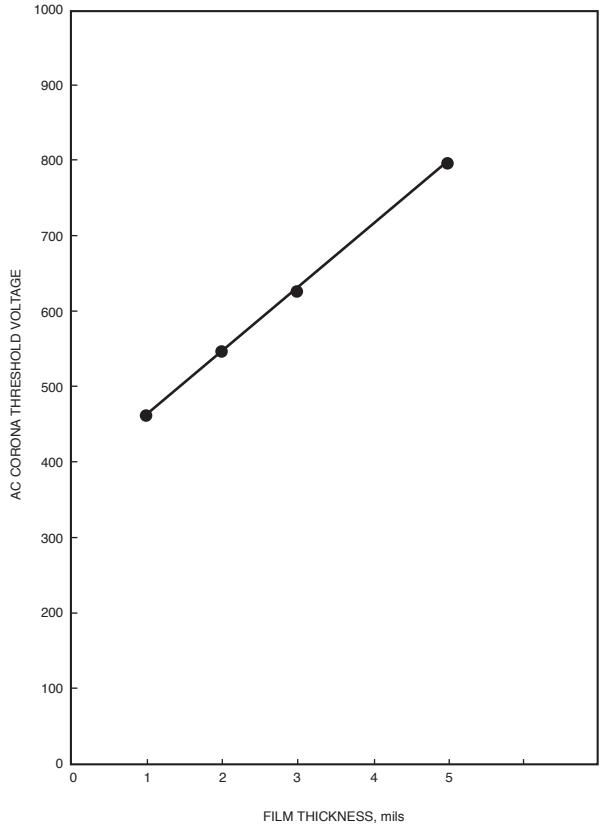


Figure 2.13. Dupont Kapton H-film corona threshold voltage vs. film thickness, Ref. [1].

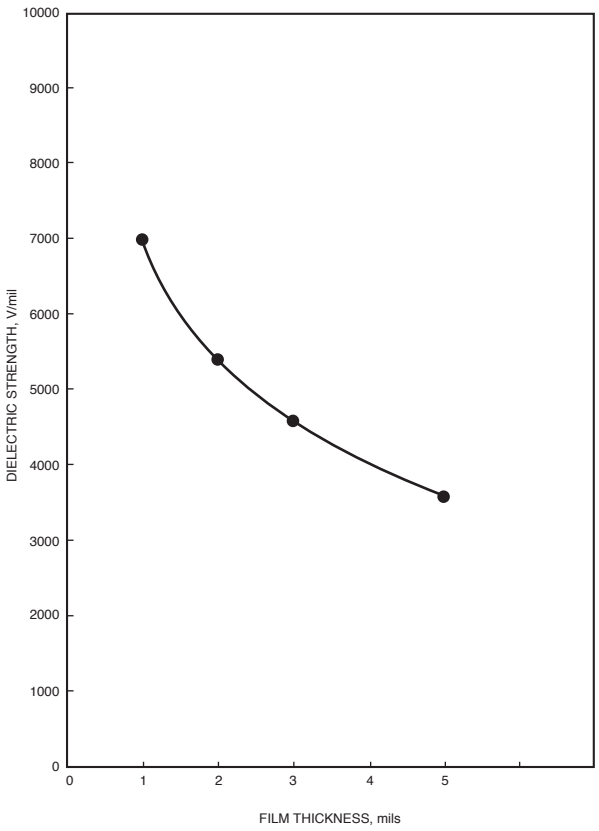


Figure 2.14. Dupont Kapton H-film dielectric strength vs. film thickness, Ref. [1].

D. Thermal Breakdown

Another very important practical mechanism is thermal breakdown. DC applied voltages cause small conduction currents to flow in a real insulator. This current flow causes localized heating created by collision of the electrons with the lattice and are the normal I^2R losses. This becomes heat, or, upon applied AC voltage, V_{rms}, at angular frequency ω, the power absorbed by the insulator is $(1/2\ \omega\ CV^2_{rms}\ \tan\ \partial)W$, where ∂ is the phase angle between applied voltage and the capacitative voltage drop of a C-R parallel equivalent network of the piece of insulation. This power dissipation under AC is usually greater than upon DC applied voltage, just due to the molecular dipole oscillations, in addition to that caused by partial discharges. The energy losses again become heat. The heating will cause general or localized temperature increases of the dielectric. But volume resistivity and dielectric strength generally decrease with increasing temperature as shown in Figures 2.15 and 2.16 respectively.

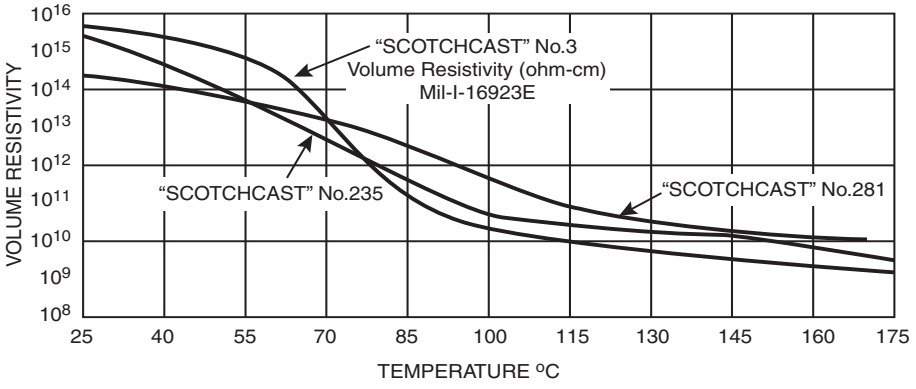


Figure 2.15. Volume resistivity vs. temperature for three encapsulant materials, Ref. [1].

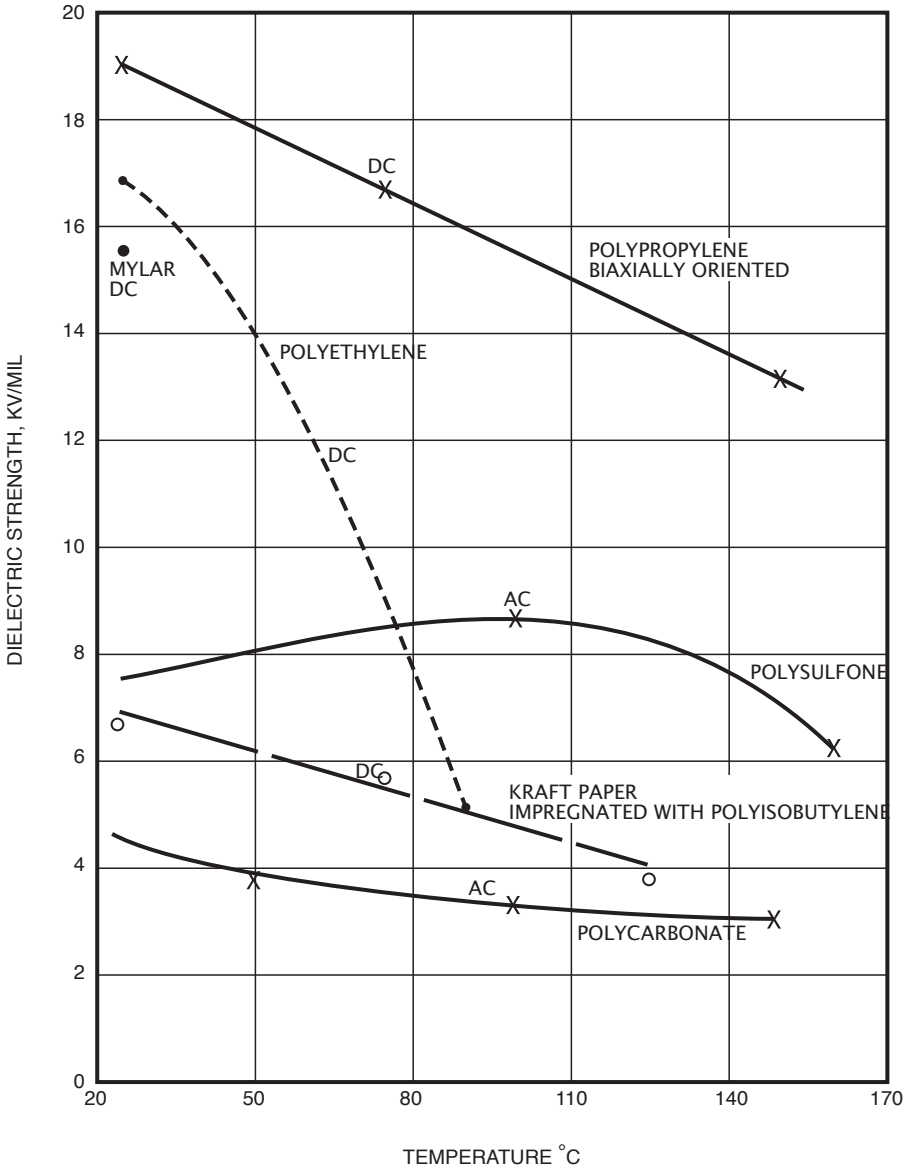


Figure 2.16. Temperature dependence of intrinsic dielectric strength, Ref. [8].

Because the heat developed cannot get away because of the generally low thermal conductivity of electrical insulation, then this whole scenario leads to thermal runaway. The fundamental differential equation of thermal breakdown is

$$C_v \frac{dT}{dt} - \nabla \bullet (c \text{ grad } T) = 6E^2,$$

where C_v= specific heat/volume, T = absolute temperature, t = time, c = thermal conductivity, 6 = electrical conductivity, and E = electrical field strength.

The 6 and c *are* functions of temperature as stated above. Numerical solutions show that there exists a critical field strength F_m for which the temperature of the hottest part of the dielectric asymptotically approaches some temperature T_m with time. For field strengths $>F_m$, the temperature reaches T_m in a finite time and then runs away without limit and causes breakdown, while for field strengths $<F_m$ the temperature rises to some value and stays there without runaway or breakdown. J.J. O'Dwyer [Ref. 16] discusses thermal breakdown in great detail.

E. Surface Flash-Over

The withstand voltage of a material to flash-over along its surface is significantly lower than breakdown through its bulk. This, combined with the fact that metallic print patterns or printed circuit trails end in sharp edges and therefore cause high electric fields across the supporting insulator, makes surface flash-over or surface creepage or tracking a very common mode of failure. Surface contamination and moisture contribute. Practical design stresses between trails are limited to 12 kV/cm (30 V/mil) and must not be allowed to be higher.

F. Thermomechanical Crack Propagation

Again, cast and extruded polymers are not perfect. Minute cracks that are present due to shrinkage or due to an attempt to confine the polymer on all sides, may grow with time once they are started due to relatively benign temperature changes. In addition, these cracks may by chance be present in regions of high electric fields; therefore, partial discharges may occur in them. Thus finally a metal to metal catastrophic failure may develop from a small crack. Bad adhesion between cast resins and circuit components embedded therein is also a type of crack (later chapter).

G. Mechanical Breakdown (other than thermally caused)

A particular type of mechanical breakdown is failure due to mechanical overstress of the solid, produced by electrically caused forces. An example is piezoelectric shear stresses which causes failure in thick discs of $BaTiO_3$ ceramic capacitors of very high dielectric constants (X7R and especially Z5U formulation).

III. Liquid Insulation

The insulating liquids have not been used in High Voltage power supplies, for space flight. Thus, discussion of them is essentially omitted other than to say that they are convenient for laboratory use. Especially in Partial Discharge testing at atmospheric pressure, the fluorocarbon liquids, such as FC-40 and FC-43 by the 3M company are particularly useful because they leave no residue on the test object immersed in them. For this reason, FC-40 and FC-43 are superior to insulating oils.

IV. Turn-On of High Voltage in Orbit

The underlying principle for the Turn-On procedure in orbit is a calculation or intelligent guess as to how long a time it takes for the gas pressure *inside* the HV power supply shielding box, and *inside* the HV instrument, to fall safely to at least below 10^{-3} torr. In other words, although the outer space pressure may be 10^{-10} torr as soon as one is in orbit, the pressure inside the boxes inside the spacecraft may still be hung up at 10^{-1} torr or so; this is because below 10^{-1} torr or so, the molecular flow of remnant molecules through the small vent holes and gaps between boxes and their lids is quite slow. Meantime, the materials outgas and supply more gas. References, especially to articles by Dr. J.J. Scialdone, on this topic, are given at the end of this chapter. Some previous experiences and rules of thumb folllow:

(1) If the power supply is bare, and the voltage is very high, such as was the case on OPEN at –30 kV DC, then waiting 4 weeks is recommended.

(2) If the power supply is only conformally coated/staked, then one should wait at least 2 weeks, preferably longer.

(3) If (a) the power supply is solid potted, and (b) if the interface to the instrument is completely insulated against the environment, and (c) if the instrument itself is vented properly and can withstand corona, then turn-on can be immediate. If (a), (b), and (c) are not so, then one must wait at least 2 weeks.

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Chapter 3. High Voltage Packaging for Space: Potting or Coating or Bare

General

There are three ways of packaging high voltage assemblies in power supplies and in instruments: (1) solid potting/encapsulating, (2) conformal coating, and (3) completely bare. Design at an early stage must take into account which way of packaging will be used. Table 3.1 below lists some of the advantages and disadvantages of each approach.

Table 3.1. Advantages and disadvantages of packaging modes.

Mode	Advantages	Disadvantages	Examples
Solid Potting Entire voltage range:	a) Protects HV portion against moisture and contamination. b) Allows HV to be energized while going through Corona Region. c) Electric field is weak at surface of potting because of great thickness. d) Rugged support for parts. e) Cushions against vibration.	a) Slows down circuit response time. b) Heavy. c) Differential thermal stresses between potting and embedded parts can cause cracks and delaminations.	IUE tubes FOC tubes Power supplies for FOC, HRS, HSP; Almost all power supplies done at GSFC for HV.
Conformal Coating Usually up to 3 kV:	a) Fast circuit response. b) Saves weight. c) Less thermo-mechanical differential stresses.	a) Power supply can NOT function in Corona region. b) Electric field still high at surface of coating. c) Sensitive to contamination. d) Long outgassing time due to large surface area.	HAPI LAPI by Doong. ISTP Modulator supply by Ruitberg.
Bare:	a) Fast circuit response. b) Saves weight c) NO thermo-mechanical stresses and delaminations.	Same as a), c) and d) immediately above. e) Bare high voltage metal is exposed. Therefore, needs long outgassing and high vacuum.	CHEM by U. of Maryland; -30 kV, on AMPTE.

I. Potting/Encapsulation

A. Material Properties and Selection

There are a bewildering variety of resins to choose from, and a Table: "Material Properties—Electrical, Mechanical" in W. Dunbar's 1979 report [1], also 1988 report [14], lists an apparently enormous variety. There are certain quantifiable target properties for high voltage (HV) potting materials shown here in Table 3.2. This helps to narrow down the choices, especially the "outgassing" criteria to prevent contamination of spacecraft optics. Reference documents for "outgassing" are NASA TN D-7362 and NASA Ref. Publ. 1124. Additional polymer characteristics that need to be considered are viscosity during the pouring of the resin, pot life, ease of handling, *need for primers,* adhesion to parts, exotherm (heat generation), tear strength, crack propagation, etc. Table 3.3 from Dunbar's 1984 [10] report gives these considerations.

Table 3.2. Target properties for high voltage potting materials.

Electrical properties:	
Dielectric constant	< 6
Dielectric strength	> 350 V/mil
Surface resistivity	$> 10^{12}\ \Omega$
Volume resistivity	$> 10^{12}\ \Omega$ cm
Other Physical Properties	
Shrinkage	$< 3\%$
Age shrinkage	$< 0.5\%$
Service temperature	$-55°$ to $+105°$C
Coefficient of Thermal Expansion	$< 1.5 \times 10^{-4}$/°F
Outgasing: Total weight loss Condensibles	$< 1\%$ $< 0.1\%$
Maximum cure temperature	$< 100°$C
Pot life	> 30 min

Table 3.3. Properties of interest for insulating materials, from W.G. Dunbar, Ref. [10].

PROPERTIES OF INTEREST FOR INSULATING MATERIALS				
Mechanical Properties	Electrical Properties	Thermal Properties	Chemical Properties	Miscellaneous Properties
Tensile, comprehensive, shearing, and bending strengths	Electric strength	Outgasing	Resistance to reagents	Specific gravity
Elastic moduli	Surface breakdown strength	Thermal conductivity	Effect upon adjacent materials	Refractive index
Hardness	Liability to track	Thermal expansion	Electrochemical stability	Transparency
Impact and tearing strengths	Volume and surface resistivities	Primary creep	Stability against aging and oxidation	Color
Viscosity	Permittivity	Plastic flow	Solubility	Porosity
Extensibility	Loss tangent	Thermal decompostion, Spark, arc, and flame resistances	Solvent crazing	Permeability to gases and vapors
Flexibility	Insulation resistance	Temperature coeffiecients of other properties		Moisture absorption
Machinability	Frequency coefficients of other properties	Melting point		Surface absorption of water
Fatigue		Pour point		Resistance to fungus
Resistance to abrasion		Vapor pressure		Resistance to aging by light
Stress crazing		Glass transition		Flammability
Crack propogation				

Table 3.4. Physical properties of some commonly used encapsulants, Ref. [12].

Material	Manu-facturer	Coefficient of Thermal Exp. $\frac{cm \times 10^{-4}}{cm\ ^{\circ}C}$	Thermal Conductivity $\frac{cal \times 10^{-4}}{cm\text{-}sec\ ^{\circ}C}$	Chemical Composition	Specific Gravity	Water Absorption Wgt %	Shore Hardness Number	Trans-parency and Color	Service Temperature Range (˚C)		Shelf Life Months
									from	to	
XR-5192	3M			Two part filled epoxy	1.53	0.36 (240 hours at 96% R.H.)	D72	Gray		+130	12
Scotchcast 235	3M	1.6	4.0	Unfilled epoxy	1.10	1.3 (1000 hour immersion)	D55	Brown		+130	12
Scotchcast 281	3M	1.5	12.0	Two part filled epoxy	1.43	0.4 (1000 hour immersion)	D665	Brown		+155	12
Scotchcast 3	3M	2.0	4.0	Unfilled epoxy	1.10	0.8 (1000 hour immersion)	D80	Clear		+130	12
RTV-11	GE	2.5	7.0	Silicone	1.18		A45	White	-59	+204	6
RTV-60	GE	2.1	7.4	Silicone	1.47		A60	Red	-59	+204	6
RTV-602	GE	2.9	4.1	Silicone	0.99		A15	Clear	-59	+204	6
RTV-615	GE	2.8	4.5	Silicone	1.02		A35	Clear	-59	+204	6
RTV-616	GE	2.7	6.6	Silicone	1.22		A45	Black	-59	+204	6
1090-SI	E&C *	0.54	4.1	Epoxy resin syntactic foam	0.78	0.4 (24 hour immersion)	D78		-73	+107	6
3050	E&C	0.40	9.5	Epoxy resin	1.55	0.2 (24 hour immersion)	D88			+125	
EP-3	E&C			Two part epoxy resin			D80	Clear	-55	+120	6
IC-2	E&C			Two component urethane			A80	Clear	-55	+120	6
93-500	DOW	3.0	3.5	Silicone	1.08	<0.10 (7 day immersion)	A46	Clear	-65	+200	12
XR-63-489	DOW	3.0	3.5	Two part silicone	1.05	<1.5 (7 day immersion)	A35	Clear	-55	+150	12
Sylgard-182	DOW	3.0	3.5	Two part silicone	1.05	0.1 (7 day immersion)	A40	Clear	-65	+200	12
Sylgard-184	DOW	3.0	3.5	Two part silicone	1.05	0.1 (7 day immersion)	A35	Clear	-65	+200	6
Sylgard-186	DOW			Two part silicone	1.12	0.1 (7 day immersion)	A32	Trans-lucent	-65	+250	6
RTV-3140	DOW		2.9	One part silicone	1.06	0.4 (7 day immersion)	A21	Clear	-65	+250	6
RTV-3145	DOW		4.0	One part silicone	1.12	0.4 (7 day immersion)	A33	Gray	-65	+250	6
K230	CONAP		5.0	Two part epoxy	~1.4	0.37 (24 hour immersion)	D65+70	Clear			12
CE-1155	CONAP			Two part solvent based polyurethane			Sward 70	Clear	-130		12
Epon 828 - Versamid 140 50% - 50%	Shell General Mills			Two part epoxy			Rockwell M80				
Solithane 113	Thiokol			Urethane prepolymer	1.07	~0.2 (24 hour immersion)	A-35 to D-60	Clear		+121	
Humiseal 1B12	CTC			One part, 20% solid acrylic	1.05	0.18 (24 hour immersion)			-59	+138	12
2# Custom Foam 6-1104	Rogers Foam		.083	Polyester-Polyurethane				Black			
Uralane 8267	Furane			One component urethane				Clear			6
B-6-640-1	Westing-house							Red			<12

* E&C = Emerson & Cuming

Table 3.5. Electrical properties of some commonly used encapsulants, Ref. [12].

Material	Dielectric Constant	Dissipation Factor	Test Frequency	Dielectric Strength, Volts/mil	Arc Resistance Seconds	Surface Resistivity ohm	Volume Resistivity ohm-cm
XR-5192	4.62	3.1	100 Hz	276	168		$1.5x10^{13}$
Scotchcast 235	5.2	0.05	100 Hz	325			$1x10^{15}$
Scotchcast 281	4.9	0.05	100 Hz	375			$>1x10^{14}$
Scotchcast 3	3.3	0.005	100 Hz	300			$>1x10^{15}$
RTV-11	3.6	0.019	60 Hz	500	≥100	$\sim10^{15}$	$6.0x10^{14}$
RTV-60	3.7	0.020	60 Hz	500	≥100	$\sim10^{15}$	$1.3x10^{14}$
RTV-602	3.0	0.001	60 Hz	500	≥100	$\sim10^{15}$	$1.0x10^{14}$
RTV-615	3.0	0.001	60 Hz	500	≥100	$\sim10^{15}$	$1.0x10^{15}$
RTV-616	3.0	0.001	60 Hz	500	≥100	$\sim10^{15}$	$1.0x10^{15}$
1090-SI	3.7 3.1 2.9	0.02 0.01 0.01	60 Hz 1 kHz 1 MHz	375			$1x10^{13}$
3050	4.4 4.2 3.9	0.01 0.02 0.04	60 Hz 1 kHz 1 MHz	400			$1x10^{14}$
EP-3	4.4	0.006	1 kHz	400			10^{13} /square
IC-2	5.0 5.0	0.04 0.04	60 Hz 100 MHz	>400			$>1x10^{12}$
93-500	2.75 2.73	0.0011 0.0013	100 Hz 100 kHz	570			$6.9x10^{13}$
XR-63-489	2.88 2.88	0.002 0.002	100 Hz 10 kHz	500	115	$3.6x10^{14}$	$1x10^{14}$
Sylgard-182	2.70 2.70	0.001 0.001	100 Hz 1 MHz	550	115		$2.0x10^{14}$
Sylgard-184	2.75 2.75	0.001 0.001	100 Hz 1 MHz	550	115		$1.0x10^{14}$
Sylgard-186	3.01 3.00	0.0009 0.001	100 Hz 100 kHz **	575		$>7x10^{16}$	$2x10^{15}$
RTV-3140	2.64 2.63	0.0016 0.0006	100 Hz 1 MHz	500	50		$5x10^{14}$
RTV-3145	2.81 2.78	0.0015 0.0028	100 Hz 1 MHz	600	50		$5.0x10^{14}$
K230	3.35	0.03	1 MHz	2000 (5 mil film)		$1.25x10^{14}$	$1x10^{14}$
CE-1155	3.50 3.43	0.0142 0.0138	100 Hz 1 kHz	3000 (2 mil film) 1045 (22 mil film)		$5.66x10^{14}$	$1.18x10^{16}$
Epon 828 - Versamid 140 50% - 50%	3.23 3.19 2.99	0.0036 0.0070 0.019	60 Hz 1 kHz 1 MHz			$5.5x10^{15}$	$1.22x10^{16}$
Solithane 113	2.8-5.0 4.5-5.1	0.014-0.162 0.006-0.079	1 kHz @ 80ºF 1 kHz @ 185ºF	340-512		$1.5x10^{15}$	$7x10^{12}$ to $3.6x10^{14}$
Humiseal 1B12 2# Custom Foam	2.8 97% voids inter-connecting calls	0.01	1 MHz	6000V (MIL-I-46058B)			$2.5x10^{14}$
Uralane 8267	4.4 3.6	0.049 0.053	1 kHz 1 MHz	2500 (3 mil film)	149		$3.0x10^{12}$
B-6-640-1	+			1200 (5 mil film)	126	$2x10^{13}$	

Table 3.6. Mechanical properties of some commonly used encapsulants, Ref. [12].

Material	Tensil Strength (kpsi)	Tensil Elongation %	Pot Life, hours	Viscosity, Poises	Principal Characteristics
XR-5192	0.995	75			High arc and track resistance
Scotchcast 235	1.3	75	0.25	15	Low viscosity, permanent flexibility
Scotchcast 281	2.1	45	0.3	480	Permanent flexibility, high temp. stability
Scotchcast 3	4.4	1.8	0.3	16	Lowest viscosity, excellent electrical properties
RTV-11	0.35	180	1-6	120	Flexible
RTV-60	0.80	130	1-5	500	Flexible, high temperature
RTV-602	0.10	200	0.5-8	12	Transparent
RTV-615	0.925	150	~4	40	Transparent, high temperature
RTV-616	0.925	125	~4	90	High temperature
1090-SI				18	Low density
3050				5	Low viscosity
EP-3			6	2.4	Surface coating, good mechanical and water resistance
IC-2		400		4.0	Surface coating, good mechanical and water resistance, high temperature
93-500	0.790	110	1	80	Low weight loss in hard vacuum
XR-63-489	0.90	100	8	50	Transparent, flexible, for laminating glass
Sylgard-182	0.90	100	8	30	Low viscosity, low cure shrinkage, wide temperature range
Sylgard-184	0.90	100	2	30	Low viscosity, low cure shrinkage, wide temperature range
Sylgard-186	0.70	420	2	450	High strength, wide temperatue range
RTV-3140	0.30	350		350	Clear conformal coating, no acetic acid evolved during cure
RTV-3145	0.70	675			Clear, high strength, non-corrosive, wide temperature range
K230	2.0		1-1.5		Clear epoxy, kit form
CE-1155			6	.72	Coating with good moisture and abrasion resistance
Epon 828 - Versamid 140 50% - 50%	8.3	8.3		~160	
Solithane 113	0.16-3.2	60-120	0.3-8	200	Versatile, soft to extremely rigid depending on catalyst used
Humiseal 1B12 2# Custom Foam 6-1104			1.05	0.3 strokes	Low viscosity coating Excellent vibration and shock protection
Uralane 8267				1.5-3.0	Repairable, solder-through, transparent coating
B-6-640-1			12	<12	Tough, resilent nontracking surface coating

Table 3.7. Potting and coating compounds used most often at GSFC.

Potting Resin:	Primer:	Volume Resistivity in Ω cm: 25°C	Dielectric Constant: 25°C	Coeff. of Thermal Expansion per °C	Glass Trans. Temp. Tg	Dielectric Strength V/mil
DC 93-500	DC 36060	6.9×10^{13} (6.2×10^{14})	2.7 at 0.1 MHz	300×10^{-6}	-115°C	550
Uralane 5753 LV	PR-1	1.2×10^{16} (2.3×10^{16})	2.9 at 1 MHz	200×10^{-6}	-60°C	450–500
Conathane EN-11*	PR4-20 or Epon828/ Versamid 140,50%-50%	4.3×10^{15} at 25°C; but 4.8×10^{11} at 130°C	2.9 at 1 MHz	140×10^{-6}	-70°C	450–500
Devolatil-ized RTV 615	SS 4155	4.5×10^{13} (1×10^{15})	3.0 at 1 KHz & 100 Hz	270×10^{-6}	-120°C	550
2B74 Polyure-thane		1×10^{15}	2.9 at 1 MHz, 4.2 at 100 Hz	100×10^{-6}		450
Hysol PR 18M		2×10^{13}	3, at 1000 MHz			
Parylene C		7×10^{16}	3, at 1 MHz	30×10^{-6}		~5000 V/mil:1mil; ~550 V/mil at 1/8 inch.

* EN-11A resin has been discontinued; instead, use EN-4A resin with EN-11B catalyst.

Table 3.8. Some glass transition temperature (T_g) measurements; excerpted from S.Y. Lee, Ref. [7].

MATERIAL	Tg, °C, by TMA	Tg, °C, by DMA
Lexan	146, 148	155
Plexiglass (regular)	110, 111	119
ULTEM 1000	215	
Epon 828/Versamid 140 51%, 49%	42, 43	71
Conap EN-11	-70, -68	-39
Uralane 5753LV	-59, -62	
Solithane 113/113-300 Compound #1	-7, -7	25
Humiseal-2B74 100/85	5, 5	37

Note: The first three materials are thermoplastics. The others are thermosetting materials cured at room temperature for 7 days, except for Epon 828/V140, which was cured at 70°C for 3 h and then at 80°C for 1 h.

Unfortunately, there is *no single, ideal* potting material that has all the desirable properties. Choice of the potting material is usually made from among (1) silicone rubbers or RTVs, and (2) polyurethanes. The encapsulant properties from the earlier GSFC document by Sutton and Stern [12] are repeated here for convenience as Tables 3.4, 3.5, and 3.6, with the addition of the most recently used potting materials at GSFC, namely Uralane 5753 LV and Conathane EN-11 as in Table 3.7. Epoxies, type (3), used for small jobs such as parts encapsulation, often are Epon 828/Versamid 140 or Stycast 3050.

A few words need to be said about the Glass Transition Temperature, T_g in the last column of Table 3.7. T_g is a polymer material's transition temperature below which the "plastic" chemical is hard and brittle and above which it is rubbery and softer. Actually the transition occurs over a small range of temperature of about 20°C. Also, in the literature, from different investigators, the T_g can be different by 20–30°, depending on the method of measurement, whether it is by Thermomechanical Analysis (TMA) or Dynamic Mechanical Analysis (DMA). The single temperature given in Table 3.7 is a rounded average from various sources. It is important that the lowest expected temperature during the flight and the lowest test temperature during the thermal vacuum testing is well *above* the T_g of the chosen potting or coating material. Table 3.8 gives some of the data from the research and article by Shen Yen Lee, Ref. [7].

Mention must also be made of plastic materials that are used *below* their glass transition temperatures. Two good examples of these are the older VESPEL, a polyimide, and the newer Ultem 1000, a polyetherimide by General Electric Plastics. These latter materials have excellent machinability and are used as housings for transformer molds, diode housings, etc. This is seen in Chapter 7 in the Cassini/CAPS high voltage power supply. There, the Ultem 1000 was chosen to house the parts in the high voltage multiplier stack and also for the transformer molds. Compared to other machinable thermoplastics, such as polycarbonate, the Ultem 1000 is better in that it does not craze upon machining, and there is a definite procedure for annealing afterwards to alleviate stresses. Ultem 1000 also has good adhesive

properties to the materials that might be used for potting or coating after the insertion of the electronic parts, such as to EN-11 or to Parylene. Furthermore, the Ultem fulfills the low outgassing requirements. Its glass transition temperature is 215°C.

B. Potting Process

The manufacturer's recommendations for the processing of the selected potting material should be carefully followed. In addition, very important steps to ensure successful potting for HV use in space must be taken. The Materials Processing Document, "Encapsulation of HV Power Supplies using Urethane Resin," No. S-313-029, Feb. 1993 is reprinted in this report as Appendix I in this chapter (Chapter 3).

1) *To ensure good adhesion* of the encapsulant to all the parts and cables of the HV assembly, this assembly must be scrupulously cleaned. Ultrasonic cleaning can be done with Freon TMS or vapor degreasing with Freon or Trichloroethylene; or a 50:50 mix of Freon and 200 proof ethyl alcohol can be used. Materials experts should be consulted.

   Certain outer surfaces must be pre-etched just before potting. Examples are Teflon, Delrin, and Diallyl Phthalate. Again, a materials expert should recommend the particular etchant solution.

   Priming should then be done on the parts, the board, and the bus wires. Priming is sometimes done selectively, such as omitting primer on the interior of the box walls except where the HV cable penetrates, or omitting it on coated capacitors. Each primer selected for a later encapsulant must, of course, have a very high resistivity and must be applied very, very thin.
2) *To avoid gas entrapment or bubbles.* After the resin, hardener and catalyst of the potting compound have been mixed, the mixture must be pre-degassed in a very large cup under a crude vacuum of about 1–5 torr. This "poor" vacuum is desirable because it will release the stirred-in air bubbles, but will not boil off the hardener. When frothing ceases, the vacuum is released, and the mixture transferred to a smaller glass beaker, and it and the assembly to be potted placed in a "vacuum-pouring" system. This is pumped down to about 1 torr and pumped for about 20 min. Then, without opening it to the atmosphere, the glass beaker is tipped by manipulation from outside the vacuum system, and the resin is poured into the electronic assembly. There should be very little or no air bubbling out from under the resin now. If the vacuum is too "good," there might be bubbling or bumping due to boiling of the hardener. Finally, the pump is turned off and the system brought up to atmospheric pressure by admitting air or dry nitrogen. This forces the resin into small spaces in the electronics providing the bottom of the box containing the electronics is leak-tight.

   The curing is now carried out at the proper temperature and atmospheric pressure (*never* partial pressure). Overpressure of several atmospheres has been used on transformers, but care must be taken that this does not prevent bubbles from breaking through the surface of the resin.
3) *To prevent tearing loose or cracking of the encapsulant.* Cure shrinkage and much larger coefficients of thermal expansion of potting resins than the inorganic embedded parts, require design and processing attention. Even though the potting polymers are plastics, nevertheless they demand to be given a definite volume at a given temperature. If an attempt is made to constrain the potted volume with the rigid metal walls of a shielding box on all sides and force adhesion on all sides, then during temperature changes, the stresses in the constrained potting material will cause cracking in the potting material or tearing loose from components and parts. These cracks or thin gaps of poor adhesion quickly fill with vapor, and will have partial discharges in them if they are in a high electric field region (E) leading to noise, degradation, and finally total breakdown after time.

   For the above reasons, the box walls, where the E is low, should not be primed, except at cable penetrations, permitting tearing loose of the potting as a thermomechanical stress relief. Also, one of the six surfaces of a rectangular block potting job should be left free. The free surface, usually the top of the potting, can be painted with a mix of the same resin loaded with carbon-black to make it sufficiently conductive to bleed off charges to the grounded box wall. Alternatively, if necessary, the potting can be done into a totally removable Teflon mold, all the free surfaces

later to be painted with a carbon containing resin for bleed-off of electrostatic charge. The free potted HV circuit block can then be mounted into a fairly snug-fitting (but not too tight) shielding box and the coating connected to the wall to bleed off electrostatic charge. Obviously, this mechanical mounting design needs to be planned well ahead.

II. Conformal Coating

As stated earlier, conformal coating and staking rather than solid potting may be preferred up to about 3000 V. A materials expert should be consulted as to the best processing for a given choice of coating resin. For instance, if EN-11 is used for coating, it is brushed on without dilution (being sure the brush loses no hairs) after initial degassing of the resin in vacuum. The coated board is then immediately degassed again in vacuum, and then, at atmospheric pressure, left to cure at 50°C for 24 h in a horizontal position.

Alternatively, the literature recommends thinning out of the coating resin with volatile thinner and applying three successive coatings, by spraying at right angles to each other. It is obvious that the circuit boards, just as for potting, have to be cleaned and perhaps even primed initially, as per Ref. [15].

The high voltage transformer with its hundreds of turns of very thin (AWG 32 and up) magnet wire presents special problems. It must be wound relatively loose, in a basket weave, and be pre-impregnated with a low viscosity resin (epoxy), without trapped air in the wire windings. This is especially important if the HV circuit assembly is later only conformally coated. In that case, if there is trapped air in the transformer it will diffuse out through the thin coating in a few weeks or months into the vacuum of space, leaving the inner HV windings surrounded by air gaps at partial pressures. These will then have many partial discharges due to the alternating high voltages at high frequencies, leading to erosion and eventual catastrophic breakdown between turns.

More recently, successful conformal coatings have been applied with Parylene-C to high voltage circuit boards for photomultiplier power supplies, to 3 kV. Special board-mounting techniques of ceramic multilayer capacitors must be followed, and this involves leaving at least 0.005 in of spacing between the bodies of the ceramic capacitors and the top surface of the circuit board. The coating must be extremely thin, that is 0.001 in, so that the ceramic chip capacitors are not rigidly attached by their bodies to the board. This Parylene-C coating must be done with special techniques and special equipment for vapor deposition in vacuum. A Goddard Space Flight Center Process Specification for coating of Cassini/CAPS-PROC-313-1 is attached as Appendix II to this chapter. This is a much higher voltage supply of 16 kV and is of modular construction. That is, only *some* portions are Parylene coated.

III. Completely Bare High Voltage Power Supplies

This has been used successfully by the University of Maryland Space Physics Department, College Park, Maryland, for a power supply at –30 kV for the AMPTE project. Many special techniques in construction must be used for such an unprotected supply. A person to consult is Dr. G. Gloeckner, Head of the Space Physics Department there. Some of the most obvious techniques are:

- Sufficiently large volume allowed
- Corona rings or field “Smoothers”
- Especially designed HV feedthrough from shielding box
- Absolutely no plastic or polymer coatings on parts such as cables, capacitors, resistors, etc., so as to achieve low vapor pressure
- Large vent hole in shielding box; vent hole modified with metal screen
- All testing done in high vacuum

- Three weeks of outgassing allowed for HV supply, in shielding box, in high vacuum, before voltage turn-on; this is especially important in orbit
- One of the HV transformers finally had to be Parylene-coated, after all.

See Chapter 7 for more detail.

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APPENDICES to CHAPTER 3

Appendix I: Materials Proc. Document S-313-029

Encapsulation of High Voltage Power Supplies, using a Polyurethane Resin. February 1993. The great detail herein is thought to be of help to technicians, having to actually do the potting. There is also Proc. Doc. S-313-019 on Conformal Coating with Polyurethane.

Appendix II: Process Specification CAPS-PROC-313-1, Rev.

Parylene Conformal Coating of the Cassini/CAPS HV Power Supply. The *unusual* vapor deposition in vacuum for conformal coating is described in detail.

R.S. Bever, A.P. Ruitberg, C.W. Kellenbenz, and S.M. Irish

Appendix I to Chapter 3

MATERIALS PROCESSING DOCUMENT

S-313-029

Encapsulation of High Voltage
Power Supplies Using a Polyurethane Resin

February 1993

Materials Branch
Office of Flight Assurance
NASA/Goddard Space Flight Center, Greenbelt, MD 20771

Encapsulation of High Voltage
Power Supplies Using a Polyurethane Resin

LIST OF FIGURES

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1.0 OVERVIEW

An insulating, encapsulating, polyurethane resin is applied to the cavity area of a high voltage power supply for several reasons. First, the encapsulant material must electrically insulate electrical parts and critical surfaces. Second, it must provide maximum moisture protection and environmental isolation. Third, it must have ultimate adhesion to the electrical parts and surfaces for the duration of the space flight mission.

This document defines approved procedures for encapsulating high voltage power supplies used in space flight applications. It specifies, in detail, all essential equipment, necessary materials, cleaning, masking, priming, end item acceptance criteria and approval requirements.

Personnel involved with encapsulating high voltage power supplies according to the procedure in this document are required to be trained and qualified in all work aspects described by the document, including the precautions and controls associated with handling polymer materials.

2.0 PURPOSE

The procedures outlined in this document are intended to produce uniform, repeatable and consistent results and high quality space-flight approved, encapsulated high voltage power supplies.

In the high voltage encapsulating process, the encapsulating material is applied to the high voltage cavity area under vacuum to minimize entrapped air bubbles and moisture. The prime objective of the overall process is the production of a finished encapsulated high voltage power supply containing a polyurethane resin with no entrapped air bubbles, good adhesion and electrical isolation.

3.0 SCOPE

This document contains the Goddard Space Flight Center (GSFC) approved procedure for encapsulating high voltage power supplies used on space flight missions.

This document is available for general use by GSFC or other NASA projects or by contractors, subcontractors, universities or other individuals engaged in building space flight hardware, but its use is subject to the provisions in Section 4.0.

4.0 APPROVAL REQUIREMENTS

Prior approval by the GSFC Materials Assurance Office (GSFC Code 313.A) or the personnel listed on the document sign-off page and the project for which the work is performed, shall be required before use of this document is permitted.

Any polymer or other material substitutes (materials not specified herein including solvents, wipes, etc.) used to encapsulate high voltage power supplies shall require prior approval by GSFC Code 313.A before their use in a space flight application is allowed.

5.0 QUALITY ASSURANCE REQUIREMENTS

5.1 WORKMANSHIP REQUIREMENTS

Space flight quality, encapsulated, high voltage power supplies are the result of careful workmanship by qualified personnel performing the work. Personnel involved in the encapsulation of power supplies for space flight hardware according to the procedures in this document shall be trained and certified as qualified and competent in all work

aspects encompassed by the document. Certification and training of personnel performing the project work shall be considered the responsibility of the Quality Assurance section of the organization performing the work.

Upon request, GSFC Code 313.2 personnel may be available for assistance during the encapsulating process. It is strongly recommended that personnel attend the space flight approved polymer training course given at NASA Jet Propulsion Laboratory as part of the certification process.

5.2 POWER SUPPLY FINAL ACCEPTANCE CRITERIA

All visual inspections shall be performed with a lighted magnifier having lOX magnification.

Measured Shore A hardness values shall be recorded in the appropriate documentation associated with the flight hardware.

As a precaution to protect flight hardware from electrostatic discharge (ESD), the completed, encapsulated power supplies should be stored or moved in a clean ESD approved bag or other approved container.

The encapsulating resin and its hardness test sample shall meet the following requirements before the unit is acceptable for space flight use:

a. The encapsulating resin hardness test sample shall be in a fully cured state, tack free to the touch of a plastic probe and shall be tested for Shore hardness. After testing, the hardness test sample shall exhibit a Shore A hardness within ±5 units of the value measured at the time of material receipt.
b. The encapsulated assembly shall be in a fully cured state and tack free to the touch of a plastic probe.
c. There shall be no cracks, cavities, blisters, tears, bums or discoloration on or in the assembly encapsulant material except as allowed herein.
d. The encapsulated assembly shall have no separations or delaminations on the critical surfaces or electrical parts. Critical surfaces shall be those surfaces where electrical parts or cable wires are attached to the high voltage assembly, including the part's surface. Separation of the resin from the container side walls is acceptable.
e. There shall be no entrapped air bubbles of any size in any direction in the critical area of the encapsuled assembly. The critical area shall be defined as the entire volume of the encapsulated assembly except near penetration of the high voltage output cable.
f. There shall be no exposed electrical parts or wire insulation as a result of incomplete encapsulant material coverage.
g. The encapsulated assembly shall be free of any particulate contamination such as dirt, hair, dust, etc.
h. Critical surfaces and electrical parts shall be primed for maximum adhesive strength as described herein (see Section 10.0).
i. There shall be no encapsulant material or primer residue on any of the non-encapsulated surfaces after completion of the encapsulation work.
j. The encapsulant surface shall exhibit no cuts or scratches due to post encapsulation resin trimming.

6.0 SPACE FLIGHT MATERIALS CONTROL AND USE REQUIREMENTS

There are specific control requirements for space flight approved polymer materials and their use in space flight applications. The requirements shall be follows:

a. Upon receipt, the polymer materials shall be verified against the appropriate documentation to ensure that the correct materials were delivered. A Standard Materials Certification (SMC) or Certificate of Compliance

(CofC) form from the manufacturer shall accompany the materials and shall include lot number, cured and uncured properties, date shipped, date manufactured and the manufacturer's expiration date. See Attachment I.

b. The SMC or CofC and the purchase order shall be filed for record keeping, material property test verification, and traceability of the material.

c. An inspection label shall be attached to each material container providing information on the material type, date of receipt, date of manufacture, manufacturer's expiration date, lot number, storage requirements, and Shore hardness of the cured resin. A Shore hardness test shall be performed by the receiving laboratory upon receipt of the materials and shall be completed before any high voltage encapsulating work of flight hardware begins. The Shore hardness measured upon receipt of the materials shall be verified against the SMC or CofC test values and recorded on the materials inspection label along with the test date. The material shall not be used if it does not exhibit proper cure and Shore hardness of ±5 units of the manufacturer's specified value.

d. All space flight materials shall be properly stored in a separate cabinet, refrigerator or freezer as required by the temperature specifications in the SMC or CofC. This storage cabinet shall be reserved only for space flight materials, and shall be labeled "FOR SPACE FLIGHT USE ONLY," which have not exceeded their expiration date. Material expiration dates shall be inspected weekly. Expired materials shall be removed from the space flight material storage cabinet and stored in a separate cabinet. Expired materials shall be labeled "NOT FOR SPACE FLIGHT USE" and disposed of properly.

e. Materials shall not be used for space flight applications after they have exceeded their manufacturer's expiration date unless an approval for an expiration date extension has been granted. An extension of the materials expiration date shall require the approval of GSFC Code 313.A personnel. An extension is generally granted for 30 days. The request for extension shall be submitted in writing 3 weeks prior to the materials expiration date. Approval shall be granted only after the soon-to-expire material has been tested at GSFC and has demonstrated proper uncured (visual inspection—color, lack of crystallization, etc.) and cured properties. Any material exceeding the manufacturer's expiration date by more than 90 days shall not be used.

f. Shelf life may be extended by the contractor, providing that the contractor submits a procedure for shelf life extension approval. This procedure must be submitted prior to the material's use and approved by the Materials Assurance Office, Code 313.A.

g. The preparation and application of polymers for space flight use shall be documented and controlled using a work request and mixing record form. The work request and mixing record shall be fully completed and filed for record keeping. An acceptable example of a work request and mixing record form can be found in Attachments II and III, respectively, of this document.

h. As required by law, all materials used in this document should have the appropriate Material Safety Data Sheet (MSDS) on file and readily available as needed.

7.0 MATERIAL SUPPLY AND SOURCE LIST

The following is a list of materials used in this procedure or manufacturers of these items.

Materials	Source
Acetone, A-18	Fisher Scientific Co. Pittsburg, PA
Aluminum Sheet 2.5 x 2.5 x 0.015 inches thick (63.5 x 63.5 x 0.38 mm)	Local Source
Bag, Plastic Aclar LB-522 (22C)	Clean Room Products, Inc. Ronkonkoma, NY
Bag (Plastic), ESD 3M 2100 Series	3M Austin Center Austin, TX
Beaker, Glass 100cc	Fisher Scientific Co. Pittsburgh, PA
Beaker (Plastic), Polyethylene 16 oz (454 g)	Airlite Products Omaha, NE
Brush, Gordon AL 25IN	Gordon Brush Manufacturing Co. Los Angeles, CA
Brush, Sable, 1/6, 1/8 and 3/8 inch diameter (1.6, 3.1 and 9.5 mm)	Local Source
Conathane EN-11-A*	Conap, Inc. Olean, NY
Conathane EN-11-B	Conap, Inc. Olean, NY
Dryer, Forced Air 09-201-5	Fisher Scientific Co. Pittsburg, PA
Epon 815 Epoxy	E.V. Roberts Culver City, CA
Ethyl Alcohol, 200 Proof	Midway Grain Products Perkin, IL

*EN-11A is no longer available; use EN-4A with EN-11B.

7.0 MATERIAL SUPPLY AND SOURCE LIST The following is a list of materials used in this procedure or manufacturers of these items.	
Materials	Source
Face Mask with Organic Filter 17-674	Fisher Scientific Co. Pittsburgh, PA
Gauge, Thickness, Wet Film Model 115, GR660	Pacific Scientific Silver Spring, MD
Gloves, Polyethylene, 11-394	Fisher Scientific Co. Pittsburgh, PA
Glass Beads, 11-311C	Fisher Scientific Co. Pittsburgh, PA
Heptane 03008	Fisher Scientific Co. Pittsburgh, PA
Isopropyl Alcohol A-417	Fisher Scientific Co. Pittsburgh, PA
Primer PR-420--A	Products Research & Chemical Corp. Gloucester City, NJ
Primer PR-420--B	Products Research & Chemical Corp. Gloucester City, NJ
Spatula, Plastic Part No. 6169-0010	Nalge Co. Rochester, NY
Spatula, Stainless Steel 14-375-10	Fisher Scientific Co. Pittsburgh, PA
Swabs, Cotton	Local Source
Swabs, Foam TX-700B	Texwipe Co. Hillsdale, NJ
Tape, Kapton* K-102	Connecticut Hard Rubber Co. New Haven, CT
Tape, Teflon* HM 430	Connecticut Hard Rubber Co. New Haven, CT

7.0 MATERIAL SUPPLY AND SOURCE LIST The following is a list of materials used in this procedure or manufacturers of these items.	
Materials	Source
Versamid 140	E.V. Roberts Culver City, CA
Wipes, Cotton TX 304	Texwipe Co. Hillsdale, NJ

*Registered Trademark of E.I. DuPont

8.0 PROCESSING FACILITY AND ESSENTIAL EQUIPMENT REQUIREMENTS

Encapsulation of high voltage power supplies shall require the use of a clean facility to control contamination (especially silicones, hydrocarbons, vinyl plasticizers and particulate contamination). The clean facility shall have a GSFC project approved cleanliness level and good ventilation, good lighting temperature control between 20° and 25°C, and relative humidity ranging from 30% to 60%.

Work space areas must be sufficiently large to contain the actual encapsulating work, essential equipment, instruments, and all other required hardware. These items shall be inside the clean facility to minimize contamination during the transfer of flight hardware from one work area to another.

Essential equipment shall include:

a. A calibrated, laboratory weighing balance, accurate to 0.01 gram, used to control material mixing proportions.
b. A vacuum chamber or bell jar capable of operating at a vacuum level 50 microns of mercury (Hg) or less when empty, used to ensure a bubble free end item.
c. A laminar flow bench clean work station providing a 100 cleanliness class level (per FED-STD-209B) used to prevent contamination. This work station includes a minimum lighting capability of 100 foot candles of illumination (1,076 lumens per square meter).
d. A health and safety approved exhaust fume hood for exhausting chemical fumes and vapors used to meet OSHA requirements. A minimum of 125 ft/min (38 m/min) air exhaust at the hood face is recommended.
e A clean, oil free, 0 to 100 psi (0 to 0.69 MPa), nitrogen gas supply system including hoses, valves, a regulator and nozzles used to spray clean and blow dry cleaned surfaces. No flexible polyvinyl chloride (PVC) hose such as Tygon shall be allowed. Clean nylon, Teflon, polyethylene and Viton hoses are recommended and acceptable.
f. A lighted magnifier with 10x magnification used for visual inspections.
g. Shore A and D hardness testers, used for verifying proper cured hardness of the encapsulating resin and epoxy coating.
h. A clean, forced-air convection oven, used in the final process to dry surfaces and other non-flight hardware.
i. A customized vacuum chamber capable of operating at 10^{-2} Torr or better, when empty. The vacuum chamber will be used for encapsulating the electronic assembly under vacuum.
j. A spray apparatus for cleaning surfaces and other hardware.
k. A micrometer for obtaining thickness measurements of the reference primer coating.
l. A wet film thickness gauge used to determine the primer application thickness.

The following list details the model or part number, size or capacity, and source addresses for the essential equipment: (This representative list is not meant to constitute an endorsement of these products, only that they were used in the development of this work for space flight hardware on GSFC programs.)

a-l Mettler Balance
PC4400
Mettler Instrument Corp.
Hightstown, NJ 08520

b-1 Hotpack Thermal Vacuum Chamber including an
18 CFM Mechanical Pump
Floor Model 273700-13
Hotpack Corp.
Philadelphia, PA 19154

c-1 Class 100 Laminar Flow Bench
Model 530-CS
Laminaire Corp.
Rahway, NJ 07065

d-1 Slimline External Air Induction Exhaust Fume Hood
Model ESS-O6
Duralab Equipment Co.
Brooklyn, NY 11236

e-l Nitrogen Gas (99.95% pure or boil off to meet this specification)
Pressure Range: 0 to 100 psi (0 to 0.69 MPa)
Local Sources

f-1 Luxo Illuminated Hand Magnifier, 10X
Catalog No. L-03882-40
Cole-Parmer Instrument Co.
Chicago, IL 60648

g-1 Hardness Testers, Shore A & D
Shore Instruments & Mfg. Co.
Freeport, NY 11520

h-1 Blue M Convection Oven
Model POM-588C-3X
Blue M Electric Co.
Blue Island, IL 60406

i-1 Key High Vacuum Products, Inc.
Customized Chamber
Nesconset, NY 11767

j-1 Binks Model 15 Spray Gun
Binks Mfg. Co.
Franklin Park, IL 60131

k-1 Micrometer, 1 inch (25.4 mm)
Catalog No. 12-126
Fisher Scientific Co.
Pittsburgh, PA 15219

l-l Wet Film Thickness Gauge
Model 115, Part No., GR 6601
Pacific Scientific Co.
Silver Spring, MD 20910

9.0 POWER SUPPLY CLEANING PROCESS REQUIREMENTS

Starting at this point in the procedure, all of the following processes shall be performed in a clean facility. Personnel shall wear clean facility approved clothing, clean facility approved gloves and follow strict clean facility approved procedures. Only clean facility approved materials and wiping accessories (see Section 13.0) shall be allowed in the clean facility.

Thorough cleaning of the high voltage power supply is required to ensure that there is maximum adhesion between the insulative material and its contact surfaces. In addition to cleaning the power supply, brushes, spatulas, beakers, cleaning spray apparatus, and drip containers are cleaned at this time to minimize any possible contamination from these non-flight items.

It is important that power supplies containing electrostatic sensitive parts are protected against ESD. Protection procedures must be followed during the complete process. All personnel and work stations shall be well-grounded to prevent any damage during the entire processing of electronics. Wrist straps connected to an approved ESD ground shall be used. The wrist straps must be worn with the metal contact against the wearer's skin. Wrist strap electrical continuity shall be verified daily prior to the encapsulation work. Wrist straps shall be approved by the project or the Quality Assurance section of the organization performing the work.

CAUTION

Office of Safety and Health Administration (OSHA) precautions and guidelines shall be followed when handling chemicals and/or organic materials.

Personnel may need to wear a face mask with an organic filter throughout the cleaning and encapsulation process for protection from solvent and organic resin vapors. Personnel must wear a face mask if required by their local health and safety standards. The cleaning shall take place under the exhaust fume hood.

Personnel performing the encapsulation work should verify the maximum operating voltage of the power supply and place that value on the certification log accompanying the power supply.

The substrate surface preparation shall be as follows:

a. Brush and spray clean the following items: primer witness sample substrate, spatulas, blades, containers, drip container, and any other non-flight items being used in the processing of flight hardware. Use a 1:1 volume mixture of alcohol/heptane and a precleaned sable brush. Brush clean each item for 2 to 3 minutes then spray clean each item for 1 to 2 minutes using a Binks Model 15 spray apparatus. Set the spray apparatus between

40 and 50 psi (0.27 and 0.34 MPa). This ensures that the flow of solvent forces loose any particles adhering to the items and flushes away contaminants. Use a drip container to catch excess solvent. Dry the items per steps e and g shown below. Store the cleaned items, unless immediately needed, in a clean bag or cabinet free of contaminants such as silicones, vinyls, hydrocarbons and particulates.

b. Clean the high voltage power supply. Begin by gently brushing all of the critical surfaces and electronic parts, including the interior and exterior surfaces of the power supply container. Use a soft sable brush 3/8 inch (9.5 mm) diameter trimmed to 1/4 inch (6.3 mm) in length. Brush the surfaces and parts using a 1:1 part by volume of alcohol/hexane unless directed otherwise. This will loosen any contamination from the surface and be flushed away when spray cleaned. Use a small soft conductive nylon Gordon brush when working with an ESD sensitive electronic assembly. The brush should be grounded when used to clean the assembly.
c. Spray clean the power supply with a Binks Model 15 spray apparatus to clean all surfaces. During the spray cleaning, hold or position the power supply so that the long length is horizontal and parallel to the cleaning table top with the open cavity facing the operator. Tilt the power supply 10° to 20° from the vertical so that the top side is closest to the operator. This will direct the solvent spray away from the operator and towards the drip container. Spray the power supply back and forth from top to bottom to allow any contamination to flow downward and off the assembly.
d. Rotate the assembly a full 360° in steps of 90°. On each 90° rotation, spray clean as in step c. Spray clean each direction for 2 to 3 minutes for small power supplies and 3 to 5 minutes for large power supplies, being sure to thoroughly spray clean all surfaces and components. Set the spray apparatus gas system pressure between 40 and 50 psi (0.27 to 0.34 MPa). This will ensure that all surfaces and parts have been thoroughly spray cleaned. The cleaning of the assembly shall also include exterior wall surfaces.
e. Remove excess solvent from the assembly surfaces by blow drying the cleaned surfaces with dry, clean nitrogen. Set the nitrogen gas pressure between 40 and 50 psi (0.27 to 0.34 MPa). Dry the power supply in each direction for 2 to 3 minutes (rotating as in step d), until all of the solvent evaporates.
f. Inspect the assembly surfaces and parts for cleanliness. Use a hand held l0X magnifier. If any stubborn contamination deposits are noted, they should be removed and the power supply recleaned as in steps b through e. Use precleaned urethane swabs lightly dampened with acetone to remove any stubborn contamination.
g. Dry the cleaned assembly. This final drying removes all cleaning solvent and moisture. Place the assembly in a clean convection oven at 65°C and dry for a minimum of 30 to 45 minutes.
h. Remove the assembly from the oven and allow it to cool to ambient temperature on the laminar flow bench. Store the assembly, unless immediately needed, in a clean plastic bag. Place the assembly in a static control bag if it is ESD sensitive.
i. The assembly should be redried if stored for longer than 18 hours. Repeat step g above prior to the encapsulant material application.
j. The assembly is now clean and ready for the next step. It is very important that all the surfaces in the power supply cavity that are to be encapsulated be extremely clean and dry.

10.0 PRIMING REQUIREMENTS

To enhance the adhesion of the encapsulating resin to surfaces and parts, it is critical that primer be applied.

A person who is familiar with the electrical design, the encapsulant resin, and primer should assist the power supply designer to specify surfaces and parts to be primed. No Shore hardness test sample is required of the primer material. A primer witness sample using an aluminum sheet, (specified in Section 7.0), should be used to verify proper cure and allow personnel to continue the encapsulating process with a high degree of confidence that the primer is cured. The processing shall not continue if the primer exhibits improper curing.

The primer application shall take place at the laminar flow bench or the air exhaust fume hood to control contamination. The primer shall be kept free of any contamination because contamination may reduce adhesion or dielectric insulation properties of the encapsulated end items.

Personnel may need to wear a face mask with an organic filter during the priming process at the laminar flow bench or fume hood because of the primer vapors.

The surfaces and parts, including the primer witness samples, should be coated using a clean, small sable brush.

The primer process shall be as follows:

a. Mask-off any holes on the outside of the power supply assembly container, through which the encapsulant resin may leak or flow. Use 1/2 or 1 inch (12.7 or 25.4 mm) wide Teflon tape. Criss-cross the tape to ensure that it will not separate or delaminate during the encapsulation process. Press down firmly on the tape to ensure good adhesion.

   NOTE: Each type of encapsulation resin and surface requires its own primer. For the polyurethane, Conap EN-11, PR 420 works best, except on glass coated surfaces.

   NOTE: High Voltage power supply parts with glass coated surfaces must be primed with an Epon/Versamid mixture at least 24 hours prior to the PR-420 primer coating. The epoxy primer application is being described after the PR -420 because ordinarily few or even no glass coated parts are used in high voltage power supplies.

b. The primer formulation, all materials ±0.05 grams, shall be as follows:

Material	**Function**	**PBW***
PR-420-A	Resin	3.0 g
PR-420-B	Curing Agent	21.9 g

   * Parts by Weight

   NOTE: Part B must be well stirred for 3–5 minutes prior to using.

   NOTE: Throughout the entire process, use only plastic spatulas for stirring in plastic beakers. A steel spatula may scrape plastic off the interior of the beaker and cause contamination. Plastic or stainless steel spatulas may be used for stirring in glass beakers.

c. Weigh out the PR-420-B under the air exhaust fume hood. Use a laboratory balance. Measure the amounts specified above. Place the material in a clean glass or plastic beaker.
d. Weigh out the PR-420-A under the air exhaust fume hood. Using the laboratory balance, measure the amount specified above. Add this to the PR-420-B already in the beaker. Stir well for 3 to 5 minutes.
e. Allow the mixed PR-420 to stand at ambient temperature for a minimum of 15 minutes before using. This allows entrapped air bubbles to escape. Place a tight lid or cover on the container to prevent evaporation.

   NOTE: Do not vacuum de aerate the above mixed PR-420 primer.

f. The following surfaces and parts of the power supply shall be primed as follows:
   - High voltage container cavity side walls and bottom—*Do not prime unless required.*
   - Caddock High Voltage Resistor—Prime the resistor body, including the electrical lead wires. NOTE: The Caddock resistor *shall not contain a silicone treated surface* when purchased.
   - Maida High Voltage Ceramic Capacitor—Prime only the electrical lead wires, including approximately 1/8 inch (0.63 mm) of the capacitor legs. NOTE: Capacitor body *shall not contain a wax-treated surface* when purchased.
   - Bare electrical wires—Prime

- Carbon resistors—Prime
- Reynolds connector—Prime
- Electrical insulated lead wires—Prime
- Electrical feed-through terminals—Prime except for glass coated feed-through terminals. An epoxy coating is used for glass surface feed-through terminals—see step k below.
- High Voltage Cable—Prime if within high voltage area.
- Diodes—Prime except for glass body diodes. An epoxy coating is used for glass body diodes—see step k.
- Solder Ball joints—Prime
- Aluminum Witness Sample—coat for thickness and cure determination.
- Parts and surfaces requiring primer as specified by engineering drawing and not listed here, shall be primed.

NOTE: The above recommendations represent the majority of parts and surfaces found in power supplies. Power supplies vary in design; complexity and parts other than listed above may be found in power supplies. In most cases, these should be primed if they are within the high voltage power section.

g. Prime the power supply parts and surfaces using a 1/8 or 1/4 inch (3.1 or 6.3 mm) clean sable brush. Apply a *uniform thin coating* of the primer to the parts and surfaces, and to the aluminum witness sample. Leave a small part of one corner of the witness sample uncoated for aluminum thickness determination. Apply the primer to the parts, surfaces and witness sample to obtain a final dry thickness of 0.001 to 0.002 inches (0.025 to 0.050 mm). Use a wet thickness gauge to measure the thickness of the coating. Allow the power supply to stand at ambient temperature between 20° and 25° for 60 minutes before performing the primer acceptance criteria.
h. The primed assembly shall meet the following acceptance criteria when viewed with a lighted magnifier having l0X magnification, before the encapsulation process begins:
    1) There shall not be any entrapped air bubbles in the applied primer surface.
    2) There shall not be any unprimed spots on the assembly as required in step g and/or the engineering drawings.
    3) There shall not be any excess primer due to drops, spills or other mistakes on surfaces of the assembly which are not part of the primed area.
    4) There shall not be any primer bridging on any of the parts.
    5) The primer shall exhibit proper cure; this shall be verified using the primer witness sample.
    6) The primer shall exhibit proper thickness; this shall be verified using the primer witness sample.

Failure of any of the above six acceptance criteria shall be cause for rejection and removing the primer coat. The primer coat shall be removed and recoated per steps a to g. The primer witness test sample acceptance criteria for proper primer cure shall be as follows: after 60 minutes, the primer shall be dry and tack free to the touch of a plastic probe.

The primer witness test sample for proper thickness shall be measured as follows: after 60 minutes, the dry primer shall not exceed 0.002 inches (0.050 mm) as measured with a micrometer. The measured thickness shall be recorded in the appropriate documentation attached to the flight hardware.

i. The assembly is primed and ready for encapsulation. The encapsulation shall be performed any time after the 60 minute stand at ambient temperature between 20° and 25°C, but must be done within a 5 hour time frame from the time of primer application.
j. Label the primer witness test sample with the flight assembly serial number, date, primer material type and lot number to ensure material traceability. Store the witness sample at ambient temperature between 20° and 25°C in a clean bag. The primer witness sample should be labeled and retained for at least one year after the space flight launch.

NOTE: High voltage power supply parts with glass coated surfaces must be primed with an Epon/Versamid mixture at least 24 hours prior to the PR-420 primer coating. The epoxy primer application is being described after the PR-420 because ordinarily few or even no glass coated parts are used in high voltage power supplies.

k. Glass coated feed-through terminals and glass coated diodes shall be primed with a thin Epon/Versamid coating. Power supplies may or may not have these parts. *Any high voltage power supply parts which does not have glass coated surfaces shall proceed from here to Section 11.0.*

The epoxy coating formulation, all materials ± 0.05 grams, shall be as follows:

Material	**Function**	**PBW***
Epon 815	Resin	10.0 g
Versamid 140	Curing Agent	10.0 g

*Parts By Weight

l. Weigh out the Epon 815 under the air exhaust fume hood. Use the laboratory balance. Measure the amount specified above. Place the material in a clean beaker.

m. Weigh out the Versamid 140 under the exhaust fume hood. Use the laboratory balance. Measure the amount specified above. Add this to the Epon 815 already in the beaker. Stir well for 3 to 5 minutes.

n. Place the beaker containing the mixed epoxy in a vacuum chamber. Vacuum deaerate at an ambient temperature between 20° and 25°C at a pressure of 100 microns or less for 10 to 15 minutes or until all entrapped air bubbles are removed.

o. Remove the beaker and its contents from the vacuum chamber after clean air or nitrogen back fill. Coat the electrical glass feed-through terminals, glass diodes and the aluminum witness sample using a 1/8 inch (3.1 mm), clean sable brush. Brush the surfaces gently until a very thin epoxy coating has been obtained. The final smooth and uniform wet coating thickness shall be controlled between 0.0005 to 0.00 1 inches (0.012 to 0.025 mm) thick. Leave a small portion of one corner of the aluminum substrate for thickness measurement verification. The operator should practice resin thickness control prior to the actual resin application to obtain the specified thickness. Use a thickness gauge to measure the wet thickness of the epoxy coating. Measure the thickness of the resin on the witness sample.

p. Place the power supply, the hardness test sample, and The witness sample in the vacuum chamber and vacuum deaerate at an ambient temperature between 20° and 25°C at a pressure of 100 microns of Hg or less for 10 minutes to remove entrapped air bubbles.

q. Excess resin from each mixed batch shall be retained as a hardness test sample; the test sample shall be processed with the power supply and then used to verify the Shore D hardness. The hardness test sample shall be 0.250 inch (6.3 mm) thick and approximately 1.5 inches (38 mm) in diameter. The Epon/Versamid mixture has a pot life of 60 minutes. A fresh mixture should be prepared after this time.

r. Remove the power supply, the witness sample, and the hardness test sample from the vacuum system after proper clean air or nitrogen gas chamber back-fill. Place the items on the laminar flow bench top surface and allow to stand at ambient temperature between 20° and 25°C for 18 hours.

s. Place all the items mentioned in step r in a convection oven. Bake at 65°C for 6 hours.

t. Remove the items from the convection oven and place them on the laminar flow bench top. Allow them to cool to ambient temperature between 20° and 25°C for 60 minutes.

u. Measure the hardness test sample with the Shore Durometer. The hardness shall be a minimum of D-50. Proceed with the assembly encapsulation if the Shore hardness value is met. The encapsulation shall not be done if the Shore hardness value is not met.

NOTE: The hardness test value of the epoxy primer must be determined prior to the final cure on the flight hardware. After the final cure, as described in step s, it would be difficult to remove without damage to the hardware.

11.0 ENCAPSULATING RESIN APPLICATION REQUIREMENTS

In the encapsulation process, the primed assembly electronics are encapsulated in a vacuum chamber.

The container for the electronic assembly encapsulation is usually no more than 2 to 3 inches (50 to 75 mm) deep. The container should not present sharp comers or complex surfaces to the encapsulant. In no way should there be any attempt to restrict the encapsulating material on all sides as it will not yield during thermal excursions, if no room for expansion has been allowed. See Figure 1 [3.A.I.1] for an illustration of a typical high voltage power supply without the encapsulating resin.

The chamber used to introduce the polyurethane resin under vacuum should have the following features: A mechanical pump with a zeolite trap between the mechanical pump and the vacuum chamber to prevent hydrocarbon vapor from back streaming into the chamber. The chamber should be capable of obtaining a pressure of 10^{-3} Torr, and equipped with a vacuum gauge capable of reading the vacuum pressure, a variable back fill gas leak valve, a rotating table in the interior and workable from the exterior, a vertical stand with a ring holder for the resin cup in the interior and workable from an exterior control to tip the cup. See Figure 2 [3.A.I.2] for an illustration of the customized vacuum chamber for encapsulating power supplies.

Excess resin material from each mixed batch shall be retained as a hardness test sample; the test sample shall be used to verify proper material cure and Shore hardness. The hardness test sample shall be a minimum of 0.250 inch (6.4 mm) thick and approximately 1.5 inches (38.1 mm) in diameter.

It is important that the mixing of the resin formulation and process be performed *expeditiously* to prevent a significant increase in viscosity which in turn makes the encapsulating resin more difficult to pour.

The resin shall be prepared in the fume hood and kept free of any contamination because contamination may reduce adhesion or dielectric insulation properties of the encapsulated end item.

Personnel may need to wear a face mask with an organic filter during the resin preparation at the exhaust fume hood because of the resin vapors. A face mask shall be worn if required by their local health and safety standards.

The encapsulating process shall be as follows:

a. To prevent resin from overflowing or splattering from the power supply during the process attach a 1 or 2 inch (25.4 or 50.8 mm) wide strip of Teflon tape around the top side of the power supply's open cavity. Overlap the tape approximately 0.250 inch (6.4 mm) on the container exterior wall surface. Press down firmly on the tape surface attached to the container to prevent lifting. Mask-off any other surfaces or holes to prevent resin contact during the process. Place the power supply on the flat rotating table in the vacuum chamber in a horizontal position. See Figure 3 [3.A.I.3] for the power supply mounted on the rotating table in the vacuum chamber.

b. The encapsulating resin formulation, all materials ± 0.05 gms, shall be as follows [EN-11-A is no longer available; use EN-4-A instead].

Material	Function	PBW*
Conathane EN-11-A	Resin	100.0 g
Conathane EN-11-B	Curing Agent	55.0 g

*Parts By Weight

NOTE: Part B curing agent must be well stirred for 3 to 5 minutes before using.

c. Weigh out the EN-11-A resin under the exhaust fume hood. Use a laboratory balance. Measure the amount specified above. Place the material in a clean beaker.

d. Weigh out the EN-ll-B curing agent under the exhaust fume hood. Use a laboratory balance. Measure the amount specified above. Add this material to the EN-11-A already in the beaker. Stir the material well with a spatula for 3 to 5 minutes.

NOTE: The amount of resin to prepare will depend on the size of the power supply. More than one mix may be needed to fill large power supply cavities.

e. Place the beaker and the resin mixture in a clean laboratory vacuum chamber. Vacuum deaerate at an ambient temperature between 20° and 25°C at a pressure of 100 microns of Hg or less for 4 to 6 minutes. This chamber removes the initial entrapped air bubbles from the resin. The resin should be bubble free at this time.

f. Remove the beaker and its contents from the vacuum chamber after proper clean air or nitrogen gas back-fill.

g. Mount the beaker and the mixed resin in the customized vacuum chamber's ring clamp on the rotating tippable stand. Secure well with Teflon tape. Wrap the tape several times around the beaker's mid- section, e.g., top to bottom, being sure to pass the tape across the ring clamp surface.

h. Position the power supply beneath the resin cup so that it will pour into the middle of the power supply's cavity. The power supply may need to be rotated ± 30 degrees during the resin pouring (depends on the size of the power supply) so that all of the resin is not poured in one place.

i. Place the vacuum chamber bell jar over the resin cup, the power supply, and on the vacuum base plate. Start the pump and begin the vacuum pump down. Allow the vacuum deaeration to continue for approximately 20 minutes, before pouring, to extract as much entrapped air and water vapor from the electronics as possible. It is desirable for the vacuum chamber pressure to reach 1 Torr or less in 5 to 10 minutes, depending on the size of the power supply and the bell jar size.

j. Pour the resin slowly into the power supply cavity by tipping the beaker with the external control knob. Allow the resin to slowly enter the power supply cavity until approximately half full. Rotate the power supply platform using the external rotating knob to spread the resin across the assembly electronics during the pouring. Stop pouring and allow the vacuum de aeration to continue for approximately 15 to 20 minutes. There will be much resin bubbling as entrapped air escapes from surfaces and parts. The bubbling becomes less active and slows with time, but may never completely quit. See Figure 4 [3.A.I.4] for illustration of resin being poured into the power supply cavity in the vacuum bell jar.

k. After the above 15 to 20 minutes, slowly pour the resin again by tipping the resin cup with the external rotating knob, until the power supply is almost full and the electronics are covered, or according to engineering drawing requirements. Continue to vacuum deaerate for another 15 to 20 minutes.

l. Stop the vacuum pumping by closing the mechanical pump foreline valve. Allow the power supply to stand at vacuum pressure for 5 to 10 minutes for any remaining air bubbles to escape. Use the variable gas valve to slowly back-fill the vacuum chamber with clean air or nitrogen gas.

m. Remove any accidental particle contaminant or trapped air bubbles in the resin at this time. This shall be performed within 75 minutes after the resin is mixed. Use a clean needle to pop any trapped air bubbles or to remove any particles of contamination. Use a lighted l0X magnifier to inspect and find the anomalies.

n. This completes the encapsulation of the power supply. Cure the resin at atmospheric pressure. See Section 12.0 for resin curing.

12.0 ENCAPSULATING RESIN CURING REQUIREMENTS

The resin should be considered in a partially cured state 48 hours after the encapsulation work has been completed when cured at an ambient temperature between 20°C and 25°C.

The resin should be considered in a fully cured state 10 days after the encapsulation work has been completed when cured at an ambient temperature between 20°C and 25°C, or 5 days when cured at a maximum of 40°C but only after the completed power supply has been allowed to stand for 48 hours at ambient temperature of between 20°C to 25°C.

13.0 ACCESSORIES CLEANING REQUIREMENTS

Cotton swabs, urethane foam swabs and cotton wipes are the wiping accessories used in the clean facility during the application process. Most of these items are used for cleaning, but all of these items are potential sources of clean facility contamination if they are not certified for clean facility use.

To be considered certified and suitable for clean facility use, the items listed above require cleaning by a Soxhlet extraction method for 48 to 72 hours. Cleaning the items is time consuming, however, it is essential that these strict cleanliness procedures be followed when working with space flight hardware.

Prior to cleaning any material which is to be used in a clean facility, a solvent filled Soxhlet extractor system shall undergo a thorough, internal, self-cleaning for about 18 hours of cycling. The used solvent shall be properly discarded upon completion of the internal cleaning, and the system shall be filled with fresh, clean solvent in preparation for the extraction of the materials which are to be used. Fresh, clean solvent shall be totally substituted for the used solvent aft every third 48 to 72 hour material extraction period in the process. Glass beads should be included in the flask for smooth boiling action.

See Figure 6 [3.A.I.6] for a diagram showing two extractors (a 2 or 3 liter glass system recommended) used simultaneously to decrease cleaning times. A single Soxhlet extractor may be used in place of the two extractors shown. The extractors are set up in the clean facility.

The cleaning solvent used in Soxhlet extraction is ethyl or isopropyl alcohol. Once extracted with the alcohol, the cleaned items are spread out under a clean operating exhaust fume hood for several hours to air dry. A final drying in a convection oven at 50° to 60°C for 2 hours will complete the process. The cleaned and dry items are stored, unless used immediately, in a bag or cabinet free of contaminants until needed.

To be certified for clean facility use, the extracted items shall have been cleaned in the Soxhlet extractor system for 48 to 72 hours. In addition, as part of the certification process, three of the extracted items are chosen as test samples and their cleanliness is verified. Cleanliness of the items is verified by immersing and thoroughly rinsing the cleaned items in a glass dish containing an alcohol bath, removing the items to allow the alcohol to evaporate, and then testing the alcohol bath residue to determine cleanliness. Testing of the extracted residue is performed through infrared analysis. To be certified for clean facility use, an Infrared Spectrum of the residue extracted from 3 randomly selected *clean* samples shall exhibit a transmission curve of 95% *minimum* throughout the 2.5 to 16 micron range.

An alternative to using the Soxhlet extractor system is to purchase clean facility approved materials. Approved materials can be purchased from the Paramax Corporation, Lanham, MD, or from the Coventry Manufacturing Co., Baldwin Park, CA. Only swabs and wipes from their Diamond series are acceptable. A certificate of cleanliness level should accompany the cleaning materials.

NOTE: The above test, relative criteria and acceptance limits on nonvolatile residue from wipes and swabs is a method used by the Materials Branch. It does not conform to any standard methodology. Alternative methods may be used if approved by the Materials Assurance Office, Code 313.A.

14.0 APPLICABLE DOCUMENTS

OSHA Standards 29 CFR, Part 1910: Occupational Safety and Health Administration

ASTM D 2240: Standard Method of Test for Rubber Property Durometers Hardness

MIL-STD-1209B: Clean Room and Work Station Requirements, Controlled Environment

15.0 ABBREVIATIONS

CofC	Certificate of Compliance
CVCM	Collected Volatile Condensable Material
ESD	Electrostatic Discharge
GSFC	Goddard Space Flight Center
MSDS	Material Safety Data Sheet
PBW	Parts by Weight
PVC	Polyvinyl Chloride
SMC	Standard Materials Certification
TML	Total Mass Loss
VPM	Volts Per Mil

16.0 FIGURES AND TABLES

The figures on pages 32 through 36 are discussed in this document. Refer to page 32 to review Table 1 [3.A.I.1]. [These original page numbers refer to Figs. 1-6 in the original document and Figs. 3.A.I.1–3.A.I.6 here.]

17.0 ATTACHMENTS

The referenced attachments are located at the end of this document.

Table 1. [3.A.I.1]. Properties reference of the polyurethane encapsulating resin and the epoxy primer.

Material	Outgassing [c] %TML	%CVCM	Dielectric Strength [d] VPM 1/16 inch (1.5mm) at 25°C	Glass Transition Temperature, Tg
EN-11-A/B [a]	0.68	0.01	610	-65°C
EPON 815/V140 [b]	0.87	0.05	N/A	N/A

Material	Volume Resistivity Ω-cm at 25°C	Dielectric Constant at 100 Hz at 1 MHz at 25°C
EN-11-A/B [a]	4.3×10^{15}	3.30 2.90

a. EN-11 cured at ambient room temperature for 10 days.

b. Epoxy/Versamid cured at ambient temperature for 18 hours, plus 6 hours at 65°C.

c. ASTM E-595, (Tested at 125°C, 24 hours, 10^{-5} Torr.) Outgassing data control numbers GSC 10592 and GSC 21214

d. Conap Technical Data Sheet, Bulletin P-156

NOTE: The outgassing data for the PR-420 primer is not provided. Primers of this type generally do not pass outgassing. In this case, the primer is covered with encapsulation resin.

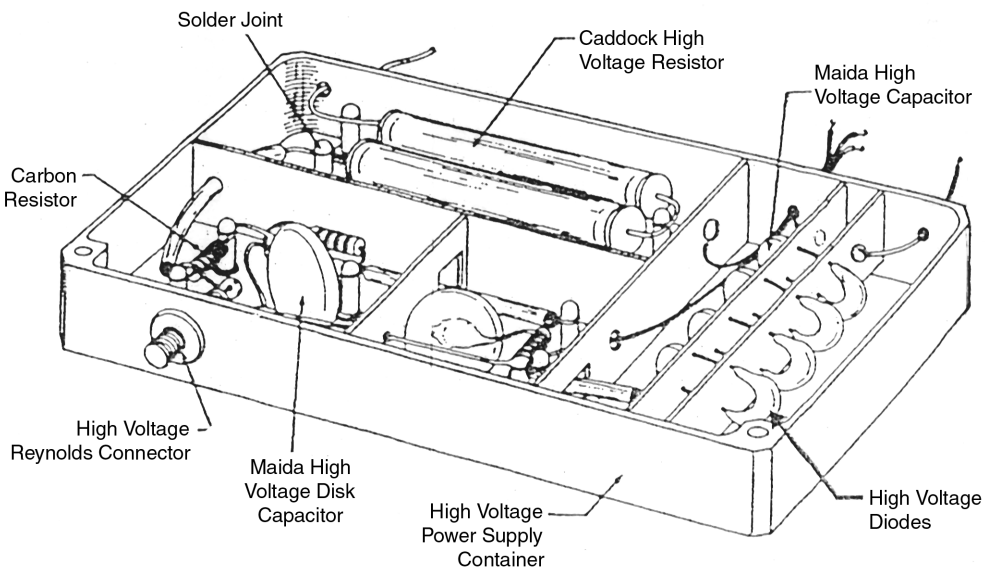

Figure 1. [3.A.I.1]. An assembled high voltage power supply without resin encapsulation.

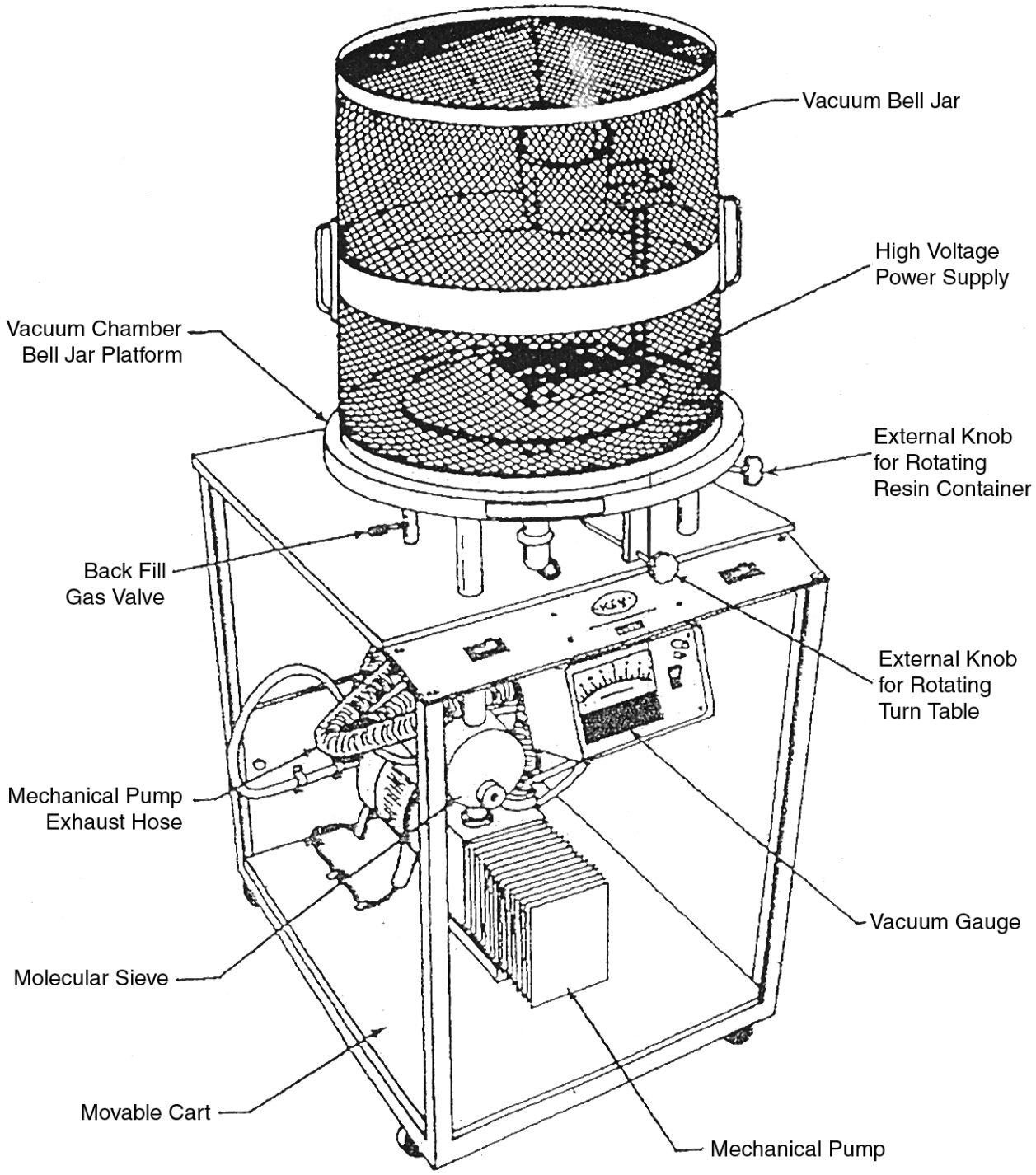

Figure 2. [3.A.I.2]. A customized system used to encapsulate high voltage power supplies in vacuum.

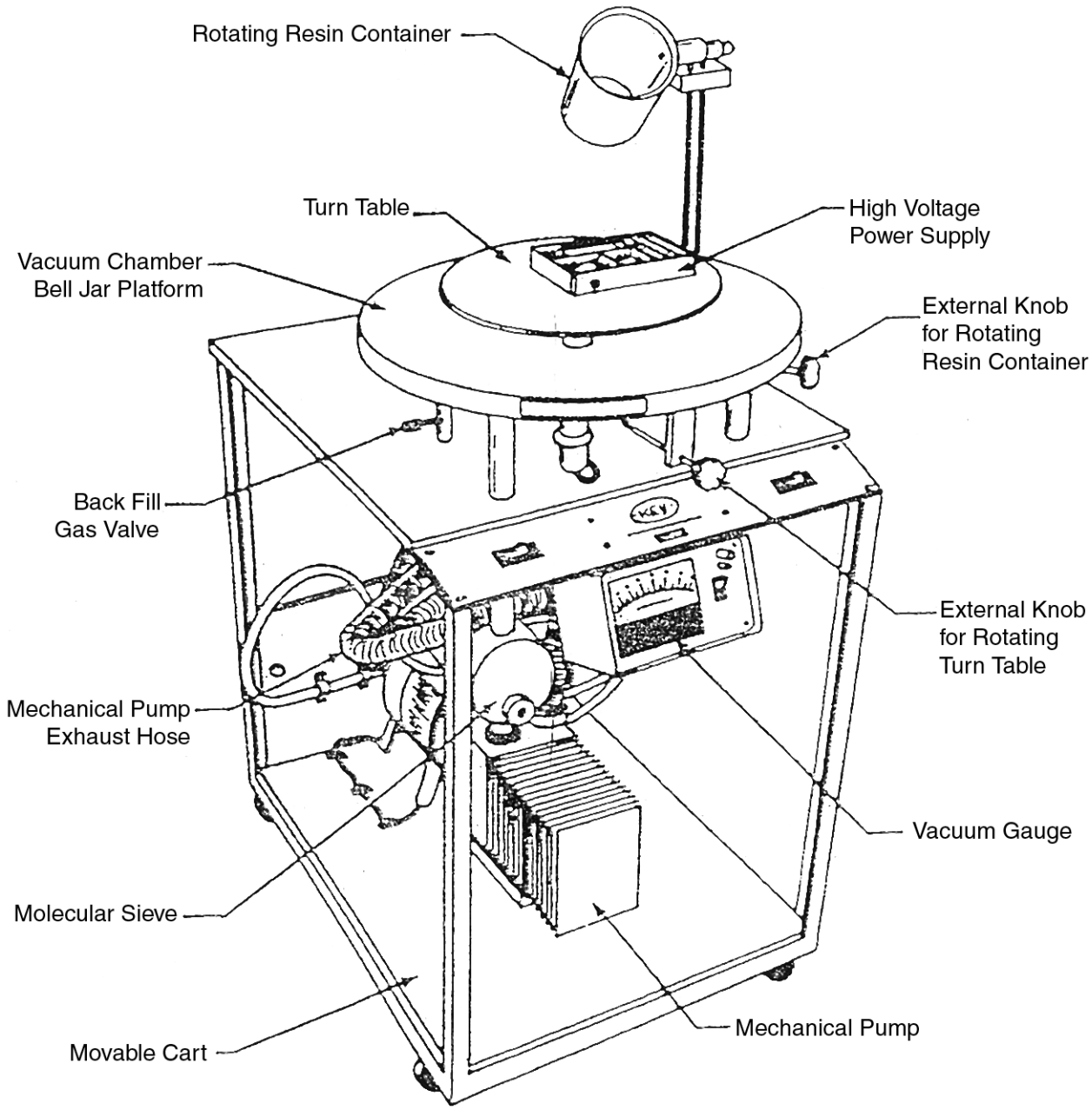

Figure 3. [3.A.I.3]. A vacuum system with a turn table and rotating resin pouring container.

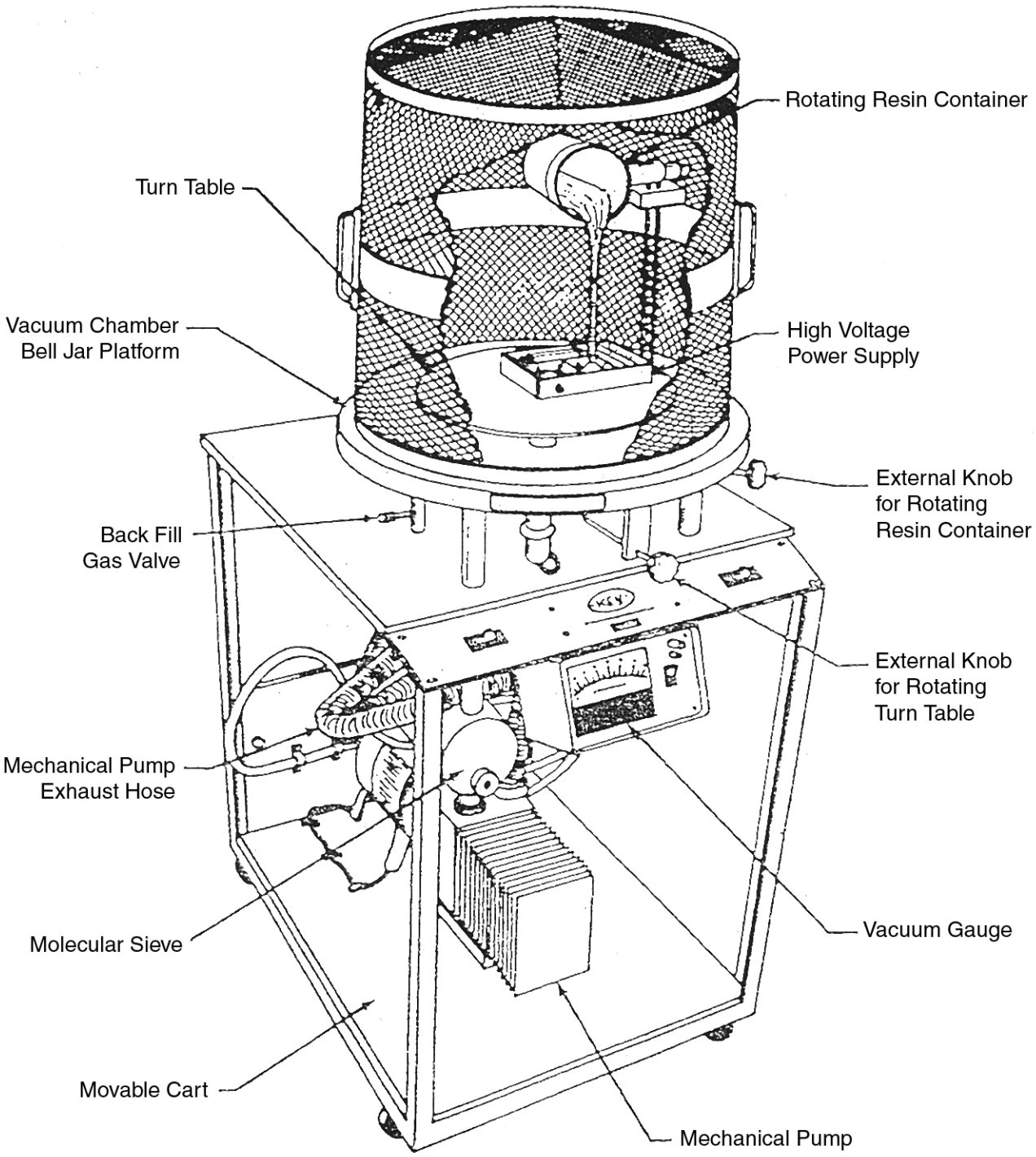

Figure 4. [3.A.I.4]. An illustration of the encapsulation resin being poured under vacuum.

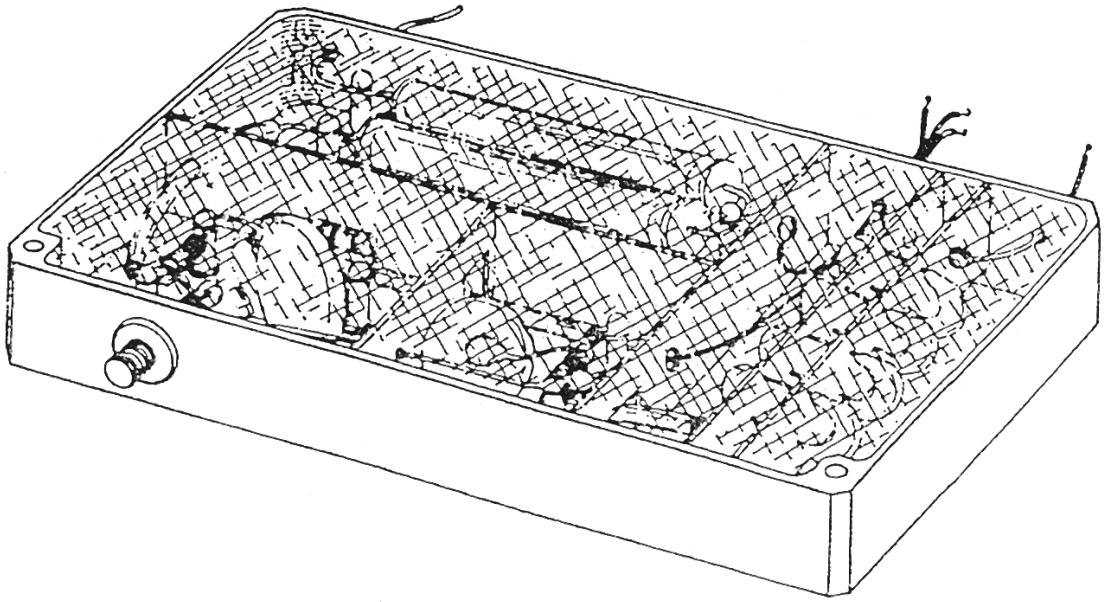

Figure 5. [3.A.I.5]. An assembled power supply encapsulated with a polyurethane resin.

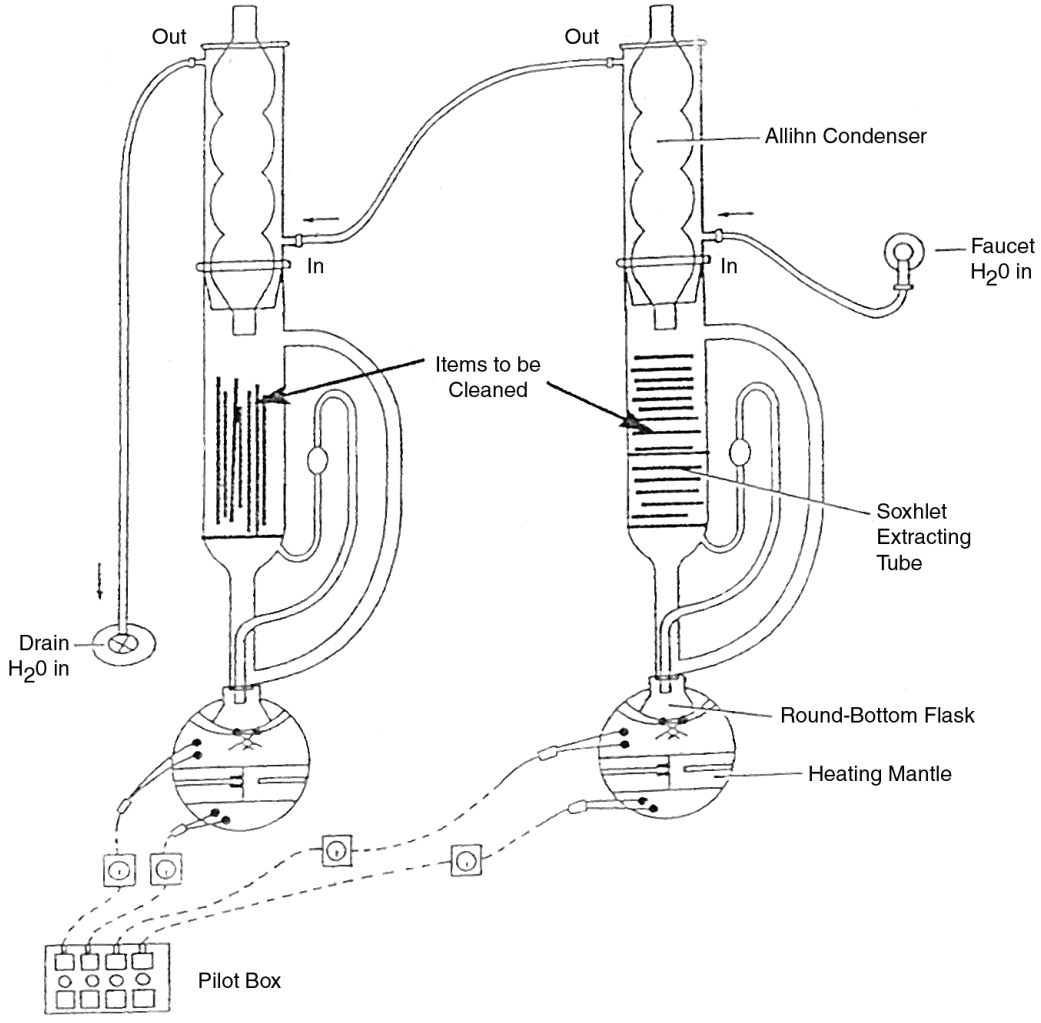

Figure 6. [3.A.I.6]. Soxhlet extractor assembly—two units.

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Appendix II to Chapter 3

PROCESS SPECIFICATION FOR PARYLENE CONFORMAL COATING OF THE CASSINI/CAPS HIGH VOLTAGE POWER SUPPLY

CAPS Process Specification, CAPS-PROC-313-1, Revision

Goddard Space Flight Center

Parylene Conformal Coating of the Cassini/CAPS High Voltage Power Supply

1. SCOPE

This document establishes the procedure to be used for conformal coating of the Cassini/CAPS High Voltage Power Supply (HVPS) with Parylene C.

2. APPLICABLE DOCUMENTS

SPECIFICATION
Goddard Space Flight Center
GC1308729E Box, HVU-1 Power Supply

3. REQUIREMENTS

3.1 Equipment

a. Beaker, glass, 4-liter, from Fisher Scientific or equivalent
b. Polyethylene container, 1-gallon, from local sources
c. Teflon-coated magnetic bar, 1-inch, from Fisher Scientific or equivalent
d. Bink No. 15 spray gun from Binks
e. Timer from local sources
f. Micrometer, 1-inch, from Fisher Scientific or equivalent
g. Tweezers, stainless steel, from local sources
h. Razor blade from local sources
i. Exacto blade from local sources
j. Brush, ½"-wide, non-coductive Nylon, from local sources
k. Sharp-pointed Teflon standoffs (4), 1 to 1.5-inch high, from Code 313 or equivalent
l. Balance, 500± 0.01-gram capacity, from Mettler Instrument or equivalent
m. Magnetic mixer plate, catalog no. 11-500-7SH, from Fisher Scientific
n. Vacuum oven with pressure of less than 300 millitorr from Blue M Electric Co. or equivalent
o. Convection oven, Blue M Model POM588C-3X, from Blue M Electric Co.
p. Convection oven, clean facility, Blue M, from Blue M Electric Co.
q. Exhaust fume hood in Room 140, Building 30, Code 313
r. Class 100 Laminar Flow Bench, Model 530-CS, from Laminaire Corp.
s. Polaroid camera, MP-4, from Polaroid
t. Optical microscope from Nikon
u. Horizontal Parylene Coating Machine, Model 1293, Paratronix

3.2 Materials

a. HVPS per GC1308729E without the low voltage board, from Code 734.3
b. Parylene C from Specialty Coating Systems
c. Organosilane A-174 primer from Specialty Coating Systems
d. Deammoniated Liquid Maskant TC-530 from Kester
e. De-ionized water with resistance value of 18.2 MΩ or better from Code 313 or equivalent
f. Reagent-grade isopropyl alcohol (IPA) from Fisher Scientific or equivalent

g. 200-proof ethanol from GSA or equivalent
h. Reagent-grade heptane from Fisher Scientific or equivalent
i. Temp-R-Tape K102 from Furon, CHR Division
j. Soxhlet-extracted cotton wipes from Code 313
k. Soxhlet-extracted foam swabs from Code 313
l. Latex gloves CR-100 from Baxter
m. Polyethylene gloves from Fisher Scientific
n. Aluminum foil, stock no. 8135-00-724-0551, from Alcan Foil Products or equivalent
o. Dry nitrogen gas, 99.99% pure, from local sources
p. Aclar 22C bags from Clean Room Products
q. Witness coupons, 1" x 2" x 0.001" aluminum strips (7) and 1"x2"x1/16" polyethylene strip (7) , from Code 313
r. Parylene aluminum boats from Code 313

3.3 Procedure for Parylene Conformal Coating

It should be noted that since the low voltage board is removed from the HVPS before the HVPS is delivered to Code 313 for the Parylene coating, ESD precaution is not a requirement for these procedures.

Portions of this procedure shall be performed in the Class 10,000 clean room. The Flight Assurance Manager or Quality Control engineer shall be notified at least twenty-four (24) hours prior to the start of this procedure.

3.3.1 Parylene Coating Equipment and Material Verification

1. Clean and precoat the Parylene Coating Machine with 25-gram of Parylene prior to coating the HVPS.
2. Verify that the chiller will obtain a temperature of less than –85°C, otherwise, the IPA needs to be replaced.

NOTE:
1. ACS-grade isopropyl alcohol has a flash point of 72°F. The Parylene coating process shall be conducted in a well-ventilated area.
2. Prolonged breathing of Parylene vapor fumes should be avoided. An organic vapor mask should be worn if warranted.

3.3.2 HVPS Inspection

1. Inspect the HVPS at 4-10X power of magnification for anomalies, imperfections, contaminants, and broken wires. Any defects shall be reported to Code 734.3 personnel.
2. Take Polaroid photographs of the HVPS prior to coating.

3.3.3 Primer Preparation

The following processing steps shall be conducted under the exhaust fume hood in a class 10,000 clean facility.

1. Place a 4-liter beaker on a magnetic mixer plate.
2. Pour into the beaker 1400cc of de-ionized water, 1400cc of IPA, and 28cc of primer A-174.
3. Place a Teflon-coated magnetic stirring bar in the beaker and cover the beaker with a clean piece of aluminum foil.
4. Turn on the magnetic mixer plate and mix the primer solution for two (2) hours minimum at room temperature.

3.3.4 Cleaning of the HVPS

The following processing steps shall be conducted under the exhaust fume hood in a 10,000 clean facility.

All supporting hardware and materials to be used in this procedure shall be cleaned with a 1 to 1 part by volume of 200-proof ethanol to reagent-grade heptane, air dried, then baked in a convection oven for thirty (30) minutes minimum at 60°C to 65°C. This solvent mixture will be referred to as ethanol/heptane solvent.

NOTE: Clean polyethylene or latex gloves shall be worn at all times during processing of the transformer. Only polyethylene gloves are acceptable for processing with a solvent.

The HVPS shall be cleaned under the exhaust fume hood of the class 10,000 clean facility as follows:

1. Brush gently all surfaces of the HVPS to loosen any contaminant present, using a Nylon brush with the ethanol/heptane solvent.
2. Spray clean the HVPS for two to three minutes with the ethanol/heptane solvent using the Binks no. 15 spray gun at approximately 25 to 35 psi with clean, dry nitrogen gas. The spray gun should be positioned at a 45° angle from the horizontal surface of the HVPS. Rotate the HVPS 90° from its original position until the entire HVPS is spray-cleaned. Repeat this step four (4) times.
3. Blow dry the HVPS surfaces with clean, dry nitrogen gas.
4. Dry the HVPS in air for 5 to 10 minutes minimum.
5. Bake the HVPS between 60°C to 65°C for thirty (30) minutes minimum in a Convection oven.

3.3.5 Priming of the HVPS

The following processing steps shall be conducted under the exhaust fume hood in a class 10,000 clean facility.

1. Place the HVPS in a polyethylene container, 1-gallon size or large enough to hold the HVPS.
2. Pour the primer solution (from Paragraph 3.3.3.4) in the container until the HVPS is totally submerged.
3. Let the HVPS soak in the primer solution for forty (40) minutes ±1 minutes.
4. Remove the HVPS from the primer solution and place the HVPS on three (3) or four (4) clean, sharp-pointed Teflon standoffs. The HVPS components shall be facing down.
5. Allow the primed HVPS to air dry for thirty (30) minutes + 5/-0 minutes.
6. Rinse the primed HVPS with IPA for approximately 2.5 minutes +1/-0 minute to remove primer stains.
7. Blow dry the HVPS surfaces with clean, dry nitrogen gas.
8. Inspect the HVPS surfaces for primer stains. If present, repeat steps 6 through 7 of this section as needed to remove primer stains.
9. Bake the HVPS between 60°C to 65°C for thirty (30) minutes minimum in a convection oven.
10. Place the primed HVPS in a clean Aclar 22C bag and remove it from the clean room for thermal vacuum bakeout.

NOTE: The HVPS must be coated within twenty-four (24) hours after the primer application.

3.3.6 Moisture Removal

The following processing steps are acceptable in a class 300,000 clean facility.

1. Bake out the vacuum oven at a pressure of less than 300 millitorr at 125°C ±5°C for twenty-four (24) hours minimum *prior to* placing the primed HVPS in the oven.
2. Place the HVPS in the vacuum oven with the temperature set between 65°C to 70°C for eight (8) hours minimum. Set the oven's fail safe temperature at 75°C.

3. Close and seal the vacuum door. Close the vent valve. Open the vacuum valve.
4. Remove the HVPS from the vacuum oven after bake-out and let it cool down to room temperature.
5. Place HVPS in the Aclar bag and take it to the clean room. This step will continue as indicated in Paragraph 3.3.8.

3.3.7 Preparation of the Parylene Coating Machine

The following processing steps are acceptable in a class 300,000 clean facility.

1. Turn on the chiller, vaporizer, and furnace heaters for at least one (1) hour before coating.
2. Fabricate three (3) Parylene C boats (2" x 8" x l") from clean aluminum foil.
3. Fill each boat with 70 g of Parylene C. The 210 g of Parylene C will provide an approximately 1.5 to 2-mils of Parylene coating of the HVPS.

3.3.8 Masking of the HVPS

The following processing steps shall be conducted in a class 10,000 clean facility.

Masking shall be performed immediately after the bake-out process. The procedure is as follows:

1. Remove the HVPS from the Aclar bag in Paragraph 3.3.6.5.
2. Mask the surfaces of the HVPS per Drawing No. GC1308729E and details (Figures 1–3 [3.A.II.1–3.A.II.3]) instructions from Code 734.3's Cassini/CAPS personnel, using the Temp-R-Tape K102 and Maskant TC-530.
3. Verify that the masked areas are in compliance with the instruction prior to the Parylene coating.
   NOTE: *This inspection must be performed by Code 734.3's Cassini/CAPS personnel.*
4. Place the masked HVPS in a clean Aclar bag and remove it from the clean room for Parylene coating.

3.3.9 Parylene Coating of the HVPS

The following processing steps are acceptable in a class 300,000 clean facility.

1. Remove the HVPS from the Aclar bag in Paragraph 3.3.8.4. Place the masked and primed HVPS on three (3) or four (4) sharp-pointed Teflon standoff. The HVPS shall be on the center shelf and in the center of the Parylene deposition chamber.
2. Label all 18 witness coupons, measure, and record the thickness of each coupon.
3. Place three (3) aluminum witness coupons and three (3) polyethylene witness coupons in the chamber, one each on the center shelf and, one directly above it. Place one (1) aluminum witness coupon and one (1) polyethylene witness coupon on the shelf directly below the center shelf.
4. Close the chamber door.
5. Place one (1) Parylene C boat (from Paragraph 3.3.7.3) in the vaporizer tube and close the endcap.
6. Turn on vacuum for 20–30 minutes and verify that the vacuum has reached 5μm or less on the T_c gauge and 5μm on the ion gauge before turning on the vaporizer.
7. Slide the heater over the vaporizer tube to start the vaporizer. The vaporization will start at approximately 135°C to 140°C. The vaporizer pressure on the ion gauge shall be between 30–40 μm.
8. Continue until the Parylene is depleted. The Parylene can be observed by sliding out the vaporizer heater.
9. Turn off the vacuum valve, and back fill the chamber.
10. Open the chamber door to remove two (2) witness coupons (1 aluminum and 1 polyethylene) from the shelf directly above the center shelf, where the HVPS is, and from the center shelf.

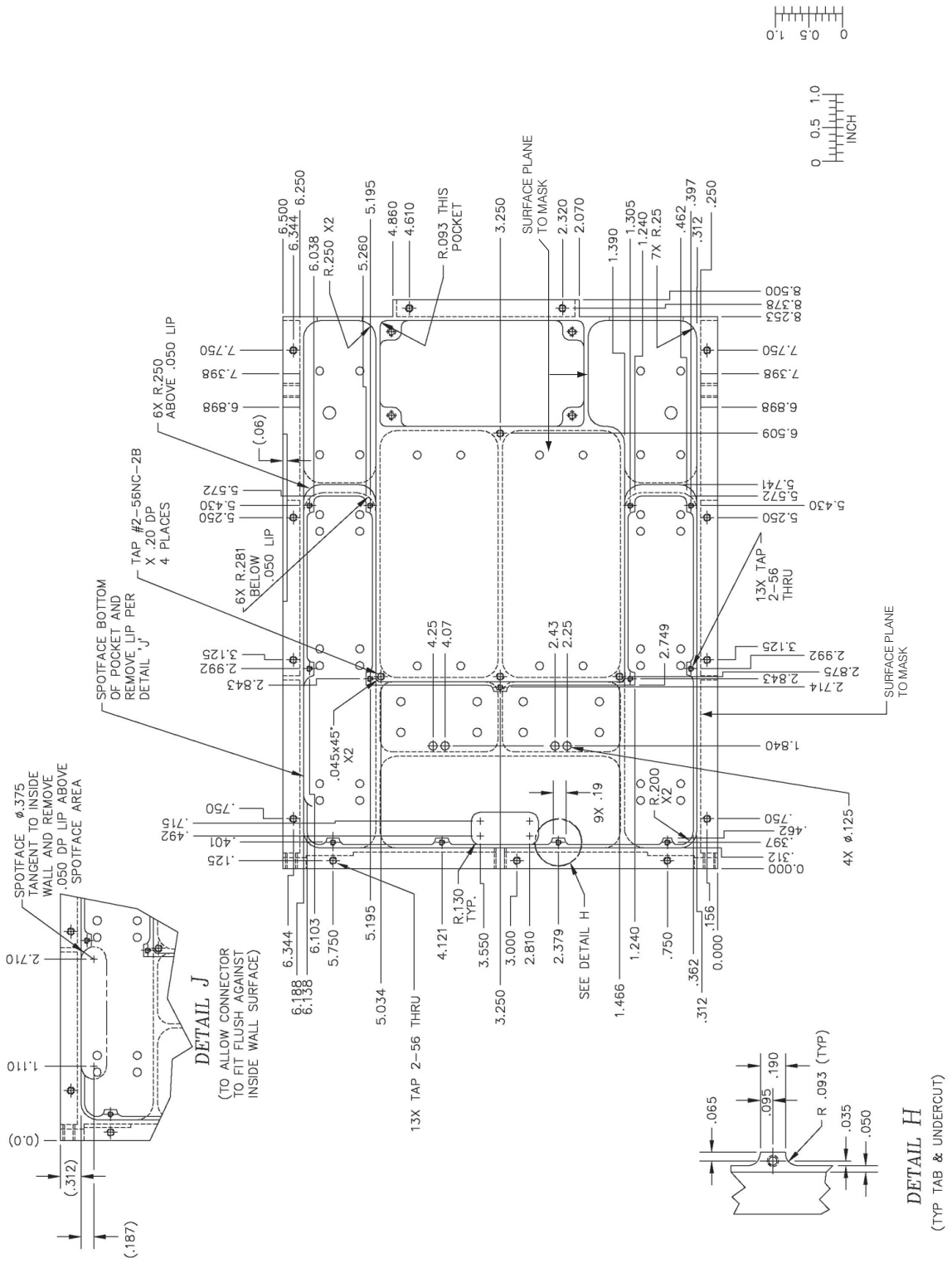


Figure 1. [3.A.II.1]. HVPS bottom view—Mask mounts.

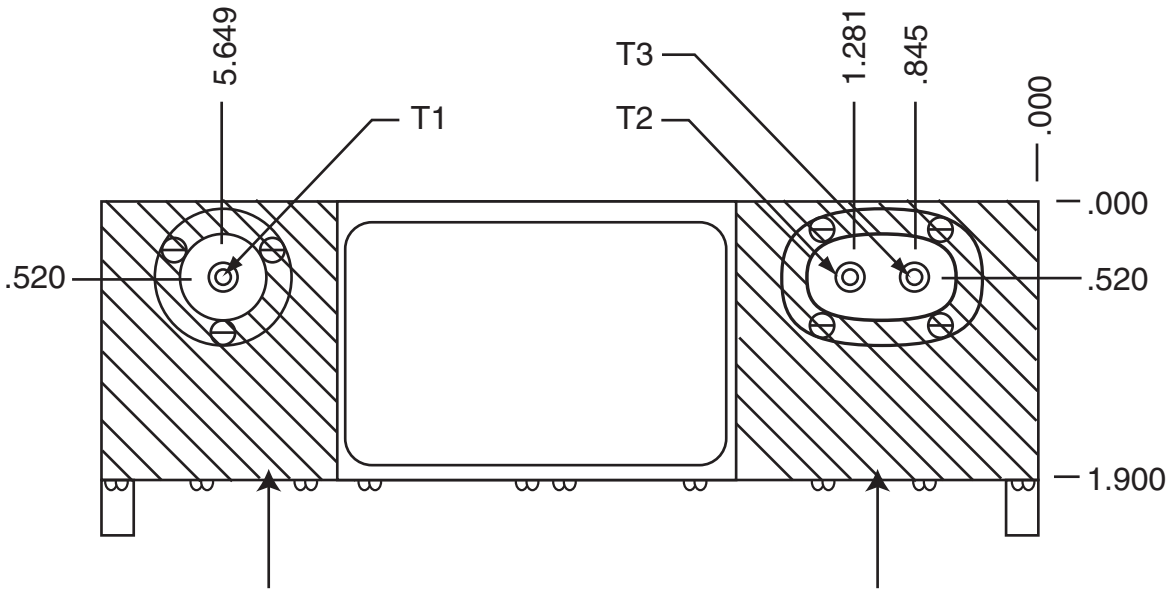


Figure 2 [3.A.II.2]. Cassini/CAPS High Voltage Unit-1. Output ends detail.

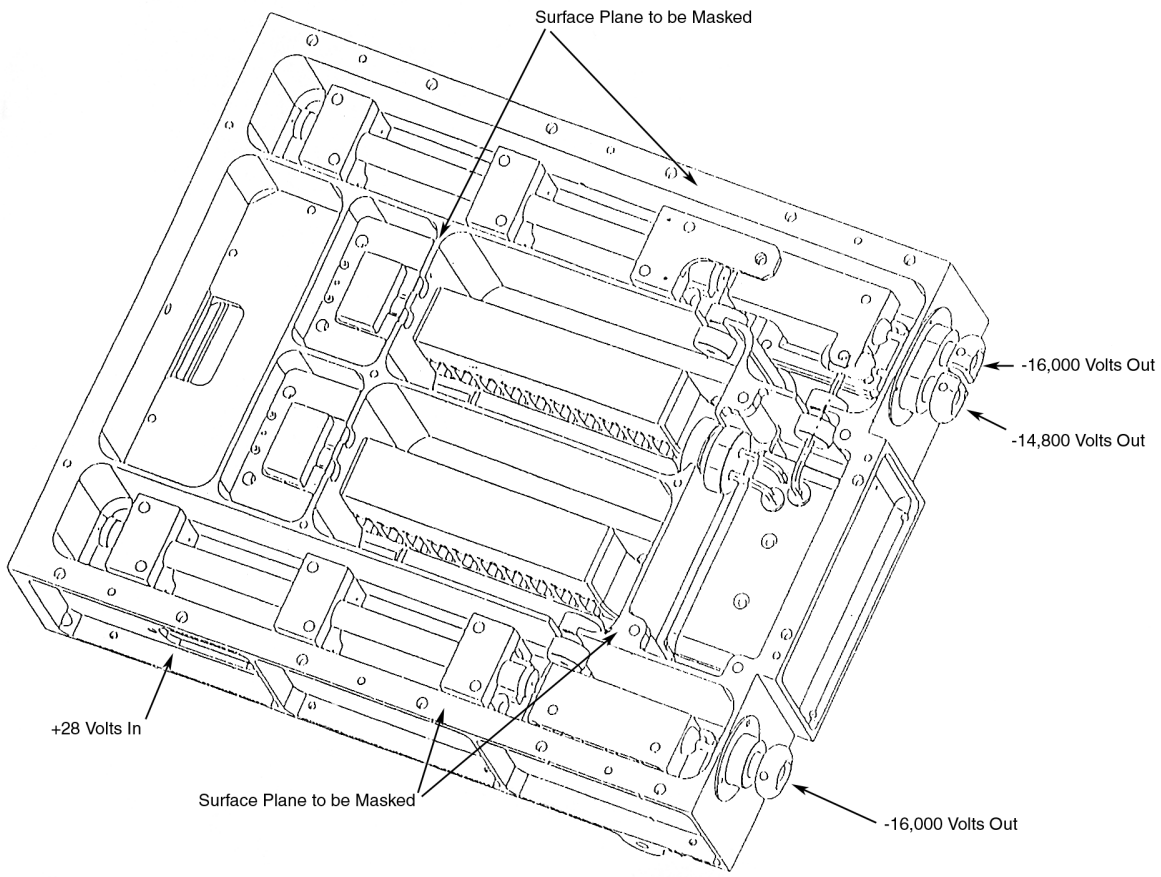


Figure 3 [3.A.II.3]. HVPS, HV-Side

11. Measure the thickness of the witness samples using a micrometer. Determine the Parylene coating thickness. Use this thickness to calculate for the amount of Parylene necessary to put on a total of 1.5 to 2 mils coating on the HVPS and, thus, the number of times to repeat the coating process (see Paragraph 3.3.9.16).
12. Close the chamber.
13. Remove the endcap on the vaporizer tube.
14. Remove the boat and place another boat containing the 70 grams of Parylene.
15. Close the endcap.
16. Repeat steps 6 through 13 of this section as necessary.
17. Verify that the last witness coupons on the center shelf have an approximately 1.5 to 2-mil of Parylene coating.
18. Remove the HVPS from the chamber.
19. Turn off the chamber controls for the chiller, vaporizer, and furnace heaters.
20. Place the HVPS in a clean Aclar bag and carry it to the class 10,000 clean facility.

3.3.10 Removal of Masking Tape from the HVPS

The following processing steps shall be conducted in a class 10,000 clean facility.

1. Remove the Temp-R-Tape K102 from the HVPS using the Exacto blade to cut the Parylene at the tape edge to prevent delamination and feathering. Cutting shall be performed under the microscope at 4-10X magnification. Use a tweezer to lift the tape while cutting the Parylene. Trim all areas of feathered Parylene by using a tweezer and an exacto blade.
2. Clean the unmask areas with either extracted wipes or extracted foam swabs that have been dampened in ethanol. This process will remove tape residue and the primer.
3. Let the HVPS air dry for 5 to 10 minutes.
4. Place the HVPS in a clean Aclar bag and remove it from the clean room.

3.3.11 Preparation for Delivery

The following processing steps are acceptable in a class 300,000 clean facility.

1. Remove the HVPS from the Aclar bag.
2. Take Polaroid photographs of the Parylene-coated HVPS.
3. Place the HVPS back in the Aclar bag.
4. Place the bagged hardware in the original bag the HVPS was delivered in; the later bag shall have been precleaned with wipes dampened in ethanol and blow dried with nitrogen gas.
5. Complete a Code 313 Work Request for Polymeric Processing.
6. Record the related processing information on the certification log and enclose one aluminum witness coupon from the final coat indicated in Paragraph 3.3.9.17, and the photographs indicated in Paragraphs 3.3.2.2 and 3.3.11.2.

4. QUALITY ASSURANCE PROVISION

4.1 Inspection

Quality Control shall visually inspect for air bubbles, delaminations, etc., of the Parylene coating. Quality Control shall also verify the coating thickness of the witness coupons from the final coat indicated in Paragraph 3.3.9.17.

5. NOTES

5.1 All cotton wipes and swabs shall be Soxhlet-extracted and oven-dried prior to use. These processes shall be performed by Code 313 personnel.

5.2 Material Safety Data Sheets (MSDS) shall be reviewed prior to handling of or processing with the solvents and materials specified in this document.

Chapter 4: High Voltage Parts

General Comment

Identification of commercial products and equipment to adequately specify or document the high voltage design does not imply recommendation or endorsement, nor does it imply that the product and equipment identified is necessarily the best available for one purpose.

I. High Voltage Parts: Passive Parts

This can only be a superficial survey, trying to touch on some of the most important and obvious topics since each type of part is an entire study in itself.

High voltage parts are capacitors, resistors, transformers, diodes, feedthrus, connectors, standoffs, cables, etc. There are no reliable high voltage relays or switches for space. For space use, the high voltage parts should be solid, without any trapped gas—if at all possible. Much of the "corona" testing activity is concentrated at the parts level since it is much easier to identify location and causes of failure at the parts level than in a completely assembled HV power supply. See Chapter 5.

Specification to which various parts types should be ordered are either Goddard Space Flight Center Preferred Parts List (PPL) or military specification. Even these do not eliminate all the difficulties that might arise.

A. HV Resistors

HV resistor bodies must be solid, not hollow. They must be of low inductance construction and low temp coefficients. Some types that have been flown successfully are:

Manufacturer	**Type**	**Goddard Spec.**
Victoreen	MOX 1125-23 MOX 750-23 MOX 400-23	S-311-P-672
Caddock	MG (Precision) and Low Inductance	S-311-P-683
Caddock	TG (Precision) Low Inductance and Low Temp. coefficient	S-311-P-741 S-311-P-742
RPC	BBMW	
IRC	RHV	MIL-PRF-49462B

One of the questions that has arisen is whether primer coats before potting affect the precision resistance of high resistance devices. Obviously this depends on the resistance, but testing carried out with 200 Megohm Caddocks of both the MG and TG types showed that *thin* primer coats of PR420 or of Epon 828/Versamid 140 epoxy, which are good primers for polyurethanes, do not spoil the ±1% precision. Thick primer coats of the epoxy do spoil the tolerance. It is also important to ensure that after the manufacturer is finished with his testing program where he

uses *silicone_oil* to immerse the resistors, that all traces of silicone oil have been *removed* by vapor degreasing before delivery. Otherwise there will be poor adhesion upon potting. Also, low temperature coefficients of resistance are, of course, very important.

B. HV Capacitors

Again, for space use, the body of the capacitor must be solid. Therefore, thin film high voltage capacitors can not be used, either the cylindrical hollow types or even the so-called encapsulated flat types which still have air gaps between film layers.

So, what can be used are ceramic single disc types, or after much testing, (see later), ceramic multilayer types or resin-impregnated mica paper types.

Some types, that have flown successfully, are:

Manufacturer	**Type**	**Specification**
Maida	Single disc ceramic	S-311-P-15C(D) (Goddard)
Calramic Technology LLC, formerly KD/Center Electronics	Multilayer, Monolithic Ceramic	MIL-PRF-49467B, since May 2001
TDK	Single disc Strontium Titanate, very thick	
Custom Electronics	Resin impregnated mica paper (much larger than the Ceramics). Useful as output filter caps above 10 kV.	Flying in HRS supply on Hubble Space Telescope
Johanson Dielectrics		

Capacitors should be DC or even AC Partial Discharge tested among other tests. They must be derated to 60% of the manufacturer's rated voltage; the multilayer capacitors should be derated to 50% of the manufacturer's.

Maida single disc $BaTiO_3$ ceramic capacitors (the X5R or X7R formulation) have been flown successfully up to about 10 kV DC for up to about 2000 pF capacitance. When the voltage and/or the capacitance gets much higher, then there have been instances of failures. This is because when the discs get too thick, the shear stresses of the piezoelectric material causes cracking. Or when the manufacturer tries to supply Z5U formulation, the capacitance, or C-characteristics are very variable with respect to temperature and voltages.

The coating on the ceramic capacitors must be fluidized-bed epoxy, compatible with potting. This coating must preserve high resistance characteristics at high temperature extremes (meaning at least to 85°C) and must not crack at low temperature extremes (at least as low as –35°C). Mil specs demand temperature ranges from –55°C to +125°C, and the problems which ensue from this requirement have prevented ceramic coated capacitors being available to Mil specs. Potted ceramic caps for high voltages must be avoided, because the manufacturers do not vacuum pot, and they include objectionable bubbles in the potting, and they also do not put enough potting between the ceramic chip and the top of the potting shell.

When the high voltage ceramic multilayer capacitors first appeared on the market, some failures and difficulties were encountered with them. There were strenuous testing programs and "Evaluations." An example of this is seen in Appendix I to this chapter (Chapter 4), Ref. [1] (1993). By May 2001, experts in the field added an AC corona test to MIL-PRF-49467B as seen in Ref. [2]. The authors of this HV Guide very much approve of this, contrary to Ref. [1]. It must be remembered, however, that the MIL-PRF-49467B is (a) for ground-based use where equipment can be easily repaired, and that it includes (b) manufacturers' encapsulation which is sometimes not done carefully enough for space. The multilayer capacitors should be ordered either bare or coated with fluidized-bed epoxy.

Various configurations of plate design in HV multilayer capacitors are reproduced (greatly enlarged) as Figure 4.1 taken from Ref. [1]. The series parallel configuration is more reliable and reduces the electric field at the tips of the plates.

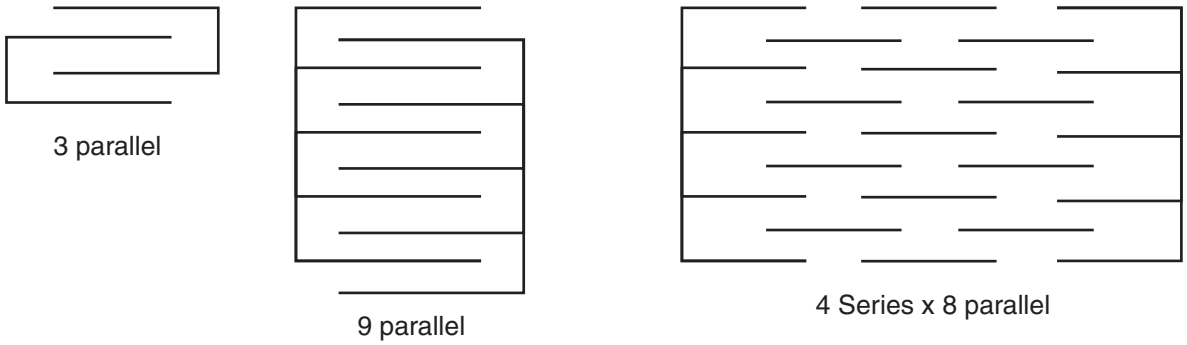


Figure 4.1. Different plate designs in high voltage ceramic multilayer capacitors, Ref. [1].

The design engineer of the HV power supply will still request the HV capacitors to be "screened" or 100% acceptance tested. The screening contractor has an established set of tests whose sequence and repetition frequency can be modified slightly. One version of the tests is shown in Table 4.1. This is a somewhat changed version from Ref. [1]. The screening contractor may also do destructive physical analysis (DPA) on a small sample from a given lot.

Table 4.1. Screening test methods for HV ceramic multi-layer capacitors, adapted from Ref. [1].

Test	Standard/Spec.	Test Condition
0: Visual	MIL-C-123	3 to 10x Magnification
1: Capacitance & Dissipation Factor	MIL-STD-202	For X7R dielectric: 1 V at 1 kHz For NPO dielectric: 1 V at 1 kHz except for C < 1000 pf, then 1 MHz Fail: Cap: outside of tolerance DF: > 2.5% for X7R, and > 0.2% for NPO
2: Insulation Resistance	MIL-STD-202	500 V DC applied; Fail: below limit of 100 GΩ at 25°C and below 10 GΩ at 85°C except where C> 10,000 pf, then 66 GΩ and 6.6 GΩ respectively
3: Dielectric Withstanding Voltage	MIL-STD-202 -Dielectric -Body	Ramp voltage to 100% rated voltage in 1 min. between the leads. Dwell 5 s max. Fail: Current > 1 μA. Ramp to 500 V DC, applied between metal leads and metal tape wrapped around body
4a: De-age or de-polarize at 85°C for 12 h with leads shorted.		
4b: DC Partial Discharge	Adapted from ASTM D 1868-81& IEEE STD 454-1973	Stepwise ramps & plateau sequences; the pulse and total charge sum data from 0 to half-rated voltage, half-rated voltage to full rated voltage, at the quiescent plateau, and from rated voltage to 0. See Chapter 5.
5: AC Partial Discharge	Adapted from ASTM D 1868-81& IEEE STD 454-1973	Ramped 60 Hz AC voltage until 100 pC pulses are detected. Dwell there no longer than 5 s. No measurement above 70% of the DC rated voltage (equivalent in rms volts)
6: Temperature Cycling	MIL-STD-202	5 cycles from –55°C to +85°C for Cycling screening.
7: Voltage Conditioning	MIL-C-49467	Ramp voltage to 100% DC rated voltage (DWELL length decided by Design Eng.)
8: 85°C/85% Relative Humidity	MIL-C-123A	Electrical measurements; do not exceed limits above. Capacitance delta not to exceed 10%. Low voltage test.

Test 4a and 4b *or* 4a and 5 can be repeated, either at atmospheric pressure with the capacitors immersed in FC-43 Fluorinert liquid, or in vacuum at 10^{-6} torr. For screening, go only to 100% V_{rated}.

A brief mention of the types of designation of ceramic materials, most of which contain a certain amount of $BaTiO_3$, follows. These designations are X5R, X7R, Z5U, NPO or else BX, COG, etc., and these have to do with ΔC, capacitance *change* due to temperature *change*. It also follows that the dielectric constants of the different materials are different, and that the change of capacitance with applied voltage change is different. In addition, confusion arises as to whether the Specification is MIL-Spec. or EIA. In general, COG equals NPO, and BX includes X5R and X7R characteristics. It is best to request literature from the manufacturers themselves, such as, for instance Technical Bulletin No. 792, "Understanding Chip Capacitors" by Johansen Dielectrics, Ref. [3]. To give an idea of the enormous differences of dielectric constants of ceramic capacitors, see Table 4.2:

Table 4.2. Approximate dielectric constants of ceramic capacitors.

Designation	NPO Class I	BX Class II-mid K	X7R	Z5U Class II-high K
Dielectric constant	Less than 150	1000–2000	1000–2000	4000–7000

In general, the NPO ceramic has the least percentage change in capacitance with temperature. But also, partial discharge tests, being very revealing for X7R, X5R, and Z5U capacitors, are not very useful for NPOs other than that no partial discharges may be tolerated at all.

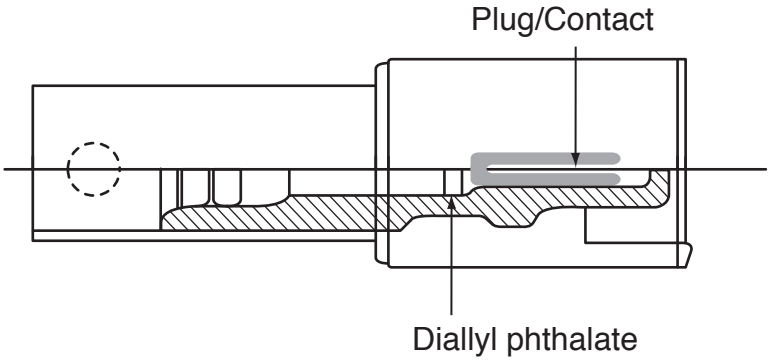
C. Connectors

A connector that is mated on the ground is necessarily filled with air at atmospheric pressure. Then, depending on the leak-rate from the shell of the connector, where the cable enters or at the mating interface, the pressure of the air within it will get down to the "critical corona region" at some indeterminate time in orbit. This will then cause a metal-to-metal (center-pin to grounded shell) continuous gas discharge within the connector. This will happen no matter how double-backed or convoluted the charged particle path is from high voltage center-pin to grounded metal shell. Two approaches to prevent this can be tried:

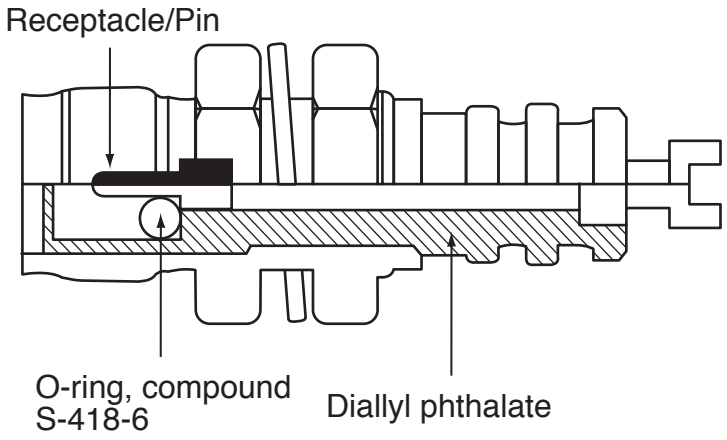
(1) Vent the connector by drilling holes through the shell.
(2) Interrupt the metal-to-metal gaseous path with a tight fitting insulating solid seal. Then one will get only occasional small partial discharge pulses instead of a continuous current or an arc.

The interrupting solid seal must, of course, be elastic and maintain its elasticity (no thermal set), despite many thermal cycles from –55°C to at least 85°C. The above discussion is usually talked about in terms of "creepage path" by the connector manufacturers instead of the "gas discharge" language of the physicists.

Reynolds Industries of Los Angeles, California, developed such an interrupting seal, Ref [4], in the form of a Silastic O-ring in the receptacle of a single pin connector. This is in their Series 600 connector, which is in addition clad internally, as well as the nose of the female plug, with Diallyl Pthalate insulator. This connector has been intensively tested in vacuum in the corona region at Goddard Space Flight Center, Ref [5]. Such tests require opening and closing the connector while inside the vacuum system at corona region pressures, from the outside of the vacuum system via a movable vacuum penetration. Then, being sure the connector has the worst possible pressure inside, high voltage is applied and partial discharges and/or continuous current, if any, are measured. Tests have been successful to 6 kV DC, and many of the Series 600 have flown. See Figure 4.2.



a) Female connector P/N 167-3770 A



b) Male panel connector P/N 167-3771

Figure 4.2

Reynolds Industries wrote a short history of their high voltage connector development. Reynolds has now brought out Advanced single-pin high-voltage connectors with molded, multiple interface seals in the receptacle male portion of the connector. However, none of these have been tested at GSFC as described above, and none of these have flown on GSFC missions. The manufacturer's ratings claim to go to 25 kV DC on these Advanced connectors.

D. HV Cable

There are many dielectric insulation types used, e.g., polyolefin, Teflon, Kapton wrap, silicone rubber, some shielded and some not. For voltages above 10 kV, the cable should have "corona strand shielding." That is, a semiconducting black material should fill the space between the metal center strand and the *inside* of the dielectric insulation and is also coated onto the *outside* of the dielectric insulation before the metal shielding braid is applied coaxially. The jacket outside the shielding braid (this braid *must* be grounded) should adhere to potting, or if made of Teflon, must be pre-etched.

It must be kept in mind that Teflon and especially silicone rubber cold-flow. Sharp right-angle and hair-pin bends must be avoided. Whereas silicone rubber HV cable is nicely flexible for work in the laboratory and on the ground, it should *not* be used in flight modules because it is more troublesome as to cold-flow and pin-holes than any other dielectric insulating material.

At the *cut* end of the cable, the metal shield and the outside anti-corona coating must be peeled back or removed at least 1.5 inches from the cut. Follow manufacturer's directions for cable-to-connector assembly, but *no shrink tubing* may be used.

Within a HV power supply thick *bare* bus wire can be used, properly spaced with respect to openings in shielding partitions and away from grounded terminals. The potting will do the insulating. HV cable is then only needed at the HV output and proper attention then needs to be given as to how it exits through the shielding box via a HV feedthrough.

A few additional rules for HV assembly with cables or bus wires are:

1. Solder balls must be used at all HV junctions, and sharp points are prohibited.
2. Even dielectrics and insulating materials should have smooth rounded edges.
3. Corona balls or corona doughnuts are advisable.
4. Parts and wiring should be mounted *up off the circuit board* with mechanical stress relief wires so that potting or alternatively coating can get *under* the high voltage part and not lock in a layer of air under the part. Also no shrink tubing or sleeving on cables or bus wires are allowed.
5. However, if the entire construction is board-mounted or hybrid construction, such as for voltages below 3 kV, then parts have to be used and ordered especially for that construction with the suitable terminations. As a specific example, if ceramic multilayer chip capacitors are to be mounted with the bodies parallel to the board, then only a very thin coating with preferably Parylene is allowed, leaving a gap of one or two mils between the coated body of the capacitor and the coated circuit board. Rigid gluing of the body of the capacitor to the circuit board is not allowed because that would cause it to shear and crack due to thermal stresses when thermal cycling occurs.

E. High Voltage Circuit Boards and HV Standoffs

Most of the parts and components of high voltage power supplies for space applications are mounted on circuit boards. As already noted in earlier HV guide books, Ref [6], "the most popular board materials are epoxy-impregnated fiberglass, types G-10 and G-11." Polyimide impregnated fiberglass boards, G-30, are used for higher voltages. When circuit trails are printed on the G-10 or G-11 boards, they have relatively sharp edges, and also water vapor absorbs on the surface of the boards. This causes the flash-over voltage along the surface of the board from one trail to the neighboring one to be about 2 kV/mm at 50% relative humidity and atmospheric pressure. The practical limit for uncoated boards with reasonable (1 cm) conductor spacing seems to be about 20 kV. This can be improved considerably by vacuum bake-out, followed immediately by coating with polyurethane or Parylene vacuum deposition.

For the higher voltages, e.g., 25 kV, G-30 boards are used and the parts and connecting wires are mounted up off the G-30 boards on high voltage stand-offs. The connecting wires on any one board are usually bare bus wire; insulated cable with shielding is only used to connect one board to another, or as output cable to the instrument. Later potting of the entire HV portion serves to insulate the bare bus wire. The stand-offs are usually made with porcelain or Teflon insulators between the top metal solder terminal and the bottom metal screw for attaching to the circuit board. Above approximately 10 kV, it is desirable to have the bottom screw and the locking nuts made of plastic, such as polycarbonate, since the high voltage electric fields will induce high voltage onto them, even though they are insulated from the top solder terminal. For the same reason, the holes into which the bottom screws are attached, must be vented, so they can thoroughly outgas. Teflon stand-offs have to be *pre-etched* for subsequent adhesion to potting or coating. Every part, such as resistors and capacitors and diodes, etc., has to have its own mechanical stress relief bend in the connecting leads.

When hybrid type of construction and assembly was first attempted for the lower HV supplies, up to about 2 or 3 kV, with the bodies of the parts rigidly adhered to ceramic boards with conformal coating, this was at first unsuccessful.

The reason was that special precautions were not taken to prevent thermal stresses during temperature cycling, causing cracking of solder joints or ceramic boards or even breaking of ceramic multilayer capacitors.

More recently, for voltages below about 3 kV, a so-called Flex Board is being used, made of a layer of 0.002 inches of Kapton Flex between two layers of rigid polyimide. See the multicolored figure in Chapter 5, Appendix III. It is undergoing extensive testing. Metallic trails are printed onto the Flex Board; see Figures 7.I.1 and 7.I.2 in Chapter 7, HVBS (I), ADC/GLAST. After assembly, it is Parylene-coated with a 1 mil thick vapor deposition. Great care is being taken to have several mils spacing between the bodies of board-mounted parts, such as ceramic chips capacitors and diodes, and the Flex Board. In fact, parts such as high voltage diodes, can now be purchased either for axial mounting with the usual axial wire leads, or for board-mounting with "surface mount square tabs" for soldering to the trails. The "square tab" serves as a stress relief and prevents the body of the diode from lying directly on the board surface. Inquiry about the Flex Board and trails was made to Dupont Flexible Circuit Materials in Research Triangle Park, North Carolina.

II. Transformers

A. Introduction

Faraday's and Ampere's laws govern high voltage transformer operations just as in low voltage ones. In addition, parasitics and distributed parameters play a dominant role because of the high turns ratio and the very large number of secondary turns. The equivalent circuit is shown in the Figure 4.3 together with some "ball park" values for the distributed parameters.

The C's come from the interwinding capacitance. It is also determined by the dielectric constant in which the windings are immersed, that is $K_e = 1$ if *not* potted, and K_e is somewhere between 2 and 4 depending on the potting compound.

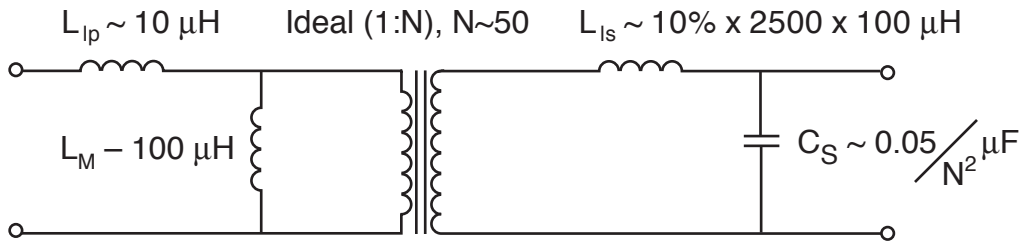
The coupling coefficient between primary and secondary is 90% or better when the windings are wound concentrically such as in a Ferrite pot core transformer. But the coupling coefficient may only be 60% when gapped Ferrite C-cores or U-cores are used with windings separated on opposite legs of the core. The leakage inductance thus created gives rise to L_{LP} and L_{LS}, in Figure 4.3. A converter topology must be chosen to accommodate the large leakage inductances.

The formula for the resonant frequency ω_0 (where $\omega_0=2\pi f_0$), as shown in the Figure 4.3b of the primary tank network, is

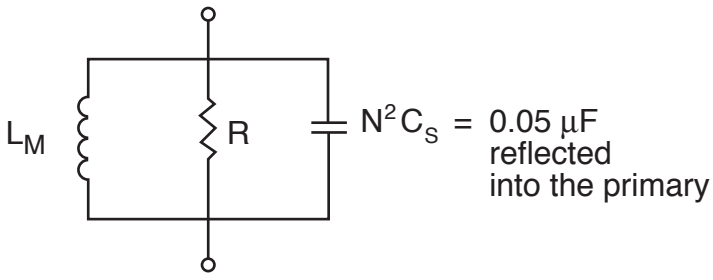
$$\omega_0 = \frac{1}{(L_M N^2 C_S)^{1/2}} \text{ and } Q=\omega_0 N^2 C_S R.$$

This is an example of parallel resonance, and the impedance is highest at resonance; thus, the current drawn is lowest when driven at resonance. On the other hand, the higher the frequency of operation away from resonance, the lower the impedance and the input current drawn is higher. This can happen just due to temperature cycling between –35°C and +85°C which causes the distributed parameters to change.

In general, secondaries above 2 kV, measured from zero-to-peak (0-pk), require special attention. (Some have flown as high as 10 kV, 0-pk, on UIT.)



(a) First order approximation



$$\omega_0 = \frac{1}{\sqrt{L_M N^2 C_S}} ; Q = \omega_0 N^2 C_S R$$

(b) Primary tank network: parallel resonance

Figure 4.3. Equivalent circuit of an HV transformer.

Selection of *number of turns* is based on:

1. Desired resonant frequency; nowadays, this is 100 kHz rather than the former 20 kHz.
2. Desired output voltage predominantly determines number of turns, and the coupling coefficient and loading need to be factored in.
3. Ferrite Core material, style, size, gap, most commonly used.
4. Desired C_s.
5. Wire Size: Wire thinner than AWG 38 is very difficult to wind. This small wire size causes no problems as far as overheating is concerned in the secondary, if the power supply purpose is biasing rather than delivery of current. Potting the secondary further helps by conducting or spreading the heat around. (Thermal conductivity of potting polymers is low, but is higher than for vacuum!)
6. The winding method must accommodate the necessary winding to winding voltage limit, potting accessibility, and interwinding capacitance control. Thus, winding method should be loose, such as "lattice" winding or "bank" winding even if it decreases coupling. Layer separation may be incorporated using a porous glass fiber or polyester mat material.
7. Impregnation material considerations—see discussion below.
8. Partial Discharge (Corona) test considerations.
9. HV breakdown considerations determine whether pot core or C-cores are used.

Spacing from HV winding to other windings and to the core follow the usual guidelines, that is, there should be no more than 50 V/mil average field strength at most.

It is also highly desirable to limit the voltage between adjacent layers of windings in the secondary to 200 V, so that even if the impregnation with potting has an inadvertent void, there will be no corona in the void if the voltage across it is below the Paschen minimum voltage.

B. Design Sequence

Design will involve interactive processes:

1. Select approximate core size and material. Use Ferrite material *below* the Magnetic Field Strength, B, of 1000 gauss.
2. Determine primary turns from Faraday's law.
3. Determine secondary turns from turns ratio and wire size.
4. Estimate size of secondary winding based on items 4–9 on previous page. Check fit on selected core.
5. Determine gap and the resonance capacitor. Build a transformer and try it. The larger the secondary windings volume, the lower the V_s output voltage. Try to keep C_s low. Adjust L_M by transformer gap.

Design Considerations to keep in mind are:

1. Ferrite material is almost always used because of good electrical performance and available with rounded smooth surfaces compatible with many materials. Ceramic Magnetics Co., NJ, makes custom shapes.
2. Windings are usually installed on a bobbin and inserted onto core as an assembly. This method allows for better control of winding placement. Toroids are not practical. Use C-shaped ones or pot cores.
3. Wire sizes smaller than #38 are difficult to wind.
4. Generally, C_s capacitances can be minimized but will form the dominant capacitance in tank network. C_s can be minimized by:
   a. Selection of impregnation material. Potting compound raises C_s by factor of K_{ε}.
   b. Winding method:
      • Layer winding produces highest C_s. Layer spacing controls C_s.
      • Lattice, bank, and section winding techniques lower C_s.
      • Generally, techniques that lower C_s also produce reduced field stress.

C. Magnet Wire Selection

Procure to Federal Spec. JW1177A.

Insulation

1. It must be compatible with potting material:
   a. Polyester insulation generally acceptable. Low voltage use.
   b. Polyimide (ML) insulation provides greatest breakdown strength, however, extremely difficult to strip.
   c. Some wire comes with lubricant overcoat. Will result in extremely poor adhesion. Avoid this.
2. For operation at 100 kHz; dissipation factor will be a consideration. D.F. of polyurethanes is too high. Polyesters and epoxies have lower D.F.s.
3. Lattice, bank windings require friction surface over insulation. (Phelps/Dodge.) This also has high Breakdown (B.D.) strength.

Wire Termination

1. Free ends of magnet wire can serve as connection leads. Difficult to prevent small wires from breaking during handling. This technique is however used by Code 563 at GSFC.

2. Ends of magnet wire connected to terminals on assembly header. Mechanical stresses can produce wire breakage.
3. Ends of magnet wire connected to hookup wire and external connections made to hookup wire. Difficult to dress hookup wire.

D. High Voltage Winding Encapsulation of Transformers

Non-Potted

1. Kapton tape used as a barrier between layers approximately every 300 V. Breakdown field of Kapton tape is 100 V/mil.
2. Leads entering transformer should be shielded with Kapton tape on HV winding and on adjacent low voltage windings. (Pot core transformers.)

Potted

1. Porous barrier material must be used. Kapton, mylar, etc., must be avoided. Fiberglass matting, polyester matting are used. Porous material between each layer aides in wicking in the encapsulant.
2. Potting may be performed on bobbin winding assembly or on complete transformer assembly.
   a. Potting of bobbin assembly first, allows for better inspection.
   b. Potting of core material must be done with semi rigid material to avoid magnetostriction. So do not pot the core—or use polyurethane, which is semi-rigid.
   c. Complete penetration of EN-11 will occur into layer-wound winding, using #38 AWG maximum wire and applying matting between alternate layers.
   d. Lattice wound coils have shown complete impregnation without use of matting material. More investigation needs to be done.
   e. Potting makes for a more rugged construction, however, some of the properties are contradictory, such as in "b" above and yet needing the lower D.F. of epoxies; then only pot the HV winding, not the whole transformer.

E. Qualification Testing

1. MIL STD 981 requirements.
2. Vacuum life tests.
3. Corona testing.
   a. With the Biddle system, it can only be performed interwinding, using DC voltages, if transformer layout provides separation between complete high voltage winding and low voltage windings/core.
   b. With a non-standardized, high pass filter, corona test system, it can be performed in a semi-qualitative manner under the transformer's own input power. See Appendix IV, in Chapter 5.

F. Dielectric Stress Design

If a transformer has to have lower voltage outputs "floating" on an already high voltage transformer, then resin coatings containing powdered carbon can be applied to the proper surfaces of the transformer ferrite core to reduce dielectric stress. See Ref. [8]. This is analogous to corona strand shielding in HV cables.

III. HV Diodes

Glass-encased diodes should be used rather than plastic molded. The glass encasement should be bubble- or void-*free*. This is best achieved with so-called Metoxilyte glass emulsion melted down onto the diodes, *not* a glass sleeve melted down over connecting ribbon. (The latter is done by Unitrode and by Phillips.)

Table 4.3. High voltage diodes guide (IN5184, IN649, and IN4586 have also been used).

Manuf.	Type	Rating	Spec.
Semtech	HF60A	6 kV	GSFC 73-15077
Semtech	HF75	7.5 kV	
Semtech	HF40	4.0 kV	
Semtech	HF15	1.5 kV	
VMI (Voltage Multiplier Inc.)	X150UFG	15 kV	
Solid State Devices, Inc.	SHM 15 UF through 140 UF	1.5 kV through 14 kV	
Microsemi-conductor	MC002		

The reverse recovery time of the diodes should be less than 200 ns. The junction capacitance should be 1 to 2 pF because the output ripple on a HV multiplier is a function of that. Since the physical size of a 6 kV diode is not much larger than a 2.5 kV diode, one can well order the 6 kV unit and derate by more than 50% for greater reliability.

For special applications, such as in Optocoupler, diodes with higher than usual reverse leakage currents and slower ones with 1 μs reverse recovery time are desirable (these are the 15 kV units by VMI). For a while, the Hewlett Packard Company was well known for advice in the Optocoupler field, but now GSFC has used Micropac Industries, Inc. units, such as the 6N140 Optocoupler 66012; also the Optek Co. is expert in this area.

IV. High Voltage Transistors

High Voltage Transistors rarely make up, or are found in, high voltage assemblies because these assemblies can be designed by use of high voltage diodes which produce fewer problems. Nevertheless, there *are* some important uses for high voltage transistors. By definition, we call them high voltage transistors if either BV_{CBO} or BV_{CEO} are greater than 150 V. (CBO or CEO means collector-base open/collector emitter-open, respectively.)

Table 4.4. HV transistors guide.

Type	Package	$BV_{CE/BO}$	Specific Unit
NPN	T0-5	300 V	2N3501 2N5662
NPN	T0-3	>300 V	2N5097
PNP	T0-5	300 V	2N5096
Power MOSFET*	T0-5 T0-254 AA T0-257 AA	1000 V 1000 V 1000 V	 IRFMG 40 IRHY7G 30CMSE

*Metal-Oxide Semiconductor Field-Effect Transistor

The earlier power MOSFETs were sensitive to high energy radiation, that is, cosmic rays, solar proton flux, etc. One can now get radiation hardened ones, for instance, from International IR Rectifier Co. Below follow some outlines of circuit schematics where high voltage transistors are used. These circuits are in Oscillator Switching, Shunt Regulators and Commandable High Voltage Switches (Figures 4.4–4.7).

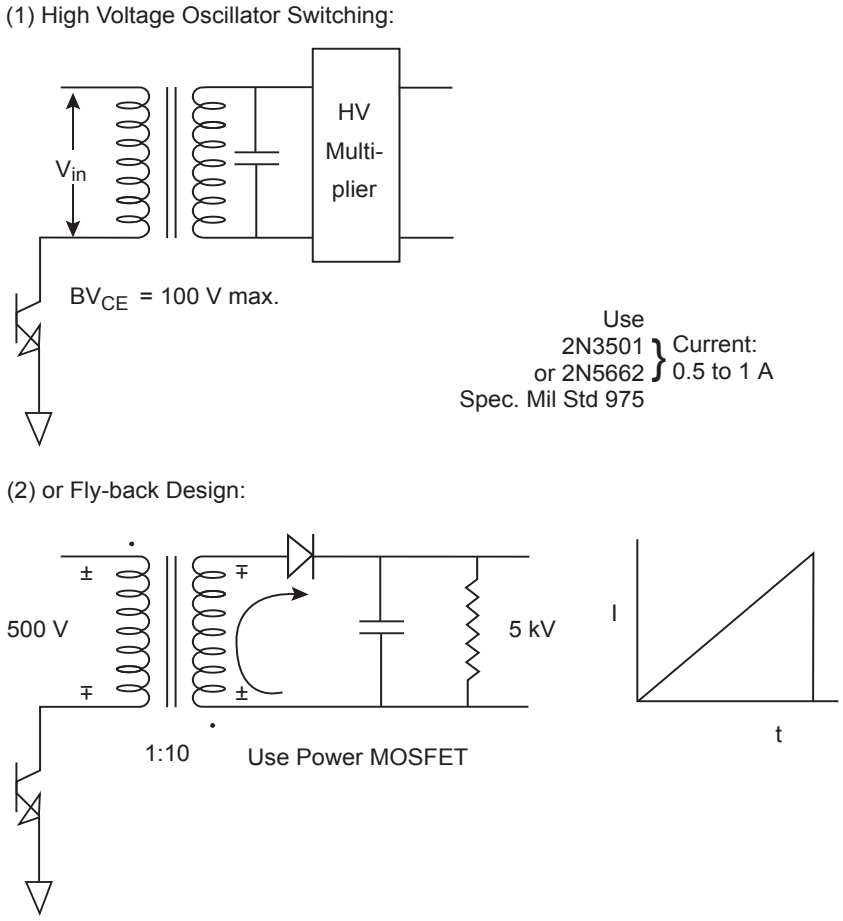
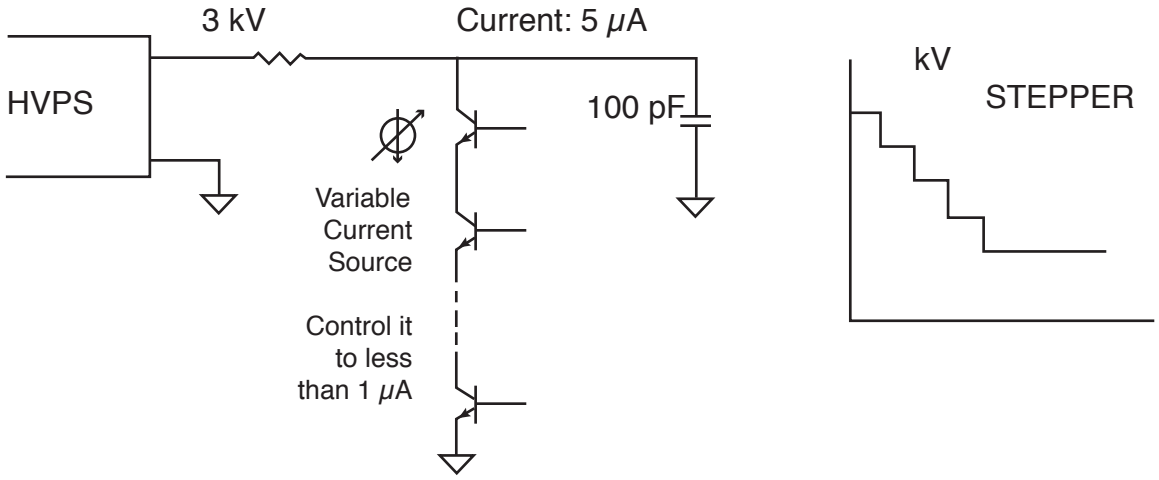


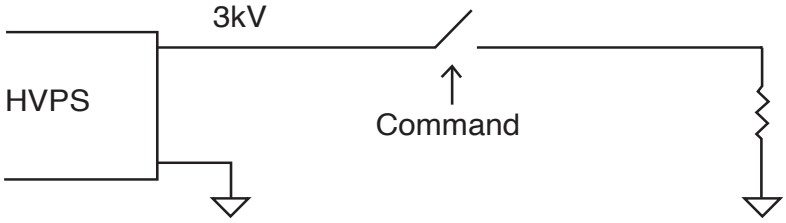
Figure 4.4. High voltage oscillator switching.



Suitable transistors: 2N5097 NPN or 2N5096 PNP

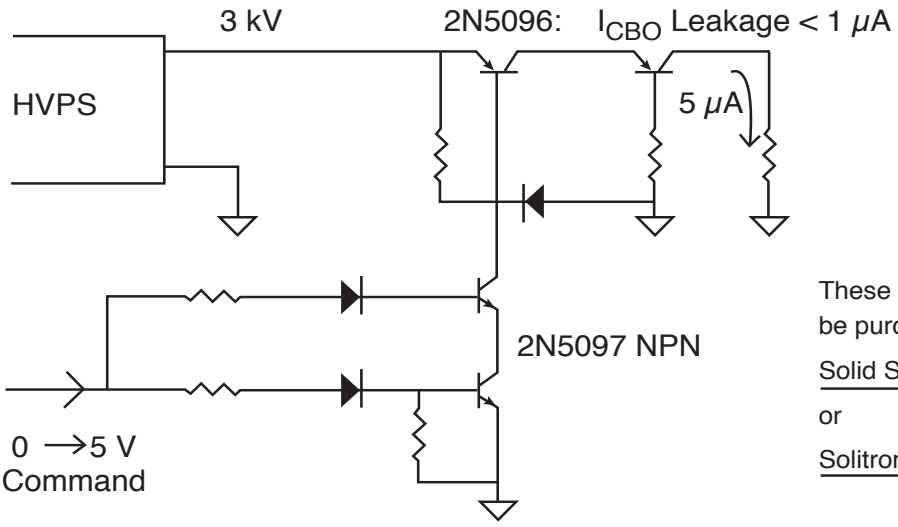
One needs to stack many transistors (10) in series here.
It is better to use optocouplers.
Power MOSFETS are not suitable here because their leakage currents are too high.

Figure 4.5. Shunt regulators.



Possibly also use Spark Gap Tubes, as was done in EGRET (GRO).

Using Transistors, this Command "Switch" is drawn in greater detail:



These transistors can be purchased from

Solid State Devices

or

Solitron

Because the current to be controlled by the switch is so low (5 μA), the leakage current must be less than 1 μA. Also, the solder pads must be rounded.

Figure 4.6. HV switch, commandable.

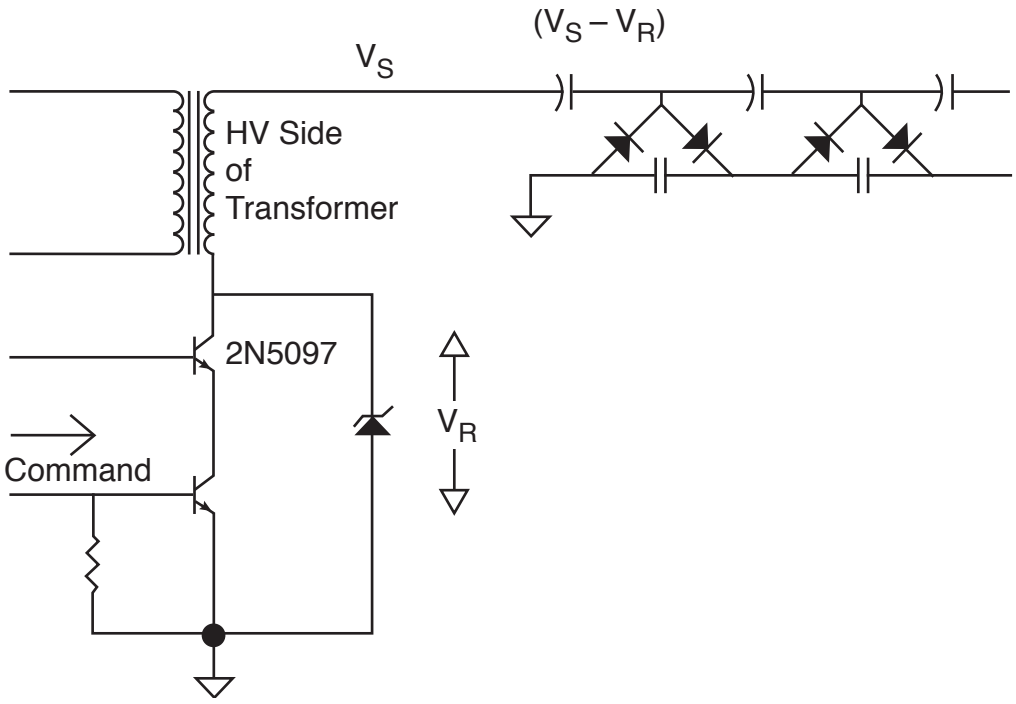


Figure 4.7. Command on HV side of transformer (K. Castell's supply).

V. High Voltage Optocouplers

Stepping high voltage applications require output voltages to typically cover a voltage range that spans four decades. Some applications call for five decades. Additionally, the voltages are swept in logarithmic fashion with durations of 3–10 ms. High slew rates and short settling times are needed to minimize the sampling dead time. At the same time, the trade-off between stepping rates and power consumption needs to be addressed.

Multi-stage bipolar transistor shunt regulators have been employed in the past to produce stepping outputs with fast "downward" voltage steps, but increasing voltage steps were controlled by long time-constant RC networks.

In the early 1980s, designers started using optocoupler techniques instead of the bipolar shunt regulators. The photoconductive characteristic of a reversed biased high voltage silicon diode served as the means to produce a light controlled, variable high voltage impedance. Illuminating the surface of transparent/translucent coated diodes are 890 nm GaAlAs infrared LEDs, which produce the necessary HV diode leakage to achieve the slew rates better than 3 kV/ms (100 pF load). Other light sources have also been successfully used.

A stepping supply block diagram is shown in Figure 4.8 using optocouplers:

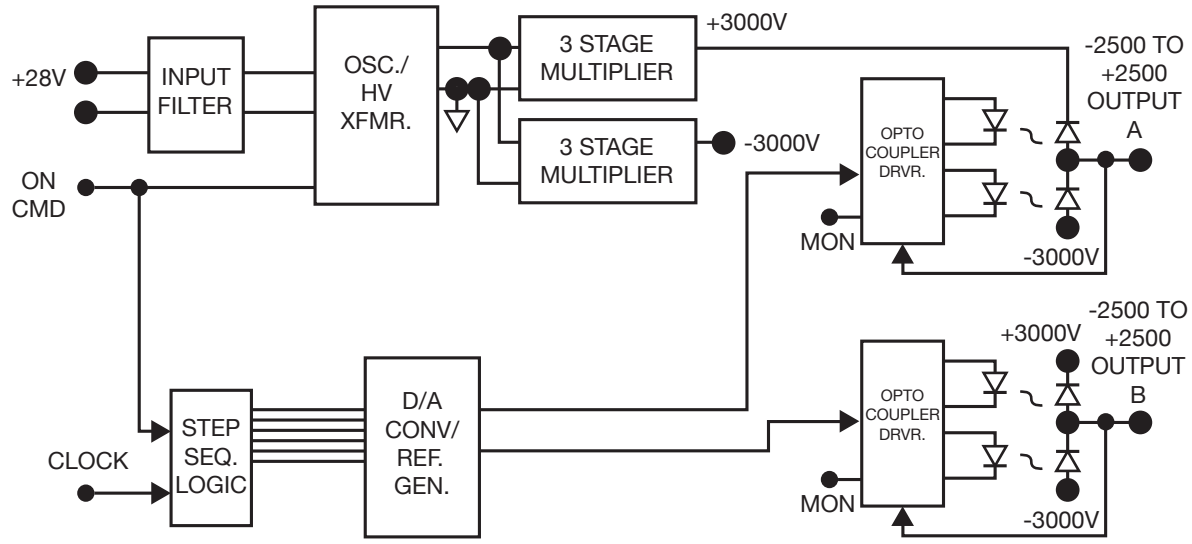


Figure 4.8. A stepper block diagram using optocouplers.

A fixed level, ± 3000 V output high voltage supply provides the inputs for the output regulators. A linear closed loop control senses the output voltage, compares it to the sweep reference, and adjusts the LED current accordingly.

The optocoupler approach yields the following advantages:
1. Fast slew rates stepping in both directions.
2. The ability to sweep from +high voltage to –high voltage from a single output.
3. Reduced size, weight, and parts count.
4. A simple linear control loop.

Supplies stepping up to 10 kV have been produced using discrete LEDs and high voltage diodes. An assembly with the proper LED to high voltage diode spacing was designed to provide the necessary dielectric breakdown strength and meet the slew rate requirements. Voltage Multiplier, Inc. manufactures diodes specifically intended for this application. AMPTEK, Inc. manufactures an optocoupler (HV601) for applications up to ±3000 V.

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8. Ruitberg, A.P., "Dielectric Stress Design," *Proc. Power Con. 9,* Power Concepts, Inc., 1982.

APPENDICES TO CHAPTER 4

Appendix I to Chapter 4

Evaluation of High Voltage Multilayer Ceramic Capacitors for Space Flight Applications, by J.F. Plante and M.J. Sampson, NASA Parts Project Office/GSFC/Unisys Corp., Lanham, MD, 1993.

The great detail shows the care applied to HV multilayer capacitor evaluation.

Appendix II to Chapter 4

Potting Procedures for the Cassini Plasma Spectrometer (CAPS) HVPS *TRANSFORMER & FILTERS,* by Suong Le, Unisys Government Systems MA-1995-169; Oct. 26, 1995.

This gives directions for a difficult potting procedure.

EVALUATION OF HIGH VOLTAGE MULTILAYER CERAMIC CAPACITORS FOR SPACE FLIGHT APPLICATIONS (~1993)

Jeannette F. Plante and Michael J. Sampson
NASA Parts Project Office/ Unisys Support Group

ABSTRACT

NASA designers frequently use high voltage ceramic disc capacitors for filtering and smoothing, in power supplies. Driven by the need for increased volumetric efficiency, NASA has evaluated high voltage multilayer ceramic capacitors (HVMLCs) for spaceflight use.

Electrical and environmental tests were performed to show part reliability with respect to the space flight environment. AC and DC partial discharge tests were included in the test plan to investigate their effectiveness as nondestructive screens for potential life test failures.

It was found that an unexpected mechanism stimulated the majority of the life test failures. A much more effective screening method can now be developed.

BACKGROUND

There is a need within NASA for high voltage capacitors that have a greater volumetric efficiency (capacitance per unit volume) than the single layer ceramic disc capacitors currently in use. High voltage multilayer ceramic (HVMLC) styles are now available that offer this size advantage. The military specification MIL-C-49467 covers this part type, however there are no qualified sources available.

The susceptibility of thin and brittle layers of dielectric to voltage breakdown is the major reliability issue when considering HVMLCs.

Also the large physical size of these devices makes them vulnerable to damage due to thermal cycling. Although encapsulated, these parts are not hermetically sealed, therefore moisture contamination is also a concern.
DC partial discharge testing has traditionally been used by NASA as a nondestructive screen for internal defects in high voltage ceramic disc capacitors. A partial discharge is an electric pulse detected within the dielectric of a capacitor related to ionization activity. This ionization occurs in regions having lower resistivity than the surrounding dielectric such as voids and other defects. When the breakdown voltage of the defect is reached a transient current flows through the fault site and the voltage drop is detected as a pulse measured in picocoulombs. The magnitudes of the discharges recorded during DC partial discharge testing are a function of the dielectric constant, the ferroelectric nature of the dielectric, and the relationship between the physical geometries of the defect and their orientations to the applied electric field.

When an AC signal is applied to these parts, internal partial discharge activity increases drastically and hot spots can develop at defect sites. Therefore the AC partial discharge test is viewed by NASA as a destructive test when applied to a part intended for DC use. However, the AC partial discharge test is much more attractive for standard use than the DC test because it is less time consuming to perform, the equipment is less costly than the DC test equipment and the data is less open to varied interpretation than that produced by the DC test. If the AC test could be shown

to be nondestructive, the test method could be standardized for incorporation into military and NASA procurement documents.

OBJECTIVES

The primary objective of the test program was to evaluate a matrix of HVMLC capacitors in order to determine if the technology exists to provide reliable parts for spaceflight use. Thermal cycling, low voltage steady state humidity testing and vacuum testing were included in the test plan to address specific space flight reliability concerns.

A second objective was to investigate the effectiveness of DC and AC Partial Discharge (PD) testing as non-destructive screens for potential life failures.

TEST PLAN

Table 1 [4.A.I.1] shows the test plan and Table 2 [4.A.I.2] lists the test methods used. Each set was submitted to exactly the same test routine.

Table 1 [4.A.I.1]. Test Plan

Screening Tests: (36 pieces/Lot)
Initial Electrical Tests
Construction Analysis
DC Partial Discharge
AC Partial Discharge
Temperature Cycling & Voltage Conditioning
DC Partial Discharge
AC Partial Discharge
Environmental Tests
100 Thermal Cycles
85°C/85% Relative Humidity, Low Voltage
DC Partial Discharge
Barometric Pressure/DC Partial Discharge
Life Test: 1000 hours
DC Partial Discharge Tested
AC Partial Discharge Tested
100 Thermal Cycles tested
Barometric Pressure Tested
Control parts

Table 2 [4.A.I.2]. Test methods for evaluation.

Test	Standard/Specification	Test Condition
Dielectric Withstanding Voltage	MIL-STD-202 - Dielectric	Ramp voltage, 120% rated voltage between the leads. Fail: current greater than or equal to 1 μA.
	- Body	Ramp to 500 V DC, applied between leads and metal tape wrapped around body.
Capacitance and Dissipation Factor	MIL-STD-202	For X7R dielectric: 1 V at 1 kHz For NPO dielectric: 1 V at 1 kHz except for C < 1000 pF then 1 MHz Fail: Cap: outside of tolerance, DF: > 2.5% for X7R and > 0.2% for NPO.
Insulation Resistance	MIL-STD-202	500 V DC applied, Fail: below limit of 100 GΩ at 25°C and 10 GΩ at 85°C, except for one set where C > 10,000 then 66 GΩ and 6.6 GΩ respectively.
Temperature Cycling	MIL-STD-202	5 cycles from –55°C to +85°C for screening, 100 cycles for environmental test.
Voltage Conditioning	MIL-C-49467	Ramp voltage, except use 120% DC rated voltage, 96 hours minimum.
DC Partial Discharge	Adapted from ASTM D 1868-81 & IEEE STD 454-1973	Stepwise ramps and plateau sequence: acquiring for 60 s, the pulse and total charge sum data from, 0 to half rated voltage, half rated voltage to full rated voltage, at the quiescent plateau and from rated voltage to 0.
AC Partial Discharge	Adapted from ASTM D 1868-81 & IEEE STD 454-1973	Ramped 60 Hz AC voltage until 100 pC pulses are detected. Dwell at corona inception voltage maximum of 5 s. No measurement above 70% of the DC rated voltage (equivalent in rms volts).
85°C/85% Relative Humidity Low Voltage	MIL-C-123A	Electrical measurements do not exceed limits above. Capacitance delta not to exceed 10%.
Barometric Pressure/ DC Partial Discharge	Adapted from MIL-STD-202	DC Partial Discharge measurements taken as noted above at atmospheric pressure in the vacuum chamber. Pressure reduced to $6(10^{-6})$ torr and held for 2 h. DC Partial Discharge measurements taken while parts are under vacuum.
Life Test		See voltage conditioning above, except use 120% DC rated voltage. DWV, capacitance, DF and IR measurements after 240 and 1000 h.

PARTS DESCRIPTION

NASA procured custom parts based on commercially available designs from three manufacturers. The external dimensions complied with EIA-IS-37. All of the parts were radial leaded.

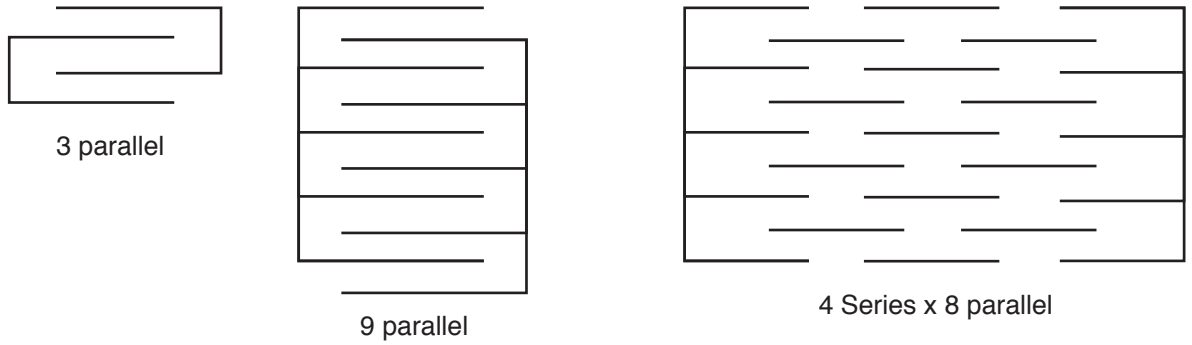
Two dielectric types were selected, NPO (low dielectric constant) and X7R (higher). Three kilovolt and five kilovolt ratings were specified. The thickness of the dielectric in the active area was restricted to 100 V/mil maximum for parts made with the X7R dielectric and 200 V/mil maximum for those made with the NPO dielectric. The manufacturers were also asked to provide a lot consisting of their 5 kV, X7R part with the highest capacitance available, in the standard EIA-IS-37 case size. No V/mil restriction was placed on this last lot.

Capacitance values were not specified (other than the rather loose requirement for the final lot) and no screening tests were required of the manufacturers. See Table 3 [4.A.I.3] for the final part matrix and some of the characteristics of the parts that were received. Manufacturer 1 (MFR1) used epoxy backfilled boxes for chip encapsulation. Manufacturer 2 (MFR 2) used urethane backfilled boxes and Manufacturer 3 (MFR 3) used a fluidized bed epoxy coating. MFR 1 supplied two lots, MFR 2 supplied three lots and MFR 3 supplied five lots.

Table 3 [4.A.I.3]. Parts matrix.

Manufacturer	Capacitance Nominal	DF Nominal	Plate Design 2/	Number of Dielectric Layers 1/	Dielectric Thickness 1/	Minimum End Margin Thickness	V/mil (Between Plates)	Chip Dimensions		
								Height	Width	Thickness
Set 2: 3 kV, X7R, < 100 V/mil, DF < 2.5%										
1	4800 pF	1.0%	3 parallel	3	30 mil	34 mil	100	435 mil	432 mil	116 mil
3	3800 pF	1.4%	4 series x 20 parallel	20	7 mil	20 mil	100	319 mil	356 mil	190 mil
Set 4: 5 kV, X7R, < 100 V/mil, DF < 2.5%										
2	6600 pF	0.8%	2 series x 8 parallel	8	23 mil	59 mil	100	740 mil	653 mil	276 mil
3	8000 pF	1.4%	4 series x 12 parallel	12	13 mil	30 mil	100	603 mil	771 mil	212 mil
Set 5: 3 kV, NPO, < 200 V/mil, DF < 0.2%										
1	400 pF	0.01%	3 parallel	3	16 mil	42 mil	200	434 mil	436 mil	101 mil
3	310 pF	>0.2%	3 series x 20 parallel	20	7 mil	19 mil	200	214 mil	309 mil	183 mil
Set 7: 5 kV, NPO, < 200 V/mil, DF < 0.2%										
2	1600 pF	>0.2%	8 parallel	8	22 mil	56 mil	200	732 mil	674 mil	218 mil
3	730 pF	0.02%	4 series x 22 parallel	22	6 mil	28 mil	200	615 mil	730 mil	181 mil
Set 9: 5 kV, X7R, No V/mil Limit, DF < 2.5%, Highest C Possible										
2	14000 pF	1.4%	2 series x 10 parallel	10	18 mil	24 mil	140	700 mil	598 mil	248 mil
3	10800 pF	1.2%	4 series x 14 parallel	14	10.5 mil	30 mil	120	600 mil	733 mil	190 mil

1/ Dielectric layers counted at thinnest points
2/ See Figures below



[Different plate designs in high voltage ceramic multilayer capacitors.]

TEST RESULTS

Material Tests

Per ASTM-E-595, "Standard Test Method for Total Mass Loss and Collected Volatile Condensable Materials From Outgassing in a Vacuum Environment," outgassing testing was performed on prepared samples of the three material combinations used for element encapsulation. Collected Volatile Condensible Materials (CVCM) data for the epoxy exceeded the limit by 0.03%. The urethane and proprietary coating passed the outgassing requirement (Total Mass Loss ≤ 1.0%, CVCM ≤ 0.1%).

Screening Tests

All of the test parts were screened using standard electrical test (See Table 2 [4.A.I.2]). Insulation resistance (IR) testing which was performed at 25°C and 85°C, using a 500 V DC bias for 2 minutes showed the only initial failures. Large numbers of MFR 3's parts (three out of five lots) showed IR failures at 85°C. The problem was traced to moisture absorbed by the coating. Passing IR values (>100 GΩ) were measured after these parts were baked for 12 hours at 125°C. DC and AC partial discharge testing was performed on two subgroups of each lot (10 pieces each) following initial electrical characterization. Results of the partial discharge testing will be discussed later.

Table 4 [4.A.I.4]. Summary of screening failures.

36 pieces tested in each lot Lot and Manufacturer	Incoming Failures		Post Voltage Conditioning Failures		Capacitance Change From Incoming Nominal (%)	Dissipation Factor Change From Incoming Nominal (%)
	No.	Type	No.	Type		
Lot A: X7R, 3 kV, <100 V/mil						
1	1	Cap	7	DWV	0%	0%
3	0	—	35 1/	CAP	-11%	-0.04%
Lot B: X7R, 5 kV, <100 V/mil						
2	0	—	1	DWV	-4.6%	0%
3	43	IR 85C	1 36 1/	DWV CAP	-7.6%	-0.02%
Lot C: NPO, 3 kV, <200 V/mil						
1	1	Cap & DF	2	Cap & DWV	0%	0%
3	37	IR 85C	0	—	0%	-0.01%
Lot D: NPO, 5 kV, <200 V/mil						
2	2	Cap	2	DWV	-6%	0%
3	8	IR 85C	2	DWV	0%	-0.02%
Lot E: X7R, 5 kV, No <100 V/mil limit						
2	0	—	0	—	-3.7%	0%
3	0	—	0	—	-9%	0%

1/ Measured below 10% capacitance tolerance

All of the parts (36 pieces) were submitted to the following testing sequence: five thermal cycles (–55°C to 85°C), DWV tests (dielectric and body test), voltage conditioning (120% DC rated voltage at 85°C, for 100 hours), DWV (dielectric and body), Capacitance, DF, IR at high and low temperature, and DC partial discharge.

Subgroup II was AC partial discharge tested a second time instead of DC partial discharge tested at this point. See Table 4 [4.A.I.4] for a summary of the screening failures.

Construction Analysis

Two capacitors from each lot underwent construction analysis. All of the samples were visually examined externally and then cross-sectioned at 25%, 50% and 75% into the capacitor from the top down toward the two leads.

Table 5 [4.A.I.5] shows the results of this examination. The definition of a rejectable defect is in accordance with the destructive physical analysis listed in EIA-469-B. See Table 3 [4.A.I.3] for chip dimensions and plate arrangement information.

Table 5 [4.A.I.5]. Summary of internal defects.

Lot and MFR	Rejectable Defect 1/
Lot A: 1 3	X7R, 3 kV, <100 V/mil Crack None
Lot B: 2 3	X7R, 5 kV, <100 V/mil Delamination None
Lot C: 1 3	NPO, 3 kV, <200 V/mil None Delamination
Lot D: 2 3	NPO, 5 kV, <200 V/mil None Delamination
Lot E: 2 4	X7R, 5 kV, No V/mil Limit Crack None

The crack seen in one of MFR 1's parts was probably due to thermal shock during the lead attach process. The same mechanism appeared to have produced nonrejectable cracks in the cover plate, outside of the active area. These nonrejectable cracks were found in both lots received from MFR 1. MFR 2's parts showed delaminations probably induced during ink binder burn out. In one sample, a large crack at the end termination was evidence of severe thermal shock during that burn out stage. MFR 3's parts showed cracks in the cover plate due to the encapsulation process. Several parts showed severe delaminations. Lamination lines were obvious as well.

Environmental Tests

Subgroups were subjected to either one hundred thermal cycles (–55°C to 85°C) or the 85/85 test (85°C, 85% relative humidity, 1.3 V DC bias, 240 hours). DWV, Capacitance, DF, IR at high and low temperature and DC partial discharge measurements were made after the temperature cycles. The same applied after the 85/85 test with the exception of DWV testing. Table 6 [4.A.I.6] lists the failures found after thermal cycling. Cracks could be seen in the coating on several of MFR 3's larger parts (lots B, D and E) after thermal cycling even though they did not show electrical failure. All of MFR 1's and MFR 3's lots showed failing IR measurements immediately after the 85/85 test (within 24 hours). MFR 2's lot E parts only (X7R, 5 kV, 140 V/mil), showed this type of failure. All of these failing measurements recovered after oven baking for 12 hours (85°C).

Table 6 [4.A.I.6]. Summary of Thermal Cycling failure (100 cycles).

	Failures (10 pieces tested)	
Lot & Mfr.	No.	Type
Lot C: 3	NPO, 2	5 kV, 200 V/mil DF& IR at 85ºC
Lot E: 2	X7R, 5	5 kV, No V/mil limit C

The balance of MFR 2's pieces (lot B and lot D) did not show any electrical failure after the 85/85 test.

A final subgroup consisted of parts that had seen one hundred thermal cycles, parts that had seen 85/85 testing and one part that had only seen screening tests. DC partial discharge measurements were taken on these parts after two hours in vacuum (6×10^{-6} torr) in an attempt to identify voids in the potting that could have been bridging the end terminations. No significant increase in partial discharges was detected compared to measurements taken at atmospheric pressure.

Life Tests

Life testing was performed with all of the parts completely submerged in Fluorinert dielectric fluid for 1000 hours. The parts were biased with 120% of the DC rated voltage and the temperature was maintained at 85°C. The start up procedure was as follows: Submerge fixture (5 boards, 36 pieces in parallel per board) into Fluorinert bath (room temperature). Slowly (25 seconds) raise voltage on power supply to 120% DC rated voltage. Confirm voltage at several locations on the board. Set bath temperature to 85°C. Temperature rise time from room temperature to 85°C was approximately 1.5 hours.

The dielectric fluid was constantly circulated in the bath for an even temperature distribution. This start up procedure provided protection against uneven temperature exposure or system induced thermal shock. Currents in excess of 3 mA automatically shut down the power supply. IR at high and low temperature, DWV, Capacitance and DF measurements were made following 240 and 1000 hours of life testing.

Table 7 [4.A.I.7]. Summary of life failures.

Lot and Manufacturer	Internal Plate Design	No. of Failures	Hour of Failure	Type 1/	Failure Analysis Summary
Lot A: X7R, 3 kV,<100 V/mil					
1	3 Parallel	0	—	—	—
3	4 Series x 21 Parallel	0	—	—	—
Lot B: X7R, 5 kV,<100 V/mil					
2	3 Series x 9 Parallel	0	—	—	—
3	4 Series x 13 Parallel	1	262	Restart	Crack through 3 layers and the cover plate
Lot C: NPO, 3 kV, <200 V/mil					
1	3 Parallel	3	0	Restart	All three of these failures showed a crack through cover plate and breakdown from the first metal plate to the end termination
			0	Restart	
			301	Restart	
3	3 Series x 21 Parallel	0	—	—	
Lot D: NPO, 5 kV, <200 V/mil					
2	9 Parallel	1	643	Restart	No defect found
3	4 Series x23 Parallel	1	623	Restart	Cracks perpendicular to and bridging metal plates, delaminations
Lot E: X7R, 5 kV, No V/mil limit					
2	3 Series x 11 Parallel	4	364	Restart	Crack in ceramic parallel to and next to the end termination
			671	Restart	Crack in the ceramic parallel to and next to the end termination
			215	During Test	Crack at the top margin through to the metal plates
			416	During Test	Crack through cover plate through to first metal plate
3	4 Series x 15 Parallel	1	376	Restart	Cracks perpendicular to and bridging metal plates, delaminations

1/Restart: Failure during a restart of the burn in system, temperature > 60C, 120% DC rated voltage applied.
During Test: Failure well after burn in stabilization period (at 85°C with voltage applied).

Deltas (capacitance and DF) were calculated using electrical data taken just before the life test, and data taken following 240 hours of life testing for subgroups III, IV and V and data taken following 1000 hours of life testing for subgroups I and II. All of the deltas calculated showed values of less than 2%.

A matrix showing life test failures and associated lot characteristics is given in Table 7 [4.A.I.7]. These failures were breakdowns that caused the power supply to shut down. While compiling Table 7 [4.A.I.7], it was noticed that nine out of eleven of the failures occurred during a restart of the system. These “start up” failures were found in all lots

that had a life failure. Failure analyses showed failure sites that corresponded to defect areas found during construction analysis (Table 5 [4.A.I.5]).

Table 8 [4.A.I.8]. Summary of partial discharge results.

AC Partial Discharge Rating 1/	DC Partial Discharge Rating 1/	Defects Found During Construction Analysis	Life Failures No.	Lot Description		
A	A	None	3	Lot C, NPO, 3 kV, 200 V/mil	MFR1, 400 pF	3 Parallel
B	B	None	0	Lot A, X7R, 3 kV, 100 V/ mil	MFR 3, 3800 pF	4 Series x 20 Parallel
C	D	None	1	Lot E, X7R, 5 kV, no V/mil restriction	MFR 3, 10,800 pF	4 Series x 14 Parallel
D	C	None	1	Lot D, NPO, 5 kV, 200 V/mil	MFR 2, 1600 pF	8 Parallel
E	V	Crack	0	Lot A, X7R, 3 kV, 100 V/mil	MFR 1, 4800 pF	3 Parallel
V	E	None	1	Lot B, X7R, 5 kV, 100 V/mil	MFR 3, 8000 pF	4 Series x 12 Parallel
W	X	Delamination	1	Lot D, NPO, 5 kV, 200 V/mil	MFR 3, 730 pF	4 Series x 22 Parallel
X	W	Delamination	0	Lot C, NPO, 3 kV, 200 V/mil	MFR 3, 310 pF	3 Series x 20 Parallel
Y	Y	Delamination	0	Lot B, X7R, 5 kV, 100 V/mil	MFR 2, 6600 pF	2 Series x 8 Parallel
Z	Z	Crack	4	Lot E, X7R, 5 kV, no V/milrestriction	MFR 2, 14,000 pF	2 Series x 10 Parallel

1/ A B C D E V W X Y Z
Best→→Moderate→→Worst

Table 9 [4.A.I.9]. Exerpts from partial discharge data [both DC and AC].

DC PARTIAL DISCHARGE													AC PARTIAL DISCHARGE					
RATING: A													RATING: A			RATING: Z		
Serial Number	0 to V/2			V/2 to V			Hold at V			V to 0			Serial Number	CIV for 100 pC	CIV as % of DC rated V	Serial Number	CIV for 100 pC	CIV as % of DC rated V
	# of pulses	max pulse	sum of pulses	# of pulses	max pulse	sum of pulses	# of pulses	max pulse	sum of pulses	# of pulses	max pulse	sum of pulses						
1569	0	0	0	0	0	0	0	0	0	0	0	0	1590	>1.5	>71.4	2990	0.7	20.0
1570	0	0	0	0	0	0	0	0	0	0	0	0	1591	>1.5	>71.4	2991	0.6	17.1
1571	0	0	0	0	0	0	0	0	0	0	0	0	1592	>1.5	>71.4	2992	0.6	17.1
1572	0	0	0	1	19	19	0	0	0	4	85	103	1593	>1.5	>71.4	2993	0.2	5.71
1573	0	0	0	0	0	0	0	0	0	0	0	0	1595	>1.5	>71.4	2994	0.6	17.1
RATING: Z													1596	>1.5	>71.4	2995	0.6	17.1
													1597	>1.5	>71.4	2996	0.6	17.1
2969	290	1008	39779	517	2750	157198	7	276	943	622	944	53156	1598	>1.5	>71.4	2997	0.4	11.4
2970	221	462	15839	427	2510	112911	15	386	956	296	737	31760	1599	>1.5	>71.4	2998	0.6	17.1
2971	196	1012	27862	268	1506	81891	11	281	877	729	1013	67688				2999	0.6	17.1
2972	233	980	35634	358	2058	123353	8	191	481	497	992	69760						
2973	170	978	28287	229	2108	70727	2	54	94	556	442	27750						

PARTIAL DISCHARGE DATA

DC:

The DC Partial Discharge test method consisted of measuring charge pulses in *picocoulombs* while: ramping the voltage to half rated voltage, then to full rated voltage, resting at full rated (quiescent) voltage and then ramping to zero volts. After each of these four measurement segments, analytical software then calculated the following data: the total number of pulses detected, the value of the largest pulse detected, and the total charge detected. These three data points taken at each of the four measurement segments periods formed the DC partial discharge signature.

As discussed earlier, the typical DC partial discharge signature for a part type is dependant on material characteristics and internal electrical design. Therefore, only that data originating from lots that have like design and process characteristics can be compared. DC partial discharge data is typically used in two ways to screen parts: to reject

individual parts that have discharge sums that are magnitudes larger than the other parts in the lot or, to reject whole lots which have large partial discharges occurring throughout the four measurement segments.

AC:

The AC partial discharge test consists of the application of a 60 Hz sinusoidal signal, ramped up in voltage until the Corona Inception Voltage (CIV) for a 100 pC pulse is reached. The 100 pC value is a convenient test standard frequently used by the electrical insulation industry. A maximum voltage limit of 70% of the rated rms voltage was imposed to limit unnecessary damage to the part while allowing sufficient measurement range. The highest test voltage was also maintained for a maximum of 5 seconds to limit [develop damaging] potential damage. AC partial discharge data is typically used as a screening test to accept parts that do not [have] corona within the operating voltage range. Typically, NASA imposes a 60% derating factor.

Twenty pieces from each lot were screened, partial discharge tested and life tested to show any damage due to AC or DC partial discharge testing (10 pieces were DC tested only and 10 pieces were AC tested only).

All ten lots were rated based on the DC and AC partial discharge data. Table 8 [4.A.I.8] shows examples of the best (rated A) and the worst (rated Z) DC partial discharge signatures and AC partial discharge data. Table 8 [4.A.I.8] shows the results of this rating exercise. [Also Table 9 [4.A.I.9] shows partial discharge data, both AC and DC.]

Deltas calculated between incoming electrical data and electrical data taken after life test, show no parametric degradation even after the two exposures to AC partial discharge testing. Only one of the parts that had AC partial discharge testing failed on life test. This failure mechanism was not associated with AC voltage induced stress.

CONCLUSIONS

HVMLC capacitors continued to show stable electrical parameters during the application of a wide range of dc voltages and environmental stresses. The electrical and life test data, to date, do not show that the 100 V/mil field stress limit provides improved reliability versus the manufacturer's chosen design (120 and 140 V/mil). The life test failures reflected process control related defects and did not reflect a relationship to the V/mil characteristic.

Process related defects dominated the construction analysis findings. Comparison of the construction analyses and failure analyses showed that the defects were common by manufacturer. Defects found in one manufacture's parts during construction analysis were identical to defects found in a different set of his parts during failure analysis. It is believed that the technology is available to produce HVMLC capacitors, if the manufacturing processes are well controlled. This evaluation showed that none of the manufacturers involved appeared to have had adequate control over their processes.

Considering their size and the sensitivity of ceramics to thermal shock, the parts performed well after 100 thermal cycles from –55°C to 85°C. The majority of the thermal shock failures found were attributed to pre-existing cracks in the ceramic.

The urethane potting material was effective in protecting the capacitor from moisture penetration. The epoxy fluidized bed coating did not provide sufficient protection from moisture or thermal stress.

The barometric pressure test was not conclusive. A vacuum potting combined with a post encapsulation DPA will provide a more efficient and practical defect detection tool.

The failures revealed during the life test correlate well with the construction analysis findings. The majority of these failures occurred during the power up period while the temperature was increasing ("start up" failure). This indicates

that a steady state life test is not the best way to detect flawed lots. A better test would involve temperature cycling possibly combined with voltage switching. The most effective test method remains to be developed. It can be anticipated that this test method would form the basis for an effective screen (burn in) as well as an appropriate life test.

Although partial discharge testing effectively identifies flawed lots, it is unable to identify some kinds of critical defects and does not identify lot quality more effectively than sample DPA. Thus, even though it has been shown that AC partial discharge is nondestructive, it is not recommended that it be used as a specification requirement. However, the AC partial discharge test could be used as a customer imposed screen when selecting parts for use in critical applications.

RECOMMENDATION

It will be recommended that the military specification MIL-C-49467 be upgraded to a Class S specification which contains the following key features: 100 thermal cycles from –55°C to 85°C; Vacuum potting of the capacitors and material outgassing limits; Sample DPAs before termination and after encapsulation; An improved screening and life test (method to be developed).

It is further recommended that the AC partial discharge requirement be removed from the specification.

[AUTHORS' NOTE to Appendix I, Chapter 4: The authors of this HV Guide disagree with this recommendation that the AC partial discharge requirement be removed from the specification.]

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Appendix II of Chapter 4

POTTING PROCEDURES FOR THE CASSINI PLASMA SPECTROMETER (CAPS) HVPS TRANSFORMERS AND FILTERS

BY SUONG LE/ UNISYS GOVERNMENT SYSTEMS

MA-1995-169
OCTOBER 26, 1995

INTRODUCTION

In support of Code 313, Unisys personnel generated the potting procedures for the CAPS 16 kV high voltage power supply (HVPS) transformers and filters. The following procedures should be added to the respective transformer and filter specifications. The following is a log of the processing steps used by Mr. Clatterbuck of Code 313 to process the protoflight and engineering model components. They are recommended for the flight unit. It should be noted that ESD precaution is not a requirement for these procedures.

CAPS TRANSFORMERS

This procedure shall be performed in the Class 10,000 clean room. The Flight Assurance Manager or Quality Control engineer shall be notified at least twenty-four (24) hours prior to the start of this procedure.

Equipment and Materials:

- Transformer with soldered lead wires and wire-wound core on the Ultem housing from Code 734.3
- Stycast 3050 adhesive with catalyst 11 from Emerson & Cuming
- DC 6-1104 adhesive from Dow Corning
- HM-430 tape from CHR
- 200-proof ethanol from GSA or equivalent
- Reagent-grade heptane from Fisher Scientific or equivalent
- Aluminum foil cup from Fisher Scientific or equivalent
- Ultrasonic cleaner Model No. 8891 DTH from Cole Parmer or equivalent
- Binks No. 15 spray gun from Binks
- Brass cork borer No. 8 from local sources
- Stainless steel spatula from local sources
- Aclar 22C bags from Clean Room Products
- Dry nitrogen gas from local sources
- Vacuum oven with pressure of less than 200 millitorr from Code 313
- Vacuum oven with pressure of less than 400 millitorr from Code 313
- Exhaust fume hood from Code 313
- Soxhlet-extracted swabs from Code 313
- Latex gloves CR-100 from Baxter
- Polyethylene gloves from Fisher Scientific

Cleaning of Hardware

All supporting hardware and materials to be used in this potting procedure shall be cleaned with a 1 to 1 part by volume of 200-proof ethanol to reagent-grade heptane, then, baked in a convection oven for thirty (30) minutes minimum at 60°C to 65°C.

NOTE: Clean polyethylene or latex gloves shall be worn at all times during processing of the transformer. Only polyethylene gloves are acceptable for processing with a solvent.

The unpotted transformer shall be cleaned as follows:

1. Soak the transformer in a 1 to 1 part by volume mix ratio of 200-proof ethanol to heptane [ethanol/heptane solvent] for thirty (30) minutes.
2. Clean the transformer in an ultrasonic cleaner for fifteen (15) minutes at room temperature. The cleaning solvent shall be the ethanol/heptane solvent.
3. Spray clean for two to three minutes in the ethanol/heptane solvent using the Binks no. 15 spray gun at approximately 40 psi with clean, dry nitrogen gas.
4. Blow dry the transformer surfaces with clean, dry nitrogen gas.
5. Bake the transformer between 60°C to 65°C for one (1) hour minimum in vacuum at 300 militorr to 400 militorr.

Masking of the Transformer

Masking shall be performed immediately after the cleaning and drying process. The procedure is as follows:

1. Seal electrical feedthrus, around electrical lead wires, with the DC6-1104 silicone adhesive. The silicone shall be applied only to external surfaces as shown in Figure 1 [4.A.II.1].
2. Air dry the adhesive for one (1) hour minimum at room temperature.
3. Mask the top and bottom of the wire-wound center-core with the Teflon HM-430 tape (Figure 1 [4.A.II.1]). Use the no. 8 brass cork borer to cut the sealing tape for the through holes.
4. Mask the Ultem transformer housing around the periphery with a 1-inch wide HM-430 tape starting at approximately 1/8" from the top of the housing (Figure 2 [4.A.II.2]). Masking is to prevent encapsulant spillage during degassing.

Potting of the Transformer

Potting shall be performed at least one hour after the application of the DC6-1104 adhesive and immediately after the masking process. The procedure is as follows:

1. Stir the Stycast 3050 epoxy resin with a stainless steel spatula for four to five minutes or until the resin is well mixed.
2. Weight out the resin from step 1, then, add in catalyst 11 with an eye dropper. The mix ratio is 100 to 8 parts by weight of resin to catalyst. The pot life for the Stycast 3050/catalyst 11 adhesive is approximately four (4) hours.
3. Mix resin and catalyst under the hood for approximately five minutes.
4. Degas the mixed contents for thirty (30) minutes in approximately 200 millitorr vacuum or less. The deaerated adhesive is referred to as "encapsulant" hereafter.

   NOTE: Resin stirring, mixing, and degassing (Steps 1 through 4) shall be performed under an exhaust fume hood prior to bringing it into the clean room.
5 . Cast a witness sample of approximately 1 inch in diameter and ½ inch in thickness.

6. Pour the encapsulant slowly into the housing until approximately half full.
7. Degas the encapsulant in the transformer for thirty minutes in approximately 200 millitorr vacuum or less.
8. Remove the transformer from vacuum, then, fill the housing almost full with the encapsulant.
9. Degas the housing from step 8 for thirty (30) minutes in approximately 200 millitorr vacuum or less.
10. Fill the housing with the encapsulant up to the top of the transformer housing.
11. Degas for forty-five (45) minutes in approximately 200 millitorr vacuum or less for complete impregnation of the resin into the coil and core.
12. Bake the potted transformer and the witness sample of Step 5 in a convection oven at between 83°C to 85°C for thirty-six (36) hours minimum.
13. Remove the potted transformer from the oven and let it cool to room temperature.
14. Remove the masking tape, DC6-1104 adhesive and clean any adhesive residue from external surfaces of the casing and wire insulation using a Soxhlet-extracted swab dampened with ethanol.
15. Verify and record the hardness of the witness sample.
16. Place the transformer in a clean Aclar 22C bag for storage or transport.

CAPS FILTERS

This procedure shall be performed in the Class 10,000 clean room. The Flight Assurance Manager or Quality Control engineer shall be notified at least twenty-four (24) hours prior to the start of this procedure.

Equipment and Materials

- Filter with soldered lead wires and EEE components on the Ultem housing from Code 734.3
- EN-11 part B and EN-4 part A from Conap
- PR-420A/B primer from Product Research
- DC 6-1104 adhesive from Dow Corning
- HM-430 tape from CHR
- 200-proof ethanol from GSA or equivalent
- Reagent-grade heptane from Fisher Scientific or equivalent
- Aluminum foil cup from Fisher Scientific or equivalent
- Ultrasonic cleaner Model No. 8891 DTH from Cole Parmer or equivalent
- Binks No. 15 spray gun from Binks
- Brass cork borer No. 8 from local sources
- Stainless steel spatula from local sources
- Aclar 22C bags from Clean Room Products
- Dry nitrogen gas from local sources
- Vacuum oven with pressure of less than 200 millitorr from Code 313
- Vacuum oven with pressure of less than 400 millitorr from Code 313
- Exhaust fume hood from Code 313
- Soxhlet-extracted swabs from Code 313
- Latex gloves CR-100 from Baxter
- Polyethylene gloves from Fisher Scientific

Cleaning of Hardware

All supporting hardware and materials to be used in this potting procedure shall be cleaned with a 1 to 1 part by volume of 200-proof ethanol to reagent-grade heptane, then, baked in a convection oven for thirty (30) minutes minimum at 60°C to 65°C.

NOTE: Clean polyethylene or latex gloves shall be worn at all times during processing of the transformer. Only polyethylene gloves are acceptable for processing with a solvent.

The unpotted filter shall be cleaned as follows:

1. Soak the filter in a 1 to 1 part by volume mix ratio of 200-proof ethanol to heptane [ethanol/heptane solvent] for thirty (30) minutes.
2. Clean the filter in an ultrasonic cleaner for fifteen (15) minutes at room temperature (RT). The cleaning solvent shall be the ethanol/heptane solvent.
3. Spray clean for two to three minutes in the ethanol/heptane solvent using the Binks no. 15 spray gun at approximately 30 psi with clean, dry nitrogen gas.
4. Blow dry the filter surfaces with clean, dry nitrogen gas.
5. Bake the filter between 60°C to 65°C for one (1) hour minimum in vacuum at 300 millitorr to 400 millitorr.

Sealing and Masking of the Filter

Masking shall be performed immediately after the cleaning process. The procedure is as follows:

1. Seal the areas where the screws are in contact with the external surfaces of the filter housing with the DC6-1104 silicone adhesive (Figure 1 [4.A.II.1]). Use a syringe for the adhesive application.
2. Air dry the adhesive for one (1) hour minimum at RT.
3. Mask all holes of the filter housing (Figure 1 [4.A.II.1]) with a half-inch wide HM-430 Teflon tape.

Priming of the Filter

Primer PR-420A/B can be applied immediately after the DC6-1104 silicone sealing.

1. Stir part A and B well before weighing. The mix ratio shall be 13.7/100 A/B pbw.
2. Let mixed primer stand for fifteen (15) minutes at room temperature before priming all surfaces of the resistors and capacitor.

Masking of the Filter for Potting

1. Mask the Ultem filter housing completely around the periphery with a half-inch wide HM-430 tape starting at approximately 1/8” from the top of the housing (Figure 1 [4.A.II.1]). Masking is to prevent encapsulant spillage during degassing.
2 Reinforce the overlapped area of with the tape. Use a tweezer to force the tape layers in place.

Potting of the Filter

Potting shall be performed at least one hour after the application of the DC6-1104 adhesive and immediately after the masking process. The procedure is as follows:

l. Stir Conathane EN-11B well for five minutes minimum.
2. Weigh out the resin Conathane EN-4A and curing agent EN-11B in the ratio of 100 to 55 parts by weight of

EN-4A to EN-11B. The pot life for the EN-4A/EN-11B adhesive is eighty (80) minutes maximum at room temperature.

3. Mix the content under the hood for approximately five minutes.
4. Degas the mixed contents for five (5) minutes in approximately 200 to 600 militorr vacuum. The de-aerated adhesive is referred to as "encapsulant" hereafter.

NOTE: Resin stirring, mixing, and degassing (Steps 1 through 4) shall be performed under an exhaust fume hood *prior to* bringing it into the clean room.

5. Cast a witness sample of approximately 1 inch in diameter and 1/2 inch in thickness.
6. Fill the housing with the encapsulant until half full.
7. Degas the adhesive from step 6 for thirty (30) minutes in approximately 200 to 600 millitorr vacuum.
8. Remove the filter from vacuum, then, fill the housing almost full with the encapsulant (1/8" from the top of the housing).
9. Degas the housing from step 8 for thirty (30) minutes in approximately 200 to 600 millitorr vacuum.
10. Remove the filter from vacuum, then, fill the housing with the encapsulant up to the top of the housing casing.
11. Let the encapsulant and witness sample in Step 5 gel for 24 hours minimum at room temperature.
12. Bake the potted filter in a convection oven and witness sample at 65°C ±5°C for forty-eight (48) hours minimum.
13. Remove the potted filter from the oven and let it cool to room temperature.
14. Remove the masking tape, DC6-1104 adhesive and clean any potting adhesive residue from the external surfaces of the casing and wire insulation using a Soxhlet-extracted swab dampened with the ethanol/heptane solvent.
15. Verify and record the hardness of the witness sample.
16. Place the potted filter in a clean Aclar 22C bag for storage or transport.

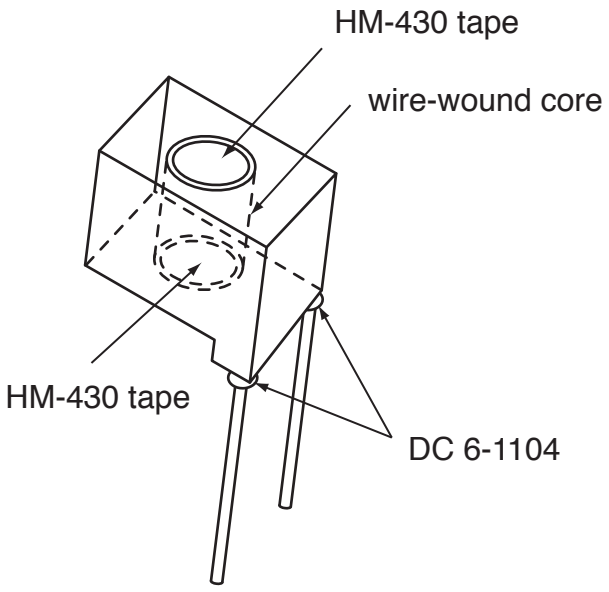

Figure 4.A.II.1. Masking of seating.

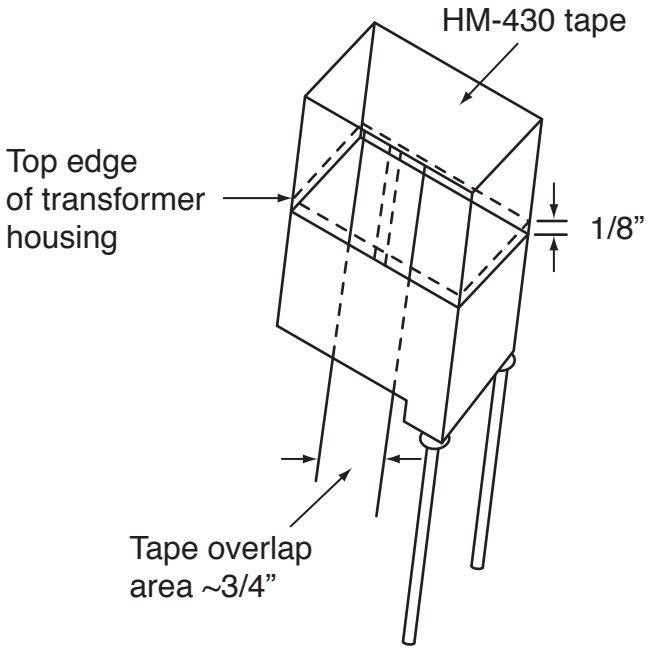

Figure 4.A.II.2. Masking of housing.

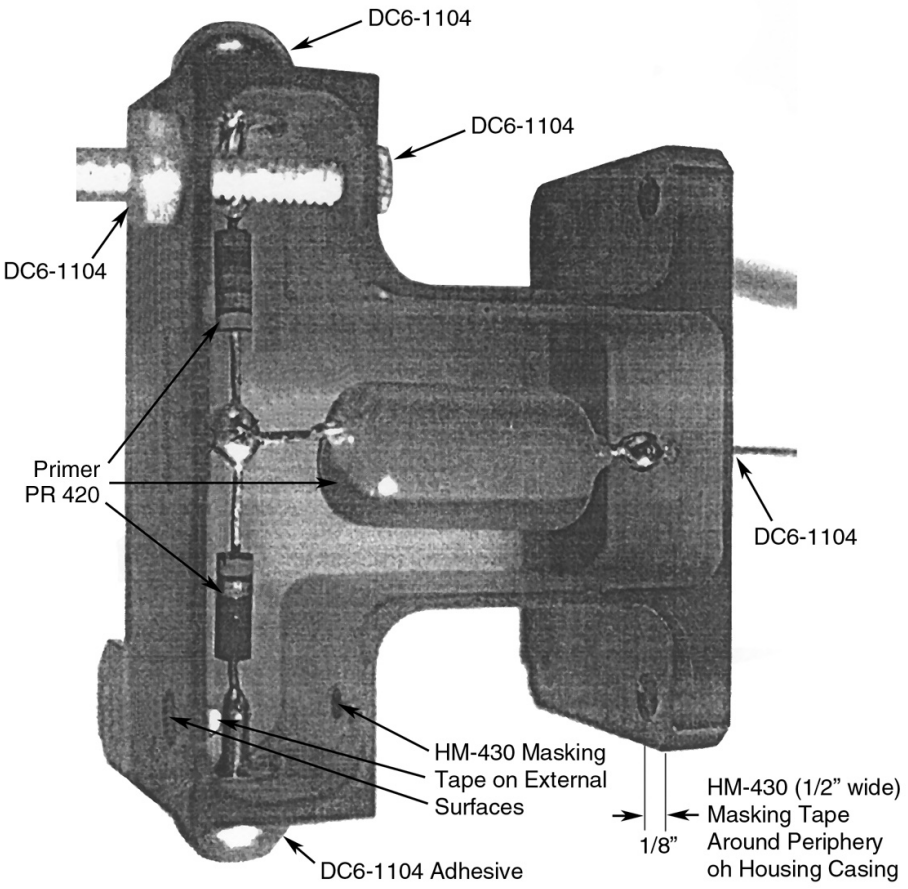

Figure 4.A.II.3. Filter masking and sealing.

Chapter 5. Partial Discharge or Corona Measurement

Introduction

Partial discharge or corona measurements are a well recognized method, under AC impressed voltage, for detecting the presence of gaseous voids, cracks, delaminations, etc., in electrical insulation. The partial discharges or corona are small electrical transients through the gaseous spaces, superposed on the main output voltage or current—the detection of the gaseous voids is thus *indirect*. Therefore, one must understand the physics of the origin of the partial discharges and why it is different for AC than for DC impressed voltage. Interpretation is not easy or obvious (Refs. [1] and [7]).

I. Theory

The equivalent circuit of a void in a dielectric is different for AC than for DC (Figures 5.l and 5.2).

A. Partial Discharge under AC Applied Voltage

Obviously, 1 kV rms "steady" 60 Hz AC Voltage is *not* steady. It is up-ramps, down-ramps, voltage reversals, down-ramps to –1.4 kV peak, etc. Again, the equivalent circuit of a void in a dielectric under AC applied voltage is essentially two capacitors in series as in Fig. 5.1. The recurrence of internal discharges at the corona inception voltage (CIV) as a function of applied AC voltage V_a is shown in Fig. 5.3. The voltage across the cavity, V_c, rises with V_a until it reaches the breakdown voltage across the cavity, and then a flow of free charges occurs through the cavity, making the voltage across it almost zero. As the outside applied voltage goes down, then by instantaneous capacitative coupling, the V_c across the cavity reduces below zero to a negative breakdown voltage across the gas, and another current transient occurs and the cavity voltage again reduces to zero. As the outside applied voltage goes through the negative half-cycle of AC, there will be two more discharges in the void, as seen in Fig.5.3, for a total of 4 per 1 AC applied cycle, already at the corona inception voltage; see Refs. [1] and [7].

Summary for AC Partial Discharge

- At corona inception voltage (CIV), already there are *theoretically 4* discharges/cycle/l void
  AC: $f_{PD} = 4f$ power at CIV
  This means 14,400 PDs/60 s at *f* power = 60 Hz
  (f_{PD}= frequency of the partial discharges; *f* power = power frequency)
- Because there are so *many* discharges on AC, the total effect over time is *harmful*. Treeing. Catastrophic arc through the Tree.
- Do not stay at CIV long. *Your* choice whether CIV at 10, 50, or 100 pC (pC = picocoulomb)
- Do not test above CIV. *Your* choice whether CIV at 10, 50, or 100 pC.
- Do not use above CIV. *Your* choice whether CIV at 10, 50, or 100 pC.
- Measure and record CIV. The "trade" uses 100 pC inception.
- The voltage across the cavity depends on the dielectric constant of the insulation in which it is buried. See Fig. 5.4. Therefore, for a given applied voltage, PDs begin at a lower applied voltage the higher the dielectric constant of the test sample.
- For acceptance/rejection criteria for capacitors under AC partial discharge testing, see Fig. 5.5.

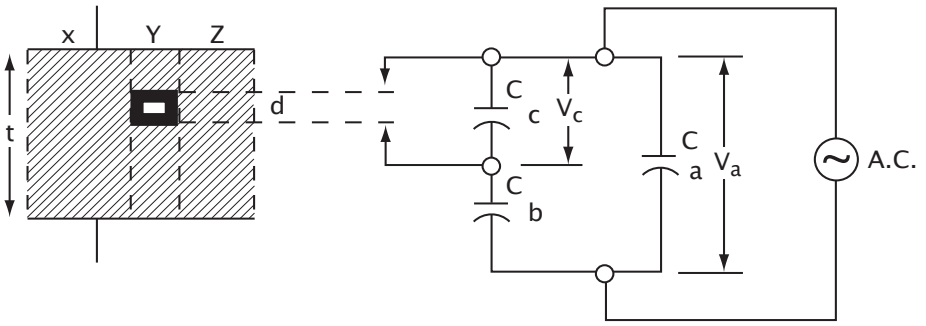

Figure 5.1. Equivalent circuit or model for void in dielectric, Ref. [13]. The left side of the figure is the dielectric with void. The right side is the equivalent circuit of void in dielectric for AC partial discharge testing.

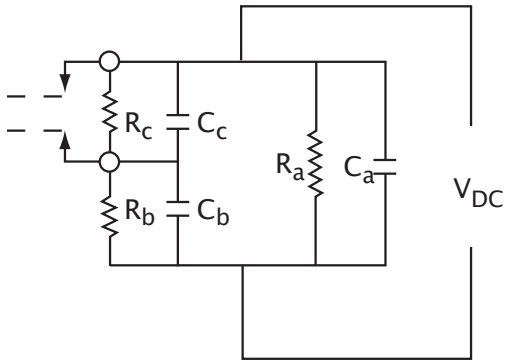

Figure 5.2. Lumped parameter circuit model of a cavity for the DC partial discharge case.

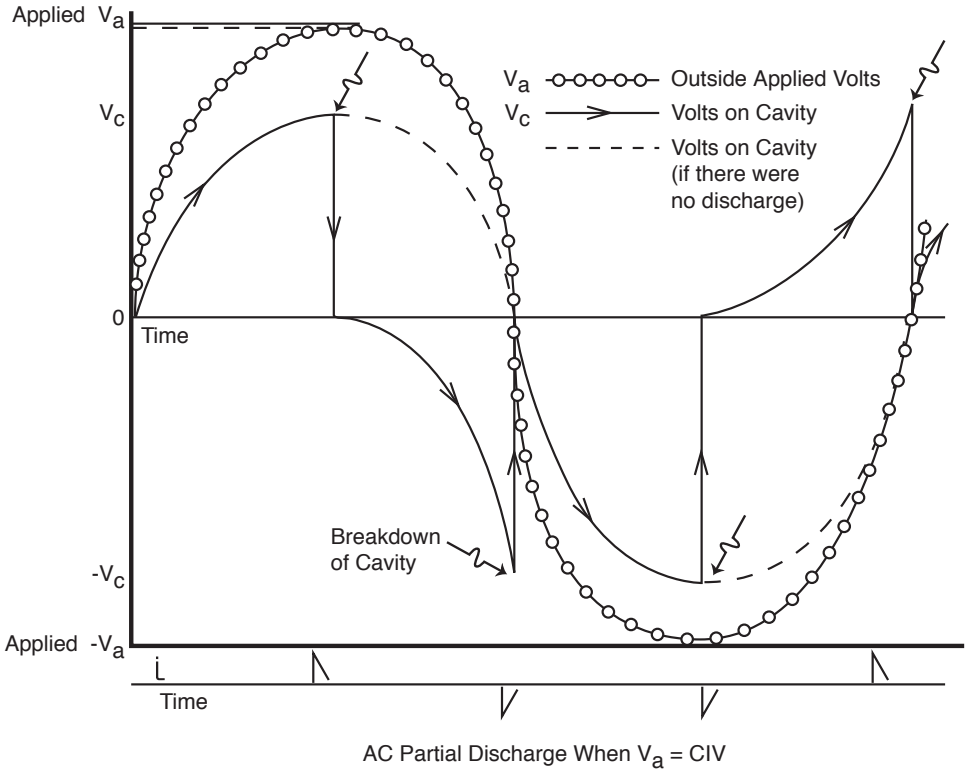

Figure 5.3. AC partial discharge when V_a=CIV, Ref. [7].

VOLTAGE ACROSS THE CAVITY OR VOID

Refer to Fig. 5.1:

(Basic 1) $C_c V_c = C_b V_b = C_{total} V_{applied}$

(Basic 2) $V_c + V_b = V_{applied}$

Therefore $V_c = \dfrac{V_{applied} C_b}{C_b + C_c}$

Assume 1 mil thick pancake void in a 40 mil thick capacitor, and $C = \dfrac{K e_0 A}{t}$

For X7R ceramic; $K \cong 2000$: $V_c = \dfrac{V_{applied} \times 50}{51} \cong V_{applied}$

For NPO ceramic; $K \cong 80$: $V_c = \dfrac{V_{applied} \times 2}{2 + 1} \cong 2/3\ V_{applied}$

For Polymer; $K \cong 4$: $V_c = \dfrac{V_{applied} \times 0.1}{1 + 0.1} \cong 1/11\ V_{applied}$

Also, Recharging of Cavity is by INSTANTANEOUS INDUCTION upon A.C. Applied Voltage

Figure 5.4. AC partial discharge.

ACCEPTANCE/REJECTION CRITERION

(1) $\left[\dfrac{\text{DC RATED VOLTAGE}}{1.41}\right] =$ RATED RMS VOLTAGE

(2) DERATING RULE for NASA $\rightarrow$ DERATE TO 60% V RATED

(3) THEREFORE CIV MUST BE $\geq$ $\left[\dfrac{0.60 \text{ DC RATED VOLTAGE}}{1.41}\right]$ VOLTS RMS

(YOUR CHOICE WHETHER CIV AT 10,50 OR 100 pC) $\geq$ $\left[0.42 \text{ DC RATED VOLTAGE}\right]$ VOLTS RMS

(4) THIS ENSURES THAT DURING SERVICE THERE WILL BE NO PARTIAL DISCHARGES.

Figure 5.5. AC PD testing.

B. Partial Discharge under DC Applied Voltage

Goddard Space Flight Center is involved in high voltage supplies and instruments, all of which are DC devices. For testing of integrity of potting jobs or other insulation in and around DC image tubes or circuit components the application of AC voltage is often *not* allowed.

The Theory shows that during *quiescent* DC application of voltage, the partition of it is according to the resistances of the cavity and the intact dielectric in series with it (Fig. 5.2 and 5.6). Because the resistance of the high resistivity dielectric is much greater than the resistance of the cavity, then on quiescent DC the cavity does not get much of the voltage across it. Moreover, after the first discharge, recharging is by slow conduction through the highly resistive dielectric. To quote from F. Krueger's book, *Discharge Detection in High Voltage Equipment: DC Voltage*, "When DC voltage is applied, discharges occur during the rise of voltage, as in the case of AC voltage. After the voltage has become constant, discharges occur only infrequently" (Figs. 5.6 and 5.7). This does *not* give enough data, on quiescent DC, during a reasonable observation time.

The question, therefore, is: How to change the DC partial discharge test to get enough data from it? The answer is to collect data on the up-ramp, then separately at the V_R plateau and then on the down-ramp. Measure pulse numbers, n, and their magnitude in picocoulombs, pC, *not* the CIV. For applied voltage versus time, see Fig. 5.8.

Also, one must realize that insulating materials have a "memory," especially ferroelectric materials such as ceramic capacitors of barium titanate. Before testing these capacitors with DC, therefore, they must be heated at 85°C for 12 h with leads shorted, to depolarize them from previous applied DC voltage.

- During quiescent DC voltage application, voltage partition is approximately according to Resistances of Cavity, R_c, and intact Dielectric in Series with it, R_b (see Fig. 5.2).
- R_b of high resistivity Dielectric > R_c of cavity.
- Therefore, on quiescent DC, the cavity does not get much of the applied voltage.
- After the first discharge pulse, recharging of the cavity is by slow conduction through the Dielectric.
- Approximate discharge frequency f P.D. : according to Densley, Refs. [1], [11], [12], and Rogers & Skipper, Ref. [23].

DC: $$f\text{P.D.} \approx \frac{1}{e_0}\,\sigma\,\frac{E}{E_i} \approx 1.13 \times 10^{11}\,\sigma\,\frac{E}{E_i}$$

σ = Conductivity of Dielectric
E = Stress in Dielectric
E_i = Discharge inception stress in Cavity.
(Stress = Electric Field)
e_0 = Permitivity of Empty Space

Figure 5.6. DC partial discharge (continued on Fig. 5.7, next page).

$$\text{If } E = E_i \text{ and } \sigma = \frac{1}{4\times10^{13}\ \Omega m} \quad \text{[Conathane]}$$

$$\text{Max. P.D.s } f = \frac{1.13 \times 10^{11}}{4\times10^{13}} \quad 1/\text{s}$$

$$\cong 3\times10^{-3}/\text{s} = 3 \text{ pulses}/1000 \text{ s} = 3 \text{ pulses}/16 \text{ min}$$

- THIS IS NOT ENOUGH DATA TO BASE ANY CONCLUSIONS ON IN A REASONABLE OBSERVATION TIME.
- DC CIV IS NOT A GOOD QUANTITY TO MEASURE, IN THE QUIESCENT DC APPLICATION.

Figure 5.7. DC partial discharge (continued from Fig. 5.6, previous page).

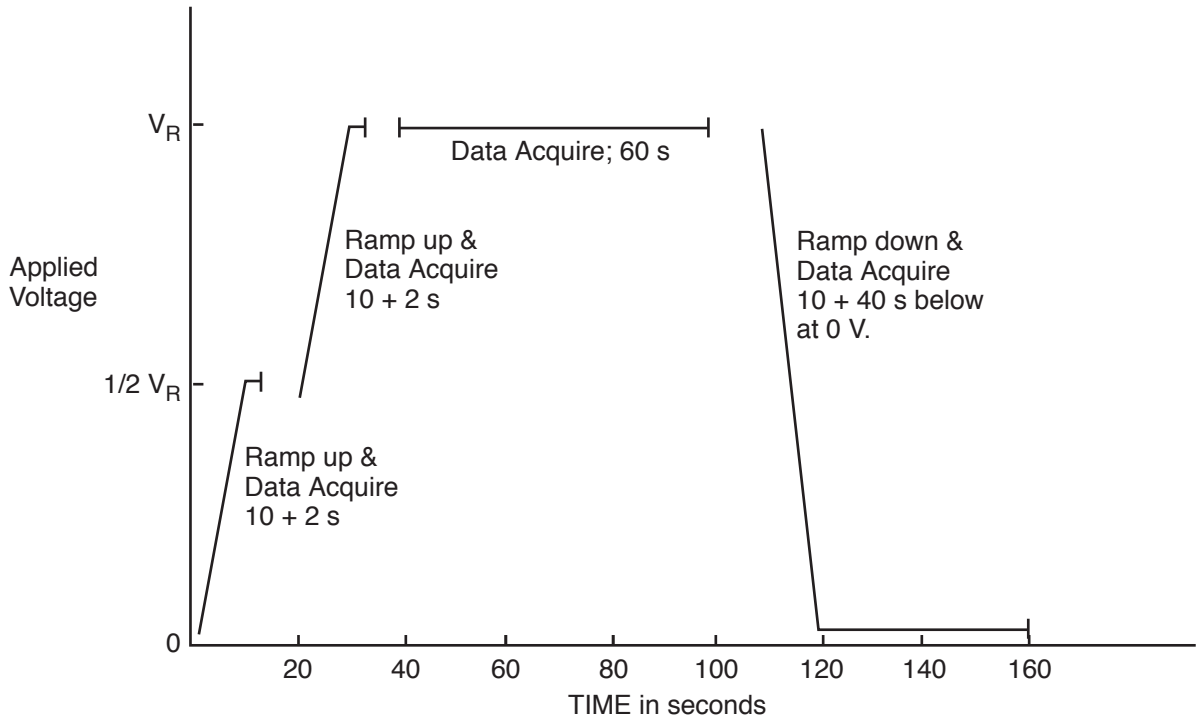

Figure 5.8. Voltage-Time profile for abbreviated DC P.D. test, Refs. [12], [21]. (The 60 s plateau at 1/2 rated voltage is omitted.)

Acceptance/Rejection Criteria for X7R, X5R BaTiO3 Disc Capacitors *of 1000 pF Capacitance*

Note: Before DC PD Testing, the capacitors must be heated at 85°C, for 12 h. Leads shorted, to depolarize. Do this every time before a DC PD test.

- On ramp-up to rated voltage:
  (1) No single pulse to be greater than 150 pC;
  (2) Sum of n_iq_i to be no greater than 3000 pC.

- On quiescent plateau of rated voltage:
  (3) No single pulse to be greater than 25 pC;
  (4) In 100 s of observation, the Sum of n_iq_i to be no greater than 150 pC, or "corona current" to be no more than 1.5 pC/s.

- On ramp-down to 0 kV:
  (5) Very little, if any, relaxation corona is usually observed on ramp-down of these highly *ferroelectric* materials like $BaTiO_3$. Much relaxation corona has always been associated with macroscopic cracks. Therefore, no more than 300 pC for sum of n_iq_i

- Also, no preferred peak distributions and no multiple corona bursts allowed.
- Naturally, <u>different capacitances</u> than 1000 pF have to be allowed different amounts of corona:
  (6) On the sum of n_iq_i, multiply by (C_{new}/1000 pF) ratio.
  (7) On the maximum charge content of single pulses, multiply by $(C_{new}/1000\ pF)^{½}$
  (8) Any capacitor whose partial discharge is notably higher (~ half an order of magnitude higher) than others from the same lot, should be rejected.
  (9) *NPO multilayer* capacitors: *No* PDs on ramps or quiescent VR Plateau. Any other behavior is rejected.
  (10) *X7R Multilayer:*
  PDs on up-ramp.
  Very little PDs on VR plateau.
  Little PD on down-ramp.
  Must be correlated/life tests, to get acceptance/rejection criteria.
  Meantime, use similar criteria as for discs.
  (11) *Z5U Multilayer, and Z5U disc:*
  Much PDs on ramps.
  Also PDs on VR plateau.
  Do not use.

II. Examples of Partial Discharge Data

Of the many DC data runs taken over the years, the next page shows a typical one for an X7R $BaTiO_3$ multilayer capacitor in Table 5.1. This capacitor was rejected, having too high a sum of n_iq_i on the ramp to rated voltage. Table 5.2 describes in words, that data one measures on a given set of capacitors when one chooses to do either a DC or an AC test or both. Table 5.3 gives two columns on DC data and one column of AC data, taken on 24 single disc capacitors. One can see that the lower half of the page of capacitors printed in Table 5.3 have much less picocoulombs for sum of n_iq_i on the ramp and 0 pC during the quiescent DC testing. The same lower half is also better on the AC test, in that the corona inception voltage is higher. The only serial number that does not "fit in" is S/N 27, which looks like the worst capacitor with lowest AC inception voltage of 1.4 kV rms, and yet it is not too bad on DC testing.

Table 5.4 shows DC partial discharge data for a 3 kV DC, X7R, multilayer capacitor. Its enlarged Destructive Physical Analysis (DPA) cross section photo of Figure 5.9. Table 5.5 is data for a 2 kV DC, X7R multilayer capacitor from a production lot that had electrical failures. Figure 5.10 gives the enlarged photo of its cross section by DPA and reveals several large pancake-shaped voids. This explains why Table 5.5 had so many numerous and energetic pulses as compared to the capacitor in Table 5.4. But one can not DPA every capacitor. And so, the partial discharge test is a good nondestructive method to reveal which capacitors will probably fail and which are risky to put into a circuit.

Table 5.1. Typical data for one multilayer capacitor; $BaTiO_3$, X7R; 27,000 pF 1 kV DC; Calibration: 4–500 pC: Amplifier: x10

Time Sec	kV	N total	4–25 pC n	25–100 pC n	100–200 pC n	200–300 pC n	300–400 pC n	400–500 pC n	Max pC	Sum n_iq_i pC
12	0–.5	13	8	2	1	1	0	1	401	952
*12	.5–1.0	342	211	89	18	11	7	6+	4,819	179,437
60	1.0	6	2	3	1				104	283
30	1.0–0	23	14	6	2	1			246	802

* By changing the amplifier to x1 before this ramp, the calibration becomes 40–5000 pC. This way, one "catches" the big pulses.

Table 5.2. PD measurement: Correlation between DC and AC data.

DC DATA	AC DATA
(I) One measures number of pulses, the pC content of each and computes sum of n_iq_i	One measures corona inception voltages at a given pC level (100 pC for X7R. 20 pC for NPO).
a) On the ramp to V rated b) At V rated for 100 s. c) On ramp down to 0 V	CIV volts
Sum of n_iq_i and max pC pulse- on ramp to VR and at VR	
(II.) Effect: In a set of capacitors, from best to worst:	
Sum of n_iq_i goes up by factor of 6 or 7 on ramp, from 1,330 pC to 9,680 pC, for example.	CIV volts only decreases by 30%, that is from 2.2 kV to 1.5 kV rms

Table 5.3. Correlation Between DC and AC Data; Single Disc D64 X5R 192M 5 kV, Maida; Post Burn-In Corona Test.

	DC DATA		AC DATA
S/N	0–5 kV in 20 s ramp; Sum of $n_i q_i$ on ramp (in pC)	Quiescent at 5 kV 100 s after wait 60 s (in pC)	AC corona inception voltage at 100 pC (in kV rms)
1	8020 pC	369 pC	1.5, 1.65 kV rms
2	7525	69	1.6, 1.65
26	8980	0	1.7, 1.9
28	9680	21	1.8, 1.8
39	7520	12	1.6, 1.6
41	7580	0	1.8, 1.8
44	6050	11	1.7, 1.8
70	7820	0	1.65, 1.7
72	6280	28	1.8, 1.8
90	6810	74	1.6, 1.6
86	5480	0	1.7
55	5800	0	1.8
27	5730	0	1.4, 1.5
11	1960	0	1.9, 1.9
17	1828	0	1.9, 1.9
18	1330	0	2.1, 2.0
51	1480	0	2.0, 2.1
53	1750	0	2.1, 2.1
60	1650	0	
73	1290	0	1.9, 2.1
83	1970	0	2.0
43	2220	0	2.1
49	2280	0	1.8, 1.8
84	2590	0	1.9
76	2900	22	2.0
15	3930	0	2.1, 2.1

Table 5.4. One multilayer capacitor DC PD test; new Novacaps for Mr. Birsa; S/N 4.1 2020 B 332 M 302S, X7R, 3 kV DC.

Time Seconds	kV	N Total	4–25 n*	25–100 n	100–200 n	200–300 n	300–400 n	400–500 n	Max pC	Sum $n_i q_i$ pC
10	0-1.5	0								
60	1.5	0								
10	1.0-3	13	9	4					89.0	295
60	3	0								
10(+40)	3-0	0								
Reverse Polarity										
	0–1.5	1							22.0	22.0
	1.5	0								
	1.5–3	5	3	1	1				143.1	226.7
	3	0								
	3–0	0								

* Where “n” is the number of pulses within the noted range. This was done at Calibration: 4–500 pC; Amplifier: x10

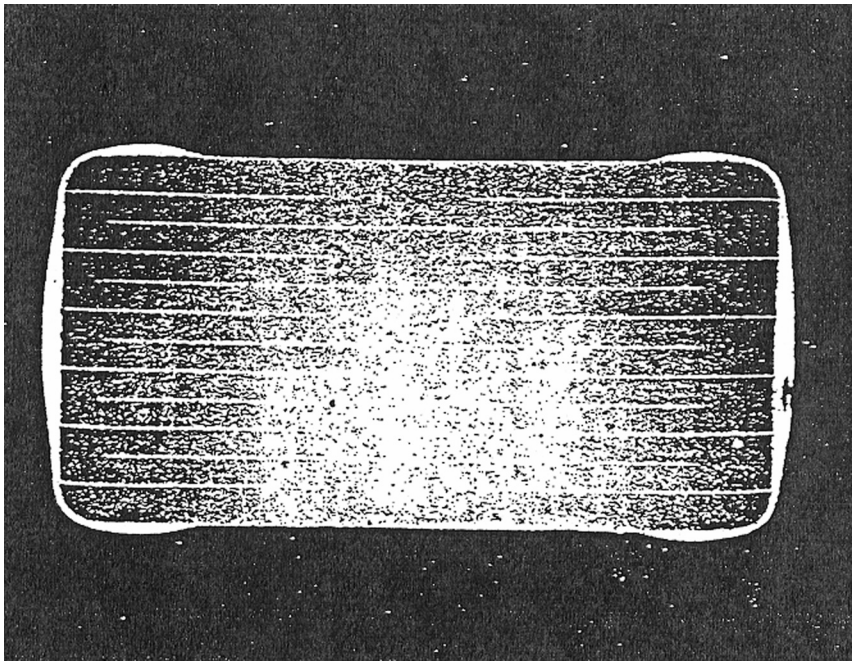

Figure 5.9. Cross section of capacitor S/N 4.1, enlarged.

Table 5.5. Another multilayer capacitor DC PD test from the lot that had failures, for Mr. Birsa; S/N 3.0, 2020B 103M 202S, X7R, 2 kV DC.

Time Sec	kV	N total	4–25 pC n	25–100 pC n	100–200 pC n	200–300 pC n	300–400 pC n	400–500 pC n	Max pC	Sum $n_i q_i$ pC
10 60	0–1 1	484+ 0	319	57	40	24	25	23+	504+	37,013+
10 60	1–2 2	1597+ 5	896 2	603 3	74	22	7	6	4,844+ 75	598,860+ 205
10 (+40)	2–0	329+	138	93	54	22	14	14	511+	31,132+

NOTE: This was done at Calibration: 4-500 pC; Amplifier: x10

DO NOT USE THE ABOVE CAPACITORS

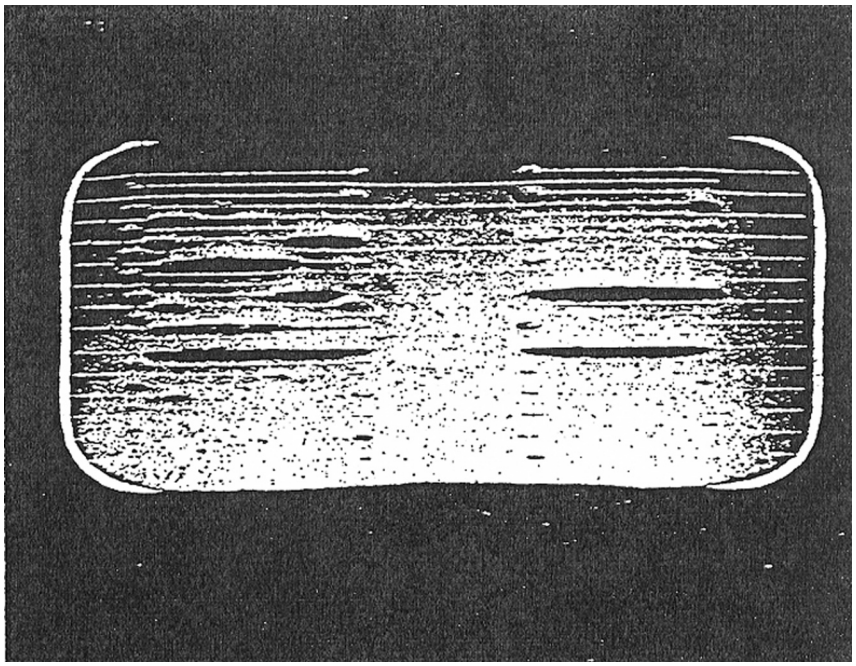

Figure 5.10. Cross section of capacitor S/N 3.0, enlarged. (Note pancake voids.)

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APPENDICES TO CHAPTER 5

Appendix I to Chapter 5: Biddle Co. Partial Discharge Detection Equipment.*

This is included as a help to new technicians at Goddard Space Flight Center.
*The James G. Biddle Co. has gone out of business. Repair on equipment can still be obtained.

Appendix II to Chapter 5: Detailed Directions for Partial Discharge Measurement, for Capacitors.

This is included as a help for new technicians at GSFC.

Appendix III to Chapter 5: Directions for GLAST Project Flex Cable Corona Test

This is an example of corona testing of different items than capacitors.

Appendix IV to Chapter 5: MIL-PRF-49467B; 2 May, 2001, Directions for AC Corona Testing of Multilayer Ceramic Capacitors.

This illustrates the approval of this type of testing.

Appendix V to Chapter 5: AC Corona Test of Transformers at 50–100 kHz

By, J.D. McCormick and M. Mogavero, Westinghouse Corp., Baltimore, Maryland, S-311320-CAPS/IS50 transformer, Sept. 1994. This illustrates the corona testing of transformers at closer-to-actual operating frequency than with the usual 60 Hz commercially available equipment.

Appendix I to Chapter 5

BIDDLE* CO. PARTIAL DISCHARGE DETECTION EQUIPMENT

**The James G. Biddle Co. has gone out of business. Repair service can still be obtained.*

I. The Biddle equipment can be in one of the *three* possible configurations:

(1) DC only

(2) AC only, at 60 Hz.

(3) AC and DC superposed

It is often in either (1) or (3). If in (3), (the superposed mode), *the voltage limits are: 12 kV rms maximum* as read on the RED display and *38 kV DC* as read on the RED display on the AC control cabinet.

Also, if in (3), then the DC ammeter will register some current when DC voltage is applied.

The diagram on next page illustrates the connections in the test cabinets, for modes (3) and (2) above. You must open all the test cabinet doors to inspect and make changes if desired. See Figures 5.A.I.1 and 5.A.I.2.

II. Read the Biddle books (3 maroon-colored direction books).

III. It is imperative that no ordinary cloths or paper towels or chamois cloth be used inside the test cabinets. Only lint-free cloth obtained from GSFC Materials Branch is permitted (small hard cotton squares). Damage to the Biddle system is "murder" to repair because of the size of the equipment. A Moving Van is required to return it for repair.

IV. The polarity of the high voltage output can only be changed by opening the DC HV supply and reversing some jumpers under the oil using clean plastic pliers. Only experienced people are allowed to do this. No dust or flakes of skin must be allowed to fall into the oil during this operation.

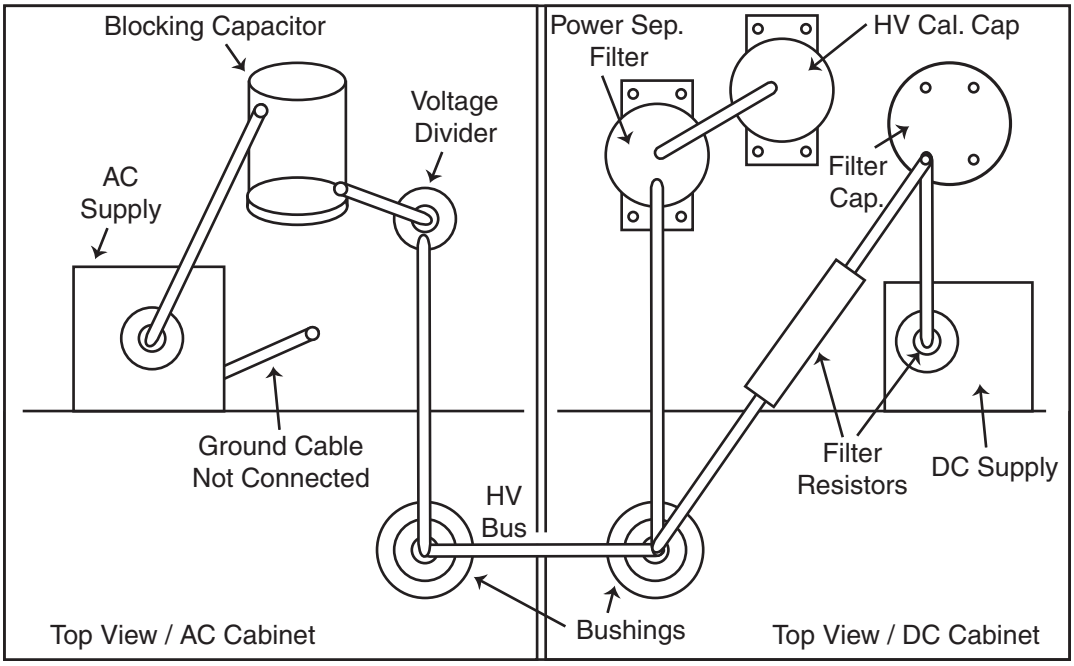


Figure 5.A.I.1. Bus arrangement for AC and DC superposed voltages. Maximum is AC 12 kV rms 60 Hz, DC 38 kV DC, Ref. [9].

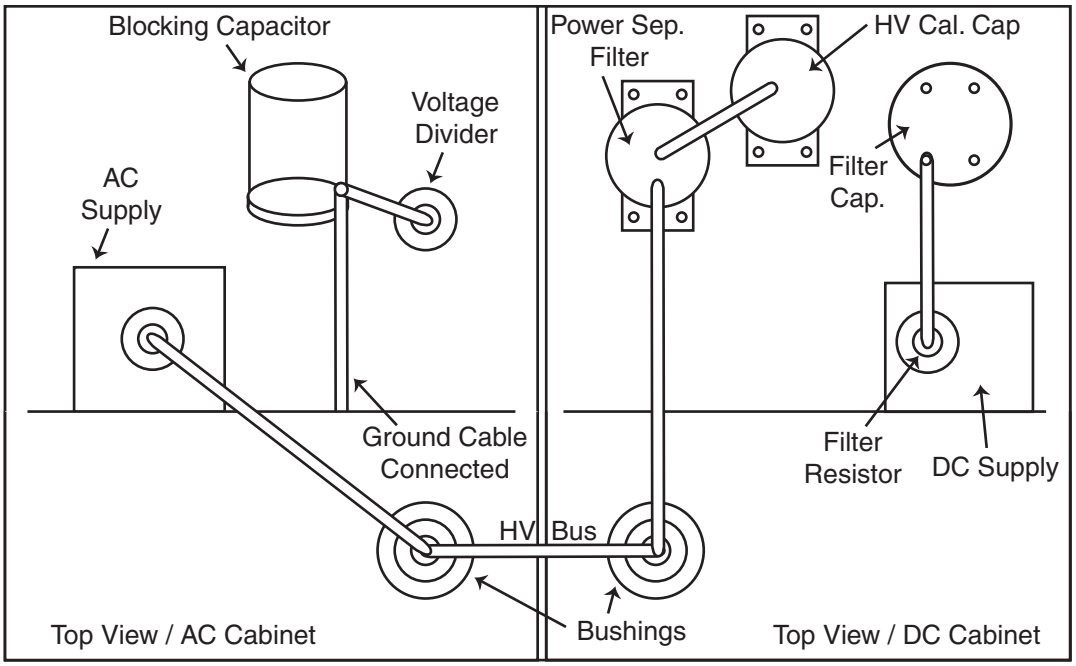


Figure 5.A.I.2. Bus arrangement for AC only, Ref. [9].

R.S. Bever, A.P. Ruitberg, C.W. Kellenbenz, and S.M. Irish

Appendix II to Chapter 5

SOME DETAILED DIRECTIONS FOR PARTIAL DISCHARGE TESTING, BOTH DC AND AC

General Comments

Before you start, *you must know:*

1. The condition of your equipment: Is it connected for the DC mode or for the superposed mode which is used for AC PD measurements? What is the polarity of the high voltage terminal with respect to ground? All the settings of the amplifiers, calibrator, control knobs need to be inspected and be set to your needs. You cannot assume that any of the settings are still the same as when you last used the equipment.

2. The properties of the materials or assembly you are testing: all insulating materials have a memory, that is, if high voltage has been applied previously in a certain polarity the material remains polarized in that polarity, even if the leads to it have been shorted at room temperature. This is especially true of ferroelectric materials, such as the ceramic capacitors (except the NPO formulation). Therefore, before PD testing, these materials need to be heated with leads shorted, to obtain consistent results from one test to the next. Despite this depolarization procedure, there is still some remnant memory and the sample should always be connected in the same polarity, so as not to introduce an unwanted variable of polarity reversal.

   The conductivity and the dielectric constant of the material have a vast influence on the partial discharge to be expected. The greater the conductivity, the more partial discharges are to be expected on DC testing for a given defect site. Also the higher the dielectric constant, for a given externally applied voltage and a given defect, PDs will incept at a lower applied voltage, both on AC and on the ramps during DC testing.

   This means that you cannot blindly apply the same acceptance/rejection criteria to everything you test. Therein lies the great difficulty of interpreting the PD data.

3. The particulars of the equipment are contained in the manuals supplied by the manufacturers of it, and kept in the file cabinet in the high voltage laboratory. There is a DC System, an AC System, a High Voltage DC power supply, and an AC supply, a Multichannel Analyzer (MA) and a Computer System. Because the last two items are probably different for each laboratory, then *detailed* directions must be supplied for the technicians there.

I. DC PARTIAL DISCHARGE MEASUREMENT

*The James G. Biddle Co. has gone out of business, however, the equipment is still fully functional.

A. De-polarization De-aging

Ceramic capacitors, being mostly $BaTiO_3$ with additives, are highly ferroelectric. Therefore, they always need to be de-polarized or de-aged before DC partial discharge measurements (DC PD) are taken. Mount the capacitors in a shorting jig. Be careful not to mechanically stress the leads where they exit from the capacitor body. Place in a *clean* oven. Raise the temperature in about 15 min to 85°C and hold at 85°C for a total of 12 h. Cool back to room temperature in about 15 min. The 12 h of heating need not be continuous, e.g., it can be 7 h and 5 h.

The capacitors will still have a small amount of polarization after this treatment. It, therefore, is important to be consistent in polarity. In the DC PD measurements, be sure to connect the leads in the same polarity as the last previous

high voltage connections, e.g., as in the DWV High Voltage power supply or in the Voltage Conditioning High Voltage power supply. If connections are made in reverse, make a note of it.

B. Calibration

This must be done with great care every time a new batch of capacitances is DC PD measured. This is because the sensitivity of the equipment depends on the test sample capacitance. Every time the test sample capacitance is changed, one must recalibrate.

In the Biddle Test Cabinet

Be sure you know the polarity of the high voltage terminal with respect to ground. Connect the test sample capacitor in the same polarity as in the last previous high voltage exposure or know if reversed. Now, also connect the *low voltage calibration capacitor, if no high voltage calibration capacitor is in the test cabinet.* Connect its B and C cable to "Cal. Signal out". (Be sure after the calibration is accomplished, as below, to remove the low voltage calibration capacitor.) If, however, a high voltage calibration capacitor is in the system, omit the last two steps.

On the Biddle Control Console

Have the amplifier on the x10 position and switch on the *Direct* Calibration. Two separate calibration signal peaks should now be visible on the oscilloscope (each peak also has a small secondary peak at its foot). Go by the higher peak.

Now dial up the desired amplitude of the calibration signal peaks. Be sure to do this or check on it because it may have been changed by someone. Suggested values are given below.

Suggested Calibration Signal Amplitudes

NPO	**X7R <10,000 pF**	**X7R >10,000 pF**
200 pC	500 pC	1000 pC

The values above are merely suggestions for the very first time that a given batch of test capacitors is being DC PD tested. The aim is to catch the most energetic pulses while at the same time not cutting off the lowest ones. Once the first capacitors of a given batch have been satisfactorily measured, then on later measurements on the same group, the same calibration signal amplitude must be used. Remember also that once the high voltage has been raised on a given capacitor, you cannot go up on it again in the same polarity without de-polarizing. You can reverse polarity and go up again, but the PD pulses will be approximately double (hysteresis in ferroelectric materials).

Now, change the Amplifier Amplitude Vernier until the highest of the two peaks is 6.5 cm high. This corresponds to the full scale on the *x*-axis of the MA, which is used as the quantitative data read-out instrument for DC PD measurements. You will have to fine-tune the 6.5 cm after turn-on procedures on the MA turn-on procedures, so do not yet remove the low voltage calibration capacitor.

On the Multichannel Analyzer

Detailed directions must be obtained in the particular laboratory. The MA has two markers that move on the *horizontal* axis, and the right-hand marker in the extreme position on channel 1024 should correspond to the *vertical* calibration signal amplitude chosen for the Biddle *vertical* pulse height on the Biddle oscilloscope. This calibrates the horizontal position of the markers in picocoulombs, and one can thus read off the number of pulses, *n*, between certain picocoulomb values.

When calibration is complete, remove the low voltage Calibration Capacitor from the Biddle Test Cabinet and tighten the corona ball on the HV terminal.

C. DC Partial Discharge Measurement (DC Ramp Test)

Be sure the low voltage calibration apacitor is removed.

Be sure the test sample ends of leads are caught into and buried inside of the alligator clip jaws of the high voltage connections to the Biddle terminals. No cut ends of terminals must stick out. Be sure the entire test sample and all naked metal of the connecting cables and fixturings are immersed in Fluorinert liquid FC-43 if the voltage is going to be 2 kV or higher. Actually, this should also be done at lower voltages. (The sample can also be placed in high vacuum.)

1. Set up regions of interest between markers on the MA according to your instrument's directions.
2. Be sure on the Biddle cabinet the voltmeter switch is in the lowest position. The variac must be turned full down or counterclockwise. Turn on the high voltage. The red light should come on.
3. Acquire pulses for 30 s at 0 V. There should be no pulses unless there is undesirable noise on the electric line. (In the past, there has been noise below channel 13 or so, but you can arrange not to count it by having the left maker on channel 14.)
4. Acquire pulses while slowly raising voltage to ½ V-rated in 10 s and acquiring for 2 s more. Record the total number of pulses; also record the pulses within the regions of interest and the maximum pulse value in picocoulombs.
5. If in step 4 there were pulses above ½ full scale, then chances are that during the next ramp to full-rated voltage for X7R capacitors, there will be pulses in the several thousand picocoulomb range.

To catch these high pulses, turn the amplifier gain to x1. This now will, of course, make the MA *x*-axis go from 45–5000 pC, instead of 4.5–500 pC. Because you changed the MA, now you must multiply the picocoulomb values by 10 before recording. Acquire pulses while raising the voltage in 10 s to V rated. Wait 2 s more. Record all data as in Step 4.

6. Return the amplifier gain switch to x10. Be sure to do this. The previous data recording should take up to 60 s of waiting period between taking the hands off the voltage variac and doing data acquisition for the truly quiescent V rated plateau. So now, at V rated, acquire pulses, and let run until the preset time of 60 s stops the acquisition. Record all data as before.
7. Acquire pulses, data while running the voltage variac down as fast as desired. Then, wait out the relaxation pulses for about 30 s more. Stop. Record all data as before.
8. Turn off the High Voltage. Discharge the HV terminal in the test cabinet with grounding wand. Remove the test sample and replace it with another sample. Close door. Repeat entire procedure III from step 2 onward until a different value of capacitance comes up at which time the calibration procedure has to be repeated, as in section II.

After practice, the entire measurement should take no more than 5 min per sample.

Table 5.A.II.1. Typical data DC PD for a single capacitor; multilayer $BaTiO_3$, X7R; 27,000 pF, 1 kV DC

Time Sec	Amplifier Gain	kV	n	4–25 n	25–100 n	100–200 n	200–300 n	300–500 n	Max pC	$\sum n_i q_i$ pC
12	X10	0→.5	13	8	2	1	1	1	401	952
12	X1	.5→1.0	342	211	89	18	11	12	4,819	179,437
60	X10	1.0	6	2	3	1			104	283
30	X10	1.0→0	23	14	6	2	1		246	802

Table 5.A.II.2. Abbreviated version typical DC/PD data for two capacitors. Multilayer $BaTiO_3$, 820 pF, 3 kV DC

MFR: WRT SET #2 S/Ns: 2209-2210; Cap: 820 pF; Vrated: 3 kV; Dielectric: X7R; Calibration: 4–500 pC; Amplifier: X10

S/N	0→V/2			V/2→V			60 s at V			V→0		
	n	Max	$\sum n_i q_i$ pC	n	Max	$\sum n_i q_i$ pC	n	Max	$\sum n_i q_i$ pC	n	Max	$\sum n_i q_i$ pC
2209	0	0	0	86	184	3816	0	0	0	0	0	0
2210	0	0	0	114	269	7346	0	0	0	3	76	133

Results: Accept S/N 2209 because $\sum n_i q_i$ ~3000 pC.
Reject S/N 2210 because $\sum n_i q_i$ too high on ramp-up.

D. DC: Approximate Acceptance/Rejection Criteria for 1000 pF, X7R, X5R $BaTiO_3$ Disc Capacitors

• On ramp-up to rated voltage:
  (1) No single pulse to be greater than 150 pC;
  (2) Sum of $n_i q_i$ to be no greater than 3000 pC;

• On quiescent plateau of rated voltage:
  (3) No single pulse to be greater than 25 pC;
  (4) In 100 s of observation; the Sum of $n_i q_i$ to be no greater than 150 pC, or "corona current" to be no greater than 1.5 pC/s.

• On ramp-down to zero:

  Very little, if any, corona is usually observed on ramp-down in these highly ferroelectric materials. Much relaxation corona has always been associated with a crack in the $BaTiO_3$. No more than Sum $n_i q_i$ ≅ 300 pC.

• Also, no preferred peak distributions and no multiple corona bursts allowed.
• Naturally, different capacitances than 1000 pF have to be allowed different amounts of corona, as follows:
  (5) On the Sum of $n_i q_i$, multiply by (C_{new}/1000 pF) ratio.
  (6) On the maximum charge content of single pulses, multiply by (C_{new}/1000 pF)^{½}.

• Finally, any capacitor whose partial discharge is notable higher (half an order of magnitude higher) than others from the same lot should be rejected.

II. AC PARTIAL DISCHARGE MEASUREMENT

A. De-age

Same as in DC; it is not absolutely necessary, but would be advisable for the sake of consistency.

B. Calibration

Same as in DC. Be sure it is done AFTER the extra bus-bar has been connected from the A.C. cabinet to the High Voltage terminal in the D.C. cabinet. The Multichannel Analyzer is not absolutely necessary for the A.C. measurement, but is nice to turn on to determine when 100 pC pulses appear with greater accuracy than by just watching the Biddle oscilloscope. For A.C. corona measurements, calibrate with 200.0 pc calibration signal injection for *all* capacitors. In this way, the 100 pc pulses will be about 3 cm high on the Biddle oscilloscope and will be ½ of the way along the MA screen, and easily visible. For NPO capacitors, 25 pC inception voltage should be looked for and recorded.

C. High Voltage AC PD Measurement

Turn lights off in the room after sample is connected. Turn on the AC High Voltage. Slowly raise the AC High Voltage Variac while also watching the Biddle oscilloscope and also the red test sample voltage readings on the digital voltmeter on the Biddle AC control cabinet. When pulses appear on the Biddle oscilloscope that correspond to 100 pC, then stop raising the voltage. (If 200 pC = 6.5 cm, then 3.25 cm = 100 pC.) Alternatively, have the MA in the Acquire mode with infinite running time and watch for pulses appearing beyond the 100 pC marker. Stop raising the voltage, and read the red digital voltmeter. Turn voltage variac down immediately. The voltage that was recorded is the Corona Inception Voltage or CIV. Repeat at least once. The CIV is defined as the voltage at which pulses higher than 100 pC (or 25 pC for NPOs) keep coming in for 5 s. Average the two voltage readings. Do not leave the voltage on where 100 pC pulses persist for longer than 5 s. The CIV is, of course, an AC rms voltage.

D. Voltage Limit

This is important for NPO capacitors. For these capacitors, it is possible that the CIV is quite high. Also, the X7R capacitors may be better than previous experience indicated. AC applied voltage on all of these capacitors may be damaging because of heating effects. Therefore, the following maximum voltage should not be exceeded:

$$\text{Maximum AC rms volts} = \frac{70\% \text{ of DC V rated}}{1.43} = .49 \text{ DC V rated allowed to be applied}$$

For a 5 kV rated DC Capacitor this equals 2.5 kV rms AC

for 2 kV = 1.0 kV rms
for 1 kV = 0.5 kV rms

D. Acceptance/Rejection Criteria: Approximate

For X7R, X5R, Z5U: Reject if, at 100 pC levels, CIV <50% DC V_r in volts rms

For NPO, $SrTiO_3$: Reject if , at 25 pC level, CIV <50% DC V_r in volts rms

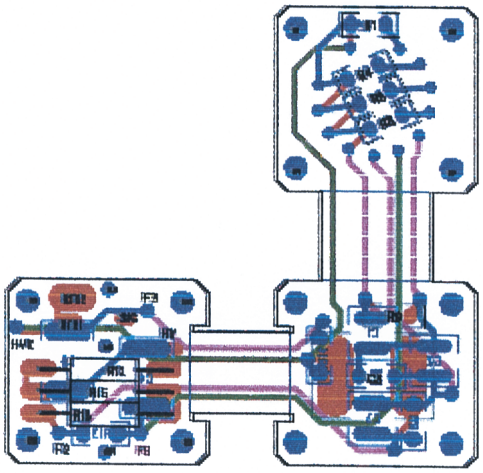
Appendix III for Chapter 5

DIRECTIONS FOR CORONA TEST OF FLEX CABLE BOARD

Flex Cable Board Corona Test

Corona testing will be performed to detect defects within the flex cable configuration. One series of tests will be conducted to examine the cabling between boards. The second series will test for defects between layers within the boards.

GLAST Photomultiplier Flex Board PWB 2054578 Rev - 02/9/04



Primary Component Side Layer 1 of 4 | Flex Layer 2 Layer 2 of 4 | Flex Layer 3 Layer 3 of 4 | Secondary Component Side Layer 4 of 4

Figure 5.A.III.1

The Resistor Network flex-cable version is shown above: ¼-in Ultem spacers will be used to hold the boards in flight configuration. As this test is strictly making an evaluation of the board itself, no components will be mounted. The Code 563 Biddle Corona Test System in Building 20 will be used for corona detection. Testing will cover the charge range from 10 pC to 500 pC. The sample will either be tested in Fluorinert FC43 or in vacuum at pressure less than l0 x 10E-6 torr.

Clean gloves will be used when handling the boards for all operations.

#24 AWG bus wire will be installed in the following tube pin locations: Pins 5, 6, 7, 8, and 13.

A test lead will be installed on C5+.

Table 5.A.III.1. Apply voltage according to the table below and record data in the test sheet.

Testing	+HV	Ground	
Between cable layers	Pin 8	Pin 13	
Within cable layers	Pin 7	Pin 5	
Board to cable	C5+	Pin 6	
Board top to board bottom	C5+	Pin 8	

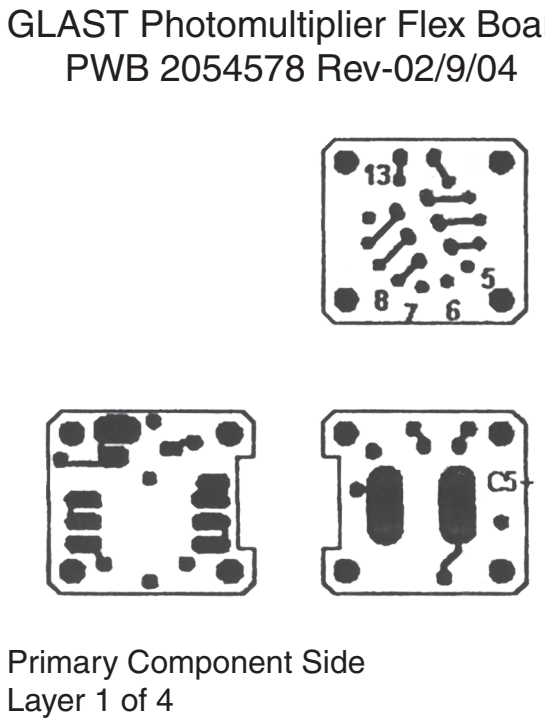


Figure 5.A.III.2

Table 5.A.III.2. Flex-cable resistor network corona test. Apply voltage according to the table and record data in the test sheet.

	Corona Counts									
Test Points	0–2 kV	2 kV	2 kV to 4 kV	4 kV	4 kV to 6 kV	6 kV	6 kV to 8 kV	8 kV	8 kV to 10 kV	10 kV
Pin 8 to Pin 13										
Pin 7 to Pin 5										
C5+ to Pin 6										
C5+ to Pin 8										

Appendix IV for Chapter 5

AC Corona Test for Capacitors, Fixed, Ceramic, Multilayer, High Voltage (General Purpose) EXCERPTED FROM MIL-PRF-49467B; 2 May 2001

MIL-PRF-49467B

AC PARTIAL DISCHARGE (CORONA) TEST

B.1 SCOPE

B.1.1 Scope. This appendix details the detection and measurement of partial discharge (corona) I in 3.10 and 4.8.6. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

B.2 APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

B.3 REQUIREMENTS AND DEFINITIONS

B.3.1 Supply Voltage. The supply voltage for AC partial discharge tests shall be variable AC voltage at a frequency of 60 Hz ±5 percent and shall be measured in AC volts rms with a tolerance of ± 5 percent of the AC test voltage.

B.3.2 Sensitivity. The partial discharge detection system's sensitivity depends on the capacitance of the test specimen. The test specimen shall be connected during system calibration and the sensitivity requirements shall be:

a. For capacitances of less than or equal to 0.005 μF, system sensitivity shall be able to detect 5 pC or less;
b. For capacitances above 0.005 μF, to and including 0.1 μF, system sensitivity shall be able to detect 15 pC or less;
c. For capacitances above 0.1 μF to and including 0.47 μF, the sensitivity shall be 50 pC or less.

B.3.3 Corona inception voltage (CIV). CIV at a given pC level shall be defined as the voltage at which continuous partial discharges can be recorded at that pC level. This is above the minimum sensitivity, as the applied voltage is increased at a constant rate.

B.4 TEST CONDITIONS AND PROCEDURE

B.4.1 Connection. The capacitor under test shall be connected between the high voltage terminal and ground of the detection system with insulated, corona-free cables. The capacitor, its leads, and bare metal connecting clips shall be immersed in FC-40 or FC-43 dielectric fluid (fluorinert) or equivalent.

B.4.2 System calibration. The system shall then be calibrated in accordance with the requirements of B.3.2.

B.4.3 Application of voltage. The applied voltage shall then be increased at a constant rate of approximately 0.2 kV rms/second. The maximum test voltage shall not be more than 42 percent of DC rated voltage.

B.4.4 Measurement. The maximum voltage specified in B.4.3 shall be maintained from 1 second to 5 seconds. If the maximum corona pulse exceeds 100 pC amplitude in this time period, the component shall be considered to be a failure. The voltage shall then be decreased to 0 volts.

Appendix V for Chapter 5

AC CORONA TEST OF TRANSFORMERS AT 50–100 KHZ FREQUENCY

By, J.D. McCormick and M. Mogavero
Westinghouse Corp., Baltimore, Maryland
S-311320-CAPS/IS50 transformer, Sept. 1994

CORONA TEST PLAN FOR N.A.S.A. TRANSFORMER (with actual changes in parentheses on schematic—see page 2)

I. TEST

A) Demonstration was performed this date of the Corona Test described in Ref. 1 attached. Deviations taken from the described procedure included:
   1) The High Pass filter was set for 200 kHz instead of the 500 kHz described to make sure low frequency corona did not get filtered out, as corona frequencies can start as low as 300 kHz.
   2) C-1 was a 22 pF, 4 kV capacitor instead of the calculated value of 80 pF and the resonant frequency for each unit was still about 1/2 of the goal of 75 kHz. This was due to the internal capacitance of the transformer as well as the Power Separation Filter in the test set that tended to allow the circuit to load at higher frequencies making it impossible to drive it to the specified value of 2000 V p-p above about 40 kHz with the existing 400 W amplifier. (Additional work could have possibly increased this frequency but the ability to reach 75 kHz is in doubt.)

It must also be noted that the circuit sketch had an error that was pointed out by Art Ruitberg from NASA. The "Cal Signal" was injected into the junction of C-1 and the UUT rather than the top of the series resonant circuit (note correction).

B) Test results were (see attached photographs):
   1) A 5 pC calibrated signal measured 15.2 mV on the oscilloscope.
   2) The first unit demonstrated had 24.6 mV of corona. It must be noted that there were air bubbles in the mold material around the secondary coil of this unit and poor adhesion of the material to the inside of the Ultem case. For these reasons a third secondary coil was manufactured.
   3) The second unit had 6.08 mV of corona.
   4) The secondary coil from the first unit was removed and replaced with another that had just completed manufacture with the new secondary coil the transformer had 6.40 mV of corona.

II. MANUFACTURE

In addition to the manufacture of a third secondary coil as described above, several other surprises and deviations from the quote (ref. 2) must be noted.

A) Additional Machining Steps:
   1) The Housing, Transformer Mold, drawing 1308772 identified a qty. of two .055 inch dia. holes to allow for the .062 inch dia. high voltage leads to penetrate the case. The cases were returned to the machine shop to have these holes enlarged to .062 in. after telecon with Ken at N.A.S.A. verified that this problem had been recognized by them.

2) The secondary coils that were wound by Westinghouse personnel at N.A.S.A. and verified by them, had a height slightly higher than the top of the Ultem case (.469 in. coil height vs. a case height of .460 in.) after they were glued into the cases. Request from N.A.S.A. by telecon to have .030–.040 in. of mold material above the coil wire resulted in the need to gently push the secondary coil wires down as far as possible after they were glued into the case (resulting in getting the wire just at the top of the case) and then building up the case with a temporary dam so that the material extended above the top of the case. The internal spacing between each core was measured and the mold material machined down to allow .002 in. clearance between the secondary and the core. This resulted in the molded secondary coil for unit number 2 being .492 in. (.032 in. of material above the coil wire) and molded secondary number three being .494 in. (.034 in. of material above the coil wire). It must be noted that this was a relatively expensive deviation as Westinghouse expected to pour the cases to the top with no further treat nor machining. The Ultem case had to be remachined to its original dimensions as it was almost impossible to remove the mold material from the outside of the case.

B) Materials

1) All materials listed in the fabrication specification as well as the solder terminals were to have been supplied by N.A.S.A. (see ref. 2 first bullet and N.A.S.A. drawing 1308769). This was not always the case. The 200 proof alcohol, the Ambion Insulstrip, the Stycast 3050 mold material, the Epon/Versamide adhesive and the solder terminals were all acquired through Westinghouse.

2) The Stycast 3050 was a very difficult material with which to work. It tended to explode into the vacuum chamber and adhere strenuously to anything it contacted including the mold release. .Although several methods were used including immediate insertion into an 80°C. oven and several hours of room temp. settling prior to insertion, Westinghouse has not yet gotten a good handle on the proper method to use to make sure that there are no voids in the material. Art Ruitberg felt that the 80°C. cure temperature may not have been correct although that was received from Grace by telecon. The second unit molded had air bubbles around the coil and poor adhesion to the case as described above. The third secondary had a hole in it that was filled with deaired material and recured. After this second cure the Ultem case cracked. We need to either get a process or spend some time to develop one prior to continued use of this material. It must be noted that in telecon with Grace Chemical, they suggested a Stycast 2850 material as it has better high voltage dielectric and thermal transfer characteristics.

C) Processes

Westinghouse expected to have N.A.S.A. processes and procedures already developed for the application of adhesives and molding (ref. 2 fifth bullet). In reality it was necessary to acquire this information from the manufacturers and generate our own information for manufacturing personnel.

D) Assembly

The assembly generally went well. Other than the hole for the high voltage wire, the only other problem was that the high voltage wire was difficult to ball solder and three of the four operators who tried (all with current Westinghouse high voltage solder certification) had trouble getting a good solder ball. It was decided to attach the primary wires to the terminals during assembly due to their size (AWG #34) and the fact that they would be needed to perform voltage ratio test. All solder attachments to the high voltage wire were made using a low corona solder ball per Westinghouse process. These were inside the secondary coil case. The primary coil solder attachments to the terminals were made with best commercial practice.

III) SUMMARY

As with any development task, this one had deviations from what was expected and surprises in results. Excellent responses from N.A.S.A. and material suppliers were a great help in getting a good handle on these deviations and surprises. Conversation with Art Ruitberg from N.A.S.A. identified a stress relief that should have been applied to the Ultem case after machining and prior to use. Application of this stress relief may have eliminated the cracked case.

Future use of this material will have stress relief performed. A hold on the charge number for two months was a slight perturbation but all material and information were held ready so that little was lost once the spending was approved. The corona test demonstration went well after some initial start-up problems although, as described above, the test frequency was lower than anticipated. NASA has accepted the units with a few comments concerning poor machining quality that will be addressed with the machine shop. (Some of this may have been the result of machining the mold material from the outside of the case.) The question of solder certifications must be addressed prior to manufacture of flight units. NASA. requested a ship-in-place status as they have additional work they would like Westinghouse to perform. Overall this was a good learning experience for Magnetic Devices and we look forward to a continued relationship in the space arena.

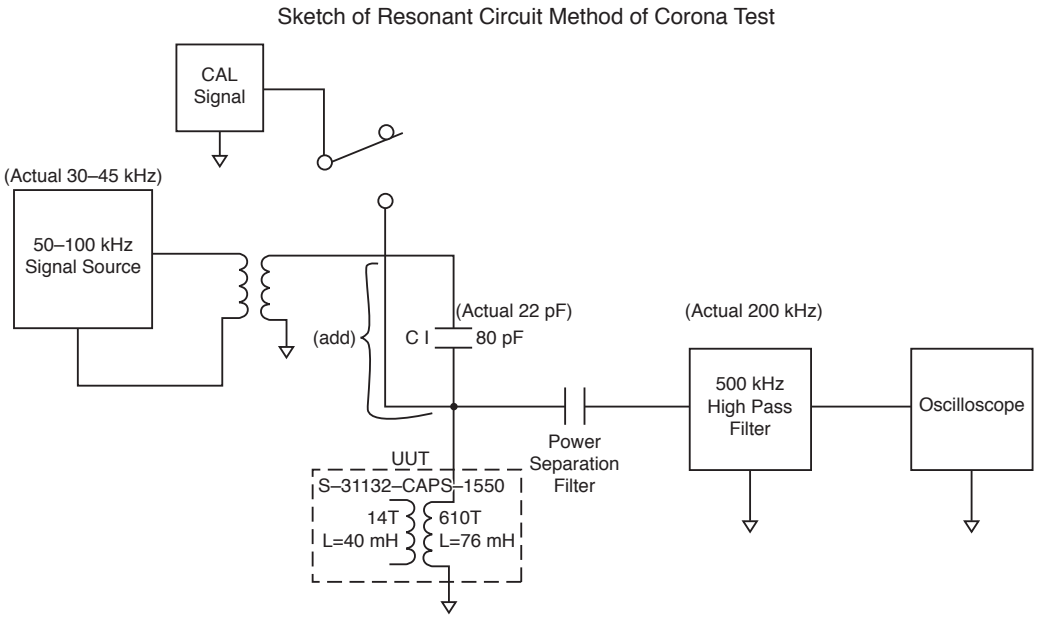
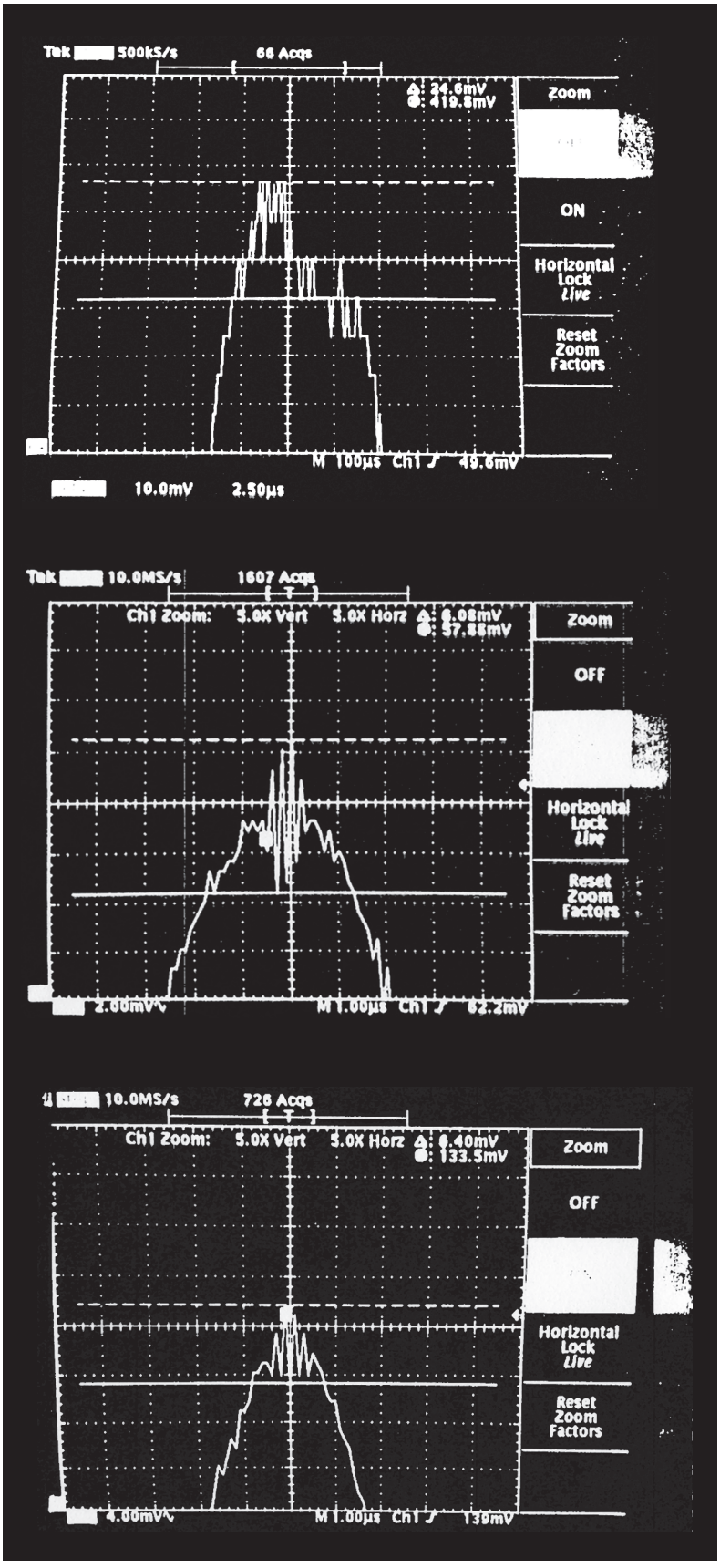


Figure 5.A.V.1. Resonant circuit method of corona test.



First unit with secondary coil that was replaced.
Corona = 24.6 mV

Figure 5.A.V.2

Second unit.
Corona = 6.08 mV

Figure 5.A.V.3

New secondary on first unit.
Corona = 6.40 mV

Figure 5.A.V.4

Chapter 6. Electrostatic Field Analysis

I. Physics and Mathematics Background:

One may analytically calculate the electric fields due to high voltage differences between ground and high voltage terminals. This can be for parts of instruments or within high voltage power supplies. If the geometry of the terminals or electrodes is simple, such as cylinders, spheres or parallel planes, then formulas exist for algebraic calculations. Even for more complicated configurations there are expressions such as the Table 2.2 of Chapter 2, which gives the *Maximum* field strength at the surface of the electrodes and perpendicular to them in direction. Electric fields are the gradients of the equipotential lines and are perpendicular to them, everywhere.

If, however, the shape of the electrodes is complex and accuracy is required, then a computer analysis of the entire space between and around the electrodes is indicated. The geometry of the electrodes can be 2-dimensional, of infinite extent in the third, or it can be a 3-dimensional solid of revolution, generated by revolving an *x*-*y* cross-section about the *y*-axis. For computer analysis of electric fields, the so-called finite element method is best suited. This is implemented in the well known, proprietary MSC/NASTRAN computer program (McNeil Schwendler/NASA Structural Analysis). It was developed under the direction of Dr. William Case during his years at NASA Goddard Space Flight Center, and it contains a Heat-Flow portion. It is the NASTRAN Thermal Analyzer (NTA) portion of the program which is of interest here. This is because the steady state differential equations governing the physics of thermal gradients and of voltage gradients, are entirely analogous in mathematical form. Also, the ratio of potential gradients perpendicular to the boundary in adjacent insulating materials is inversely proportional to the ratio of dielectric constants. Similarly, the ratio of temperature gradients in adjacent materials is inversely proportional to the ratio of thermal conductivities. So dielectric constant or rather, permittivity of an insulating material is analogous to thermal conductivity (Table 6.1(a)).

If the dielectric material also has appreciable electric conductivity, then the steady state electric field distribution in adjacent different materials is determined by the fact that the electric conductivity is analogous to thermal conductivity; then use the third part of Table 6.1(a).

Heat: For the *steady-state* solution of iso-thermal lines, LaPlace equation is

$$K\left(\frac{\partial^2}{\partial x^2}+\frac{\partial^2}{\partial y^2}+\frac{\partial^2}{\partial z^2}\right)T+\underline{Q}=0,$$

where

T = temperature in °K

$\underline{Q}$ = heat/second or joules/second generated per m^3 = W/m^3

K = thermal conductivity in $\frac{J/m^2}{s\ °C/m} = \frac{W}{°C\ m}$

$\frac{1}{K} \cdot \underline{Q} = °C/m^2$

Electrostatics: For the *steady-state* solution of equipotential lines, LaPlace's equation is, if electric conductivity is zero:

$$\varepsilon\left(\frac{\partial^2}{\partial x^2}+\frac{\partial^2}{\partial y^2}+\frac{\partial^2}{\partial z^2}\right)V+\rho=0,$$

where

V= voltage in volts;

$\varepsilon = \kappa_e \varepsilon_0$, where κ_e= dielectric constant, ε_0= permittivity of empty space, and ε = permittivity of the dielectric in farads per meter (F/m), which is *coulombs per volt meter;* and

ρ= space charge density in *coulombs per cubic meter* (coulombs/m^3), if "doping" is used.

Thus, $\rho/\varepsilon = V/m^{2.}$

If answers for the field strength, E, are finally desired in volts per millimeter (mm) (millimeter are more the dimensions of apparatus and instruments), then ρ has to be in coulombs per cubic millimeter and ε_0 has to be changed from the MKS value of 8.9 x 10^{-12} F/m, to 8.9 x 10^{-15} F/mm. The analogies are summarized in Tables 6.1a and 6.1b. Different authors use different symbols for physical quantities.

TABLE 6.1a. Electrical/Thermal analogy for steady-state analysis.

Thermal	Electric (if electric conductivity = 0)
T = Temperature, i.e., °K	V = Voltage, i.e., volts
K = Conductivity, i.e., $\frac{W}{mm\ °K}$	$\underline{\varepsilon}$ = Permitivity, i.e., F/mm = $\kappa_e\varepsilon_0 = \kappa_e$ x 8.9 x 10^{-15} F/mm
$\underline{Q}$ = Heat Source Density	$\underline{\rho}$ = Charge Source Density or Space Charge, i.e., $\frac{C}{mm^3}$
i.e., $\frac{W}{mm^3}$	κ_e = Dielectric Constant
$K\nabla^2 T + \underline{Q} = 0$	$\varepsilon \nabla^2 V + \rho = 0$
∇T = Thermal gradient	$\nabla V = -E$, the Electric Field

Electrical (with conductivity not =0)

V=Voltage, i.e., volts

σ=Electric conductivity (i.e., 1/Ωm)

$\sigma\nabla^2 V = -d\rho/dt$

(Use SOL 59 when right-hand side is non-zero. Use HEAT SOL 24 for steady state current flow.)

TABLE 6.1b. Analogous thermal and electrical parameters, adapted from Ref. [10].

MSC/NASTRAN Name	Thermal Symbol	Electrostatic Symbol	Current Flow Symbol
Temperature	T	V	V
Conductivity	K	ε	σ
Temperature Gradient	∇T	–E	–E
Heat Flux	K∇T	D	J
Internal Heat Generation	$\underline{q}$	ρ	dρ/dt
Total Heat Flow	Q	Q_e	I

II. EXAMPLE: From a report by Sandra Irish, Code 542 GSFC, Nov. 1987.

To illustrate the actual steps to do a computer analysis of an electric field, the modeling of the germanium detector for the Gamma Ray Spectrometer (GRS) that flew on the Mars Observer is shown here. The ultimate objective of this particular analysis was to find the optimum shape and "doping" of the germanium (Ge) detector to achieve a uniform field within the germanium itself. The germanium is a solid cylinder about 56 mm long with a center hole that extends about 7/8 down the length of the detector. The outer radius is 29 mm and the inner radius of the hole is 8 mm, as shown in Figure 6.1(b). It is first modeled as a 2-dimensional solid, (for practice; does *not* give the correct answers), and then is modeled as a three-dimensional solid of revolution as required by the actual geometry. Then the "doping" is added. This illustrates the progressive complexity of the modeling steps.

A. ANALYSIS

The analysis was divided into the following two parts: the two-dimensional (2-D) detector model and the three-dimensional (3-D) detector model. The 2-D model assumed the detector to be an infinitely long solid bar as shown in Figure 6.1(a). The 3-D model, shown in Figure 6.1(b), represents a solid cylinder depicting the actual GRS detector. The analysis was performed on the 2-D model first to obtain a better understanding of the analysis procedure required prior to applying this procedure to the more complex 3-D detector model. Also, the cross-section of the infinite bar model and the cross-section of the solid cylindrical model were the same, which simplified the development of the 3-D model.

Figure 6.2 shows a flow chart of the procedure used in the analysis to obtain a color graphics display of the voltage and field strength distributions for the detector. Once the basic geometry of the detector was known, a model of the detector was developed using PATRAN, a computer program which creates detailed finite element models efficiently. Various modeling checks were performed on the elements to assure that accurate results would be obtained.

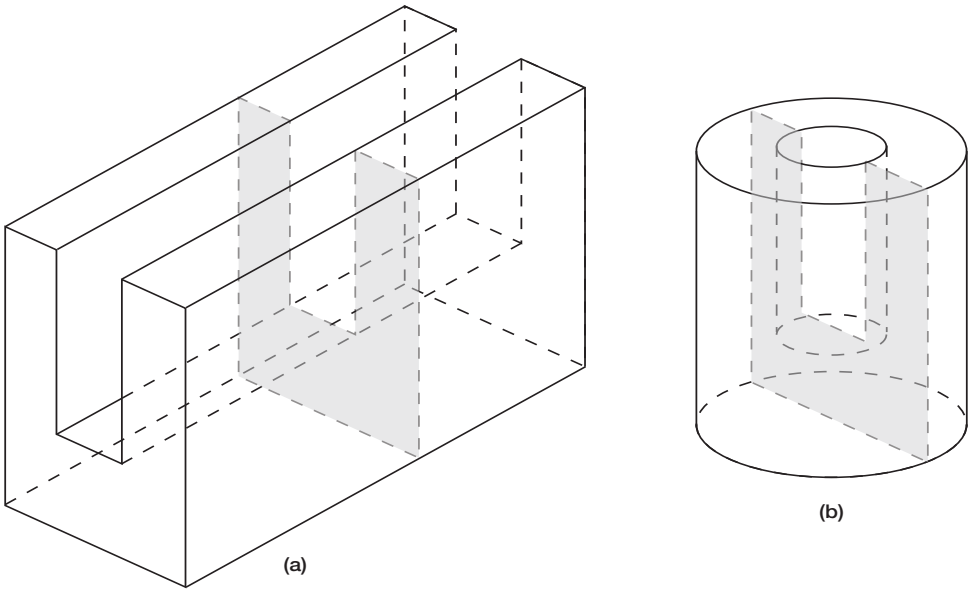


Figure 6.1. 2-D and 3-D model representation.

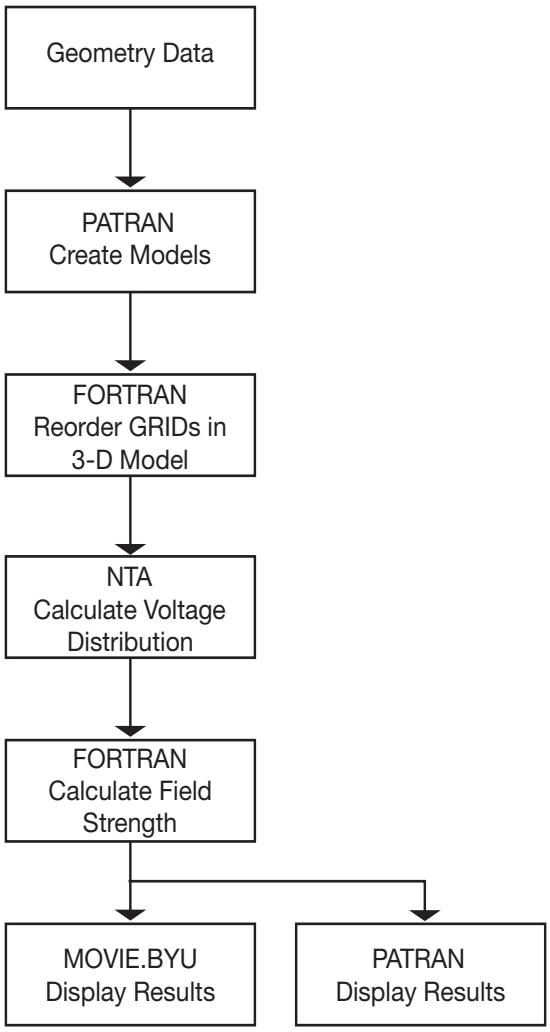


Figure 6.2. Analysis procedure.

In the 3-D model, a FORTRAN program was developed to reorder the grid points since the solid axisymmetric elements used in the model required a specific grid order format. Parameters, such as voltage boundary conditions and charge density of the material, were then added to the finite element model to produce a model ready for submittal to the NASTRAN Thermal Analyzer (NTA). The NTA was then used to perform a linear steady-state analysis with HEAT SOL 24, NASTRAN HEAT = 1. This produced a voltage value for each grid point in the model and the voltage gradients for each element in the model. A FORTRAN program was developed to extract the voltage gradient data from the NTA output file and to produce the field strength distribution for the model. The field strength values were calculated by obtaining the root sum of the squares of the voltage gradients.

The preferred method of reviewing the results from the analysis is by color graphics rather than scanning tables of numbers. Therefore, the output from the FORTRAN program was organized into a format that was read by a MOVIE. BYU, a computer program which displays results using color graphics. In addition, the Patran program can be used to display the results. Color graphics plots of the voltage and field strength distributions were then created.

Two-Dimensional Detector Model

A MSC/NASTRAN model was developed for a cross-section of the infinitely long bar. Because of the symmetric geometry of the cross-section and the symmetric loading that would be applied, only half of the section was modeled. Figure 6.3 shows a plot of the 2-D NASTRAN model. The 2-D model contained 339 grid points and 296 CQUAD4 elements. A voltage boundary condition of 0.0 V at the inner edge and –4000.0 V on the outer edge was applied to the model (refer to Fig. 6.4). The voltage distribution for the 2-D geometry was then calculated by the NTA. Figure 6.5 shows a color graphics plot of the equipotential lines, lines of constant voltage, calculated for the 2-D model. Figure 6.5 shows a fairly uniform distribution near the open end of the detector and shows that the lines become closer together and less uniform at the closed end. A field strength value for each element was then calculated from the voltage gradients. Figure 6.6 shows the field lines, lines perpendicular to the equipotential lines, for the 2-D model. Also, field strength values are labeled at various locations. The highest field strength of 688.7 V/mm was found at the lower inner corner of the detector (where the equipotential lines are closest together), and the lowest field strength of 17.8 V/mm was located at the outer bottom corner of the detector (where the equipotential lines are farthest apart).

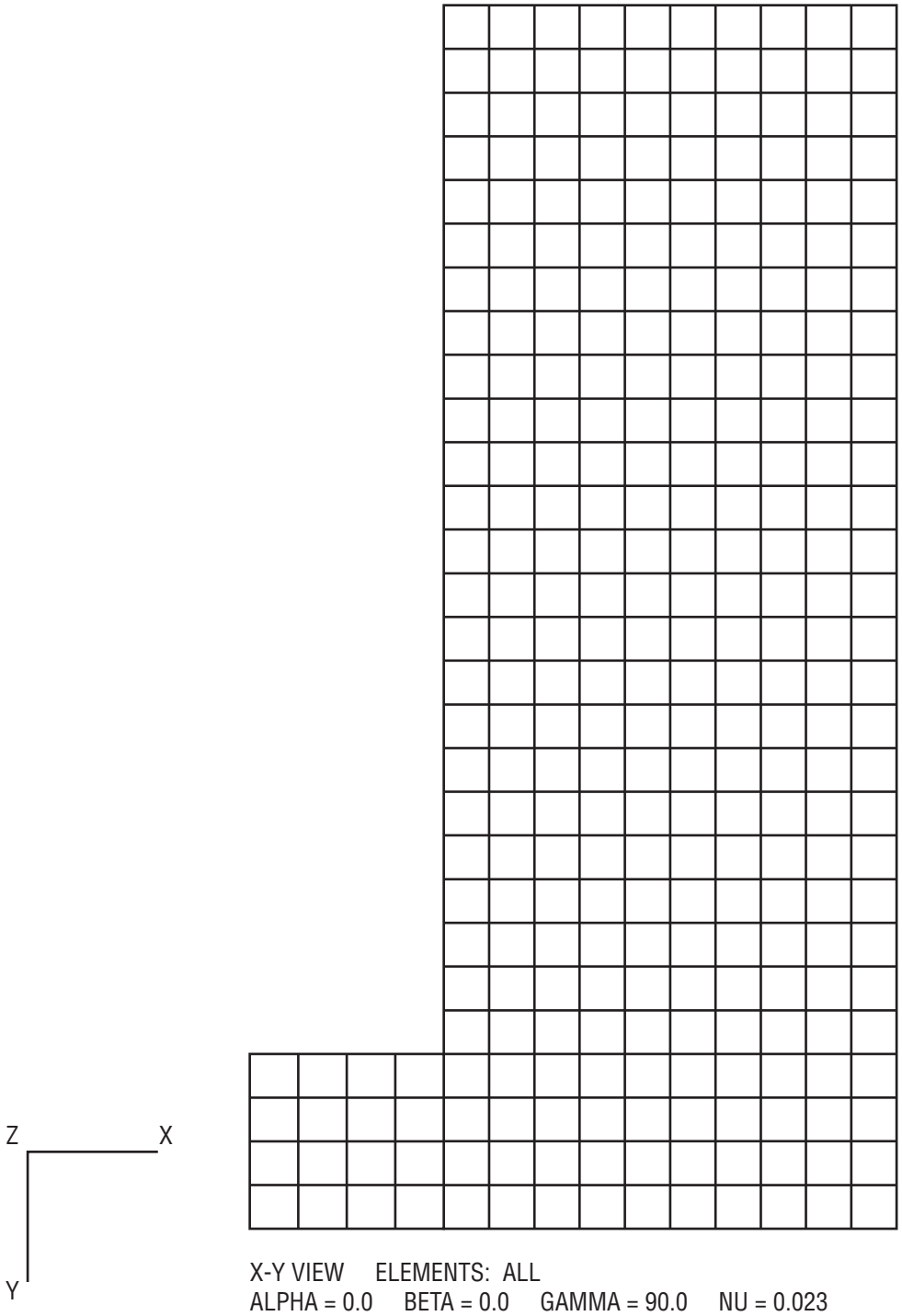


Figure 6.3. 2-D Model

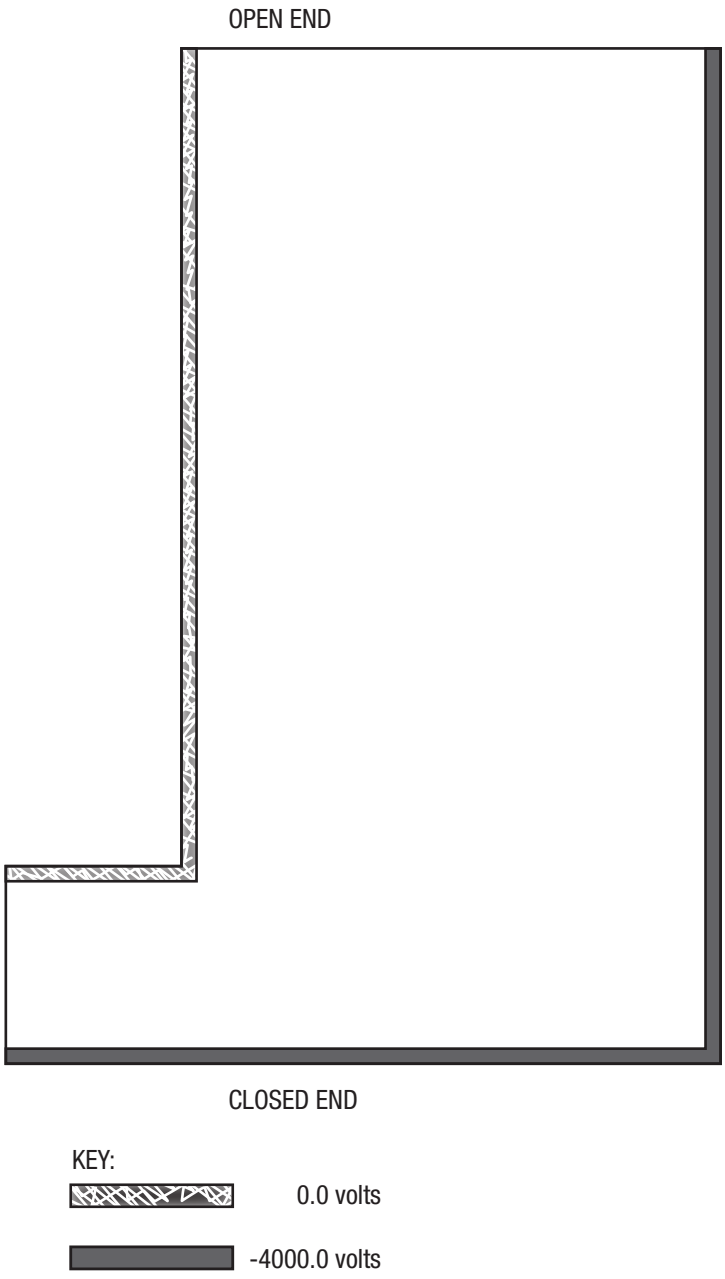


Figure 6.4. GRS boundary conditions.

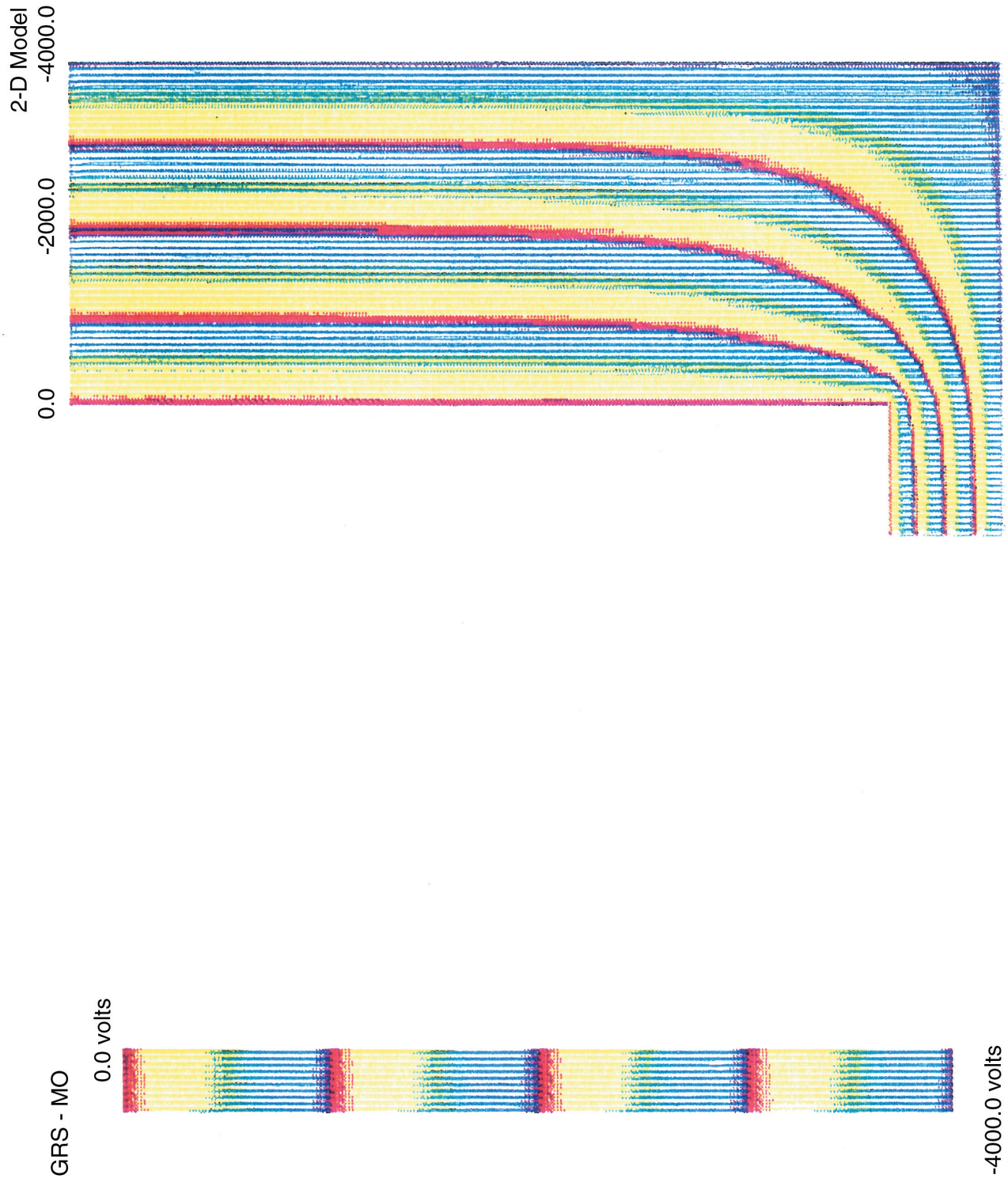


Figure 6.5. Equipotential lines for the 2-D model.

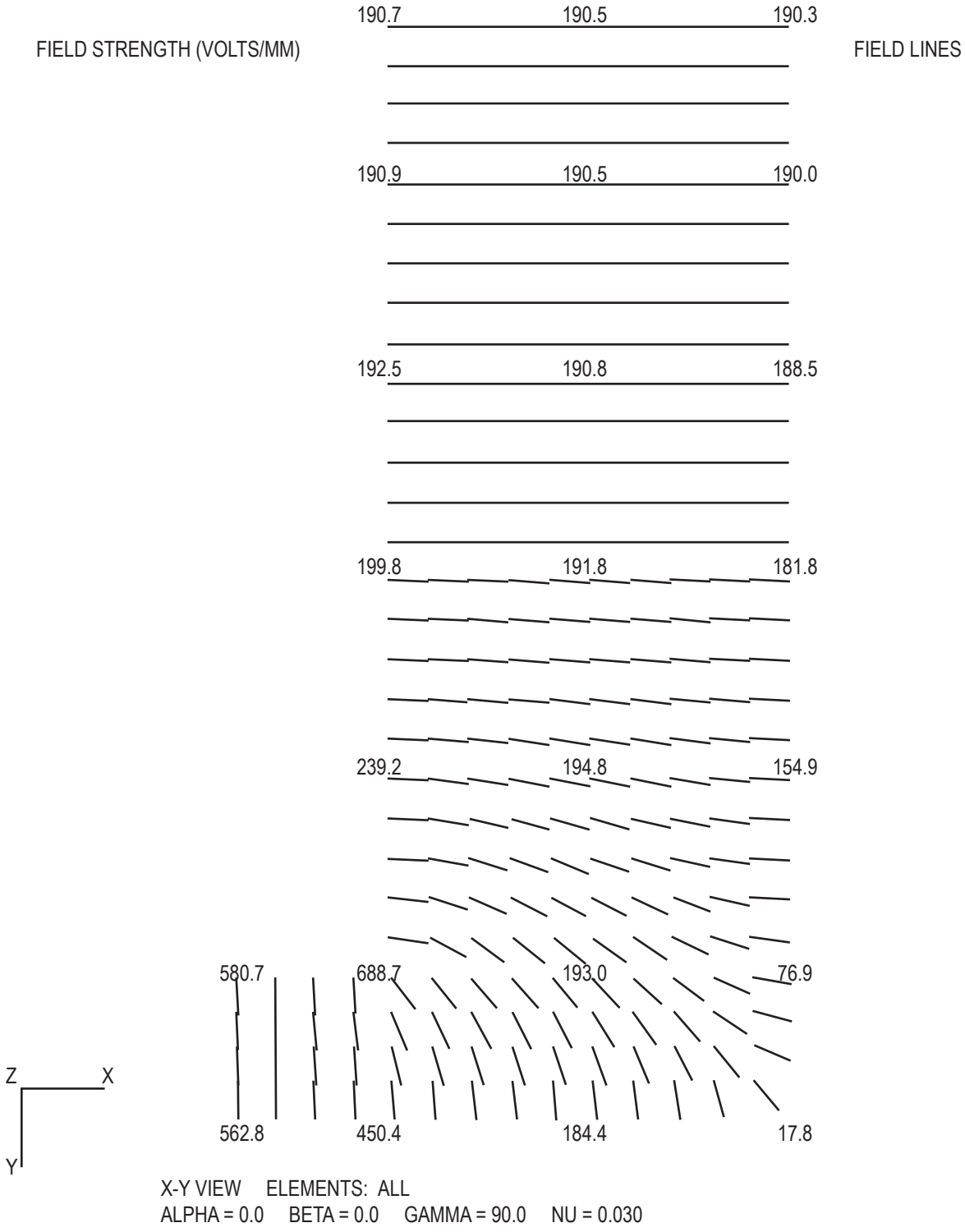


Figure 6.6. Field lines of 2-dimensional model.

Three-Dimensional Detector Model

The symetric geometry of the germanium detector made it possible to use MSC/NASTRAN's axisymmetric elements to create an appropriate 3-D finite element model. The CTRAPRG elements allows the user to model a trapezoidal cross-section in the *x*-*z* plane. This cross-section is rotated about the *z*-axis to create a solid trapezoidal ring. In this manner, the concept for converting the already existing 2-D GRS detector model to a 3-D model was relatively simple; the CQUAD4 elements were converted to CTRAPRG elements.

However, there are a few restrictions on how the CTRAPRG can be specified. The grid points must be ordered counterclockwise, starting from the lower left. Also, all grid points must lie about the +*x* axis and to the right of the +*z* axis. It was therefore necessary to pay close attention to the grid point connectivity, and use FORTRAN programs to manipulate both the connectivity and the grid point locations.

Preliminary results from the first 3-D model indicated that there were large electrical field strength gradients in the *x*-direction. Because the field strength of two adjacent elements differed as much as 20%, a finer mesh was developed, increasing the model size from 296 to 1776 elements. This fine-mesh model is shown in Fig. 6.7. Several sets of boundary conditions were applied to the model, with the final analysis configuration incorporating a voltage drop across the detector of –4000 V (Fig. 6.4).

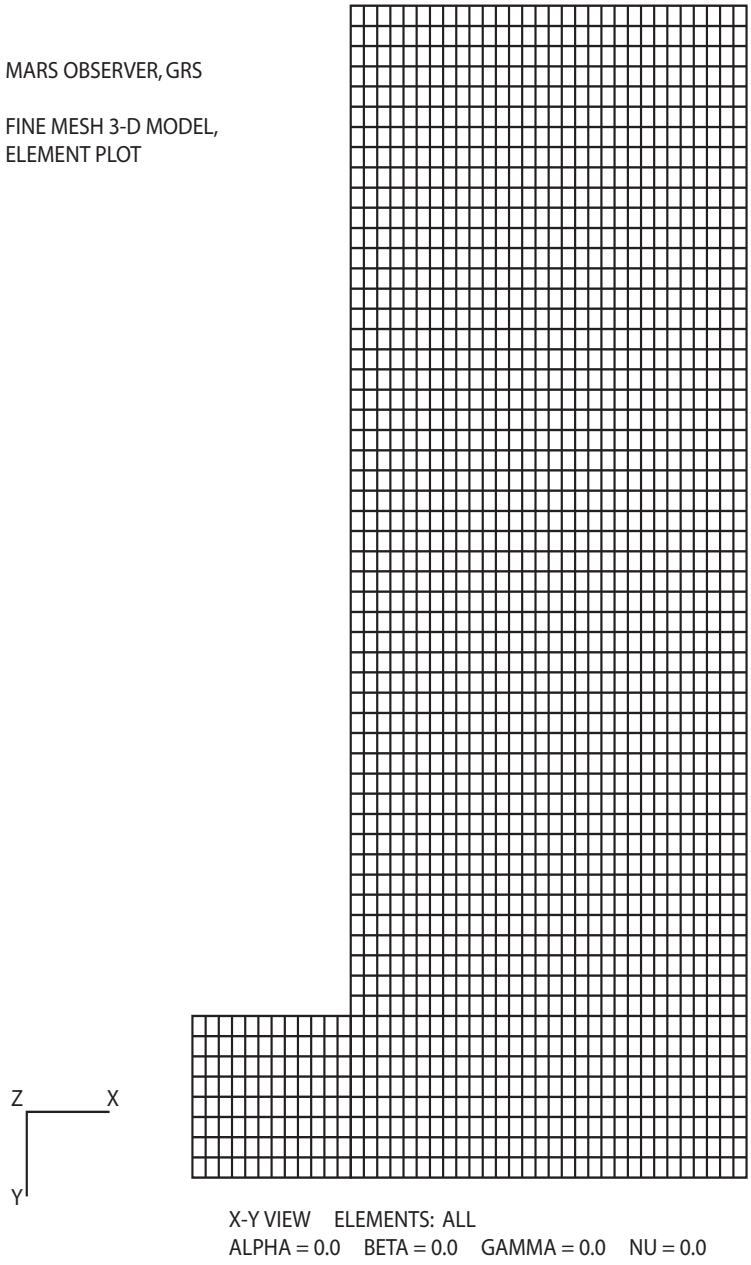


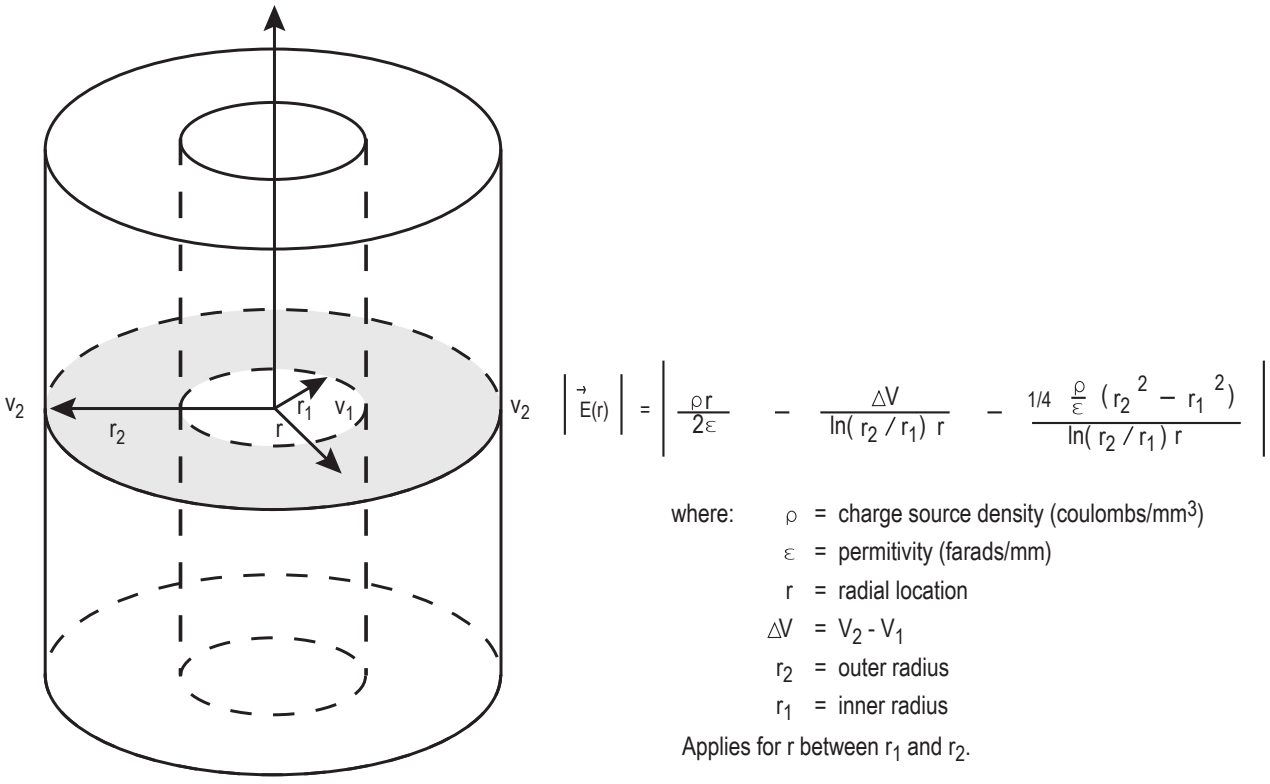
Figure 6.7. Fine mesh 3-D model, element plot.

In order to determine whether the analysis was producing reasonable results, the computed field strength values were compared to values calculated from the theoretical equation in polar coordinates, for the field strength in an infinitely long cylinder (Fig. 6.8). A few specific locations near the open end of the detector were chosen for the NTA to theory comparison because only the upper portion of the detector can be approximated by this theory. The comparison is given in Table 6.2, which shows that the NTA results were within 1% of the theory. Also, a plot of the equipotential lines is presented in Fig. 6.9. These lines were not uniformly distributed as the lines for the 2-D model (Fig. 6.5), but instead were concentrated near the inner edge of the detector, as one would expect for cylindrical geometry, from basic field theory, due to the Inverse Square Law.

Addition of Charge Density of the Material

Impurities in a germanium crystal lattice cause changes in the electric field, with the effective result being the addition of volumetric charge sources. This is often a desired effect which the detector designer can use to his advantage through doping (controlled addition of impurities). The charge density distribution in the GRS detector varied linearly along the *z*-axis, from 1.6 x 10^{-12} C/mm^3 at the open end to 2.4 x 10^{-12} C/mm^3 at the closed end. This was modeled in the NTA by using the QVOL thermal load card, which added charge sources on every element.

The doped model was tested with the boundary conditions given in Fig. 6.4, and the electrical field strength results agreed with the theory given in Fig. 6.8, with an error of less than 2%. Note that for this case, the doping was included in the theoretical calculation and was a function of vertical (*z*) position. The results of the comparison between NASTRAN and theory are summarized in Table 6.3, and the equipotential lines and field strength are displayed graphically in Figs. 6.10 and 6.11, respectively. A maximum field strength of 935.3 V/mm occurred at the inside lower corner, and a minimum of 21.4 V/mm occurred at the outside lower corner.



$$\left|\vec{E}(r)\right| = \left| \frac{\rho r}{2\varepsilon} - \frac{\Delta V}{\ln(r_2/r_1)\, r} - \frac{1/4\ \frac{\rho}{\varepsilon}\,(r_2^{\,2} - r_1^{\,2})}{\ln(r_2/r_1)\, r} \right|$$

where:
- ρ = charge source density (coulombs/mm^3)
- ε = permitivity (farads/mm)
- r = radial location
- ΔV = $V_2 - V_1$
- r_2 = outer radius
- r_1 = inner radius

Applies for r between r_1 and r_2.

Figure 6.8 Field strength in an infinitely long cylinder, from Ref. [11].

Table 6.2. GRS field strength. Voltage drop = -4000 V. No doping.

Radius mm	*E (NASTRAN) V/mm	**E (Theory) V/mm	%diff
10	310.1	310.6	–0.16
17	181.7	182.7	–0.55
29	107.0	107.1	–0.09

* Computed as an average of four elements near r, at a depth of 20 mm

** $E(r) = \left| E(r) \right|$

$$= \left| \frac{\Delta V}{\ln(r_2 / r_1) r} \right|$$

** J. Llacer, "Planar & Coaxial High Purity Germanium Radiation Detectors," *Nucl. Instr. Methods*, **98**(2), North Holland Publ., Jan. 1972.

Table 6.3. GRS field strength with doping. (Voltage drop of –4000.0 V, and doping was applied with linear variation along axis of symmetry.

Radius mm	*E (NASTRAN) V/mm	**E (Theory) V/mm	%diff
10	179.0	176.8	1.2
17	178.1	177.8	0.2
29	227.0	230.5	-1.5

*Computed as an average of four elements near r, at a depth of 20 mm

** $$E(r) = \left| \frac{\rho r}{2\varepsilon} - \frac{\Delta V}{\ln(r_2 / r_1) r} - \frac{\frac{1}{4}\rho(r_2^2 - r_1^2)}{\varepsilon \ln(r_2 / r_1) r} \right|$$

where ρ = is the charge density at a depth of 20mm
ε = permittivity (farads/mm)
r = radial location
$\Delta V = V_2 - V_1$
r_2 = outer radius
r_1 = inner radius

** J. Llacer, "Planar & Coaxial High Purity Germanium Radiation Detectors," *Nucl. Instr. Methods*, **98**(2), Jan. 1972.

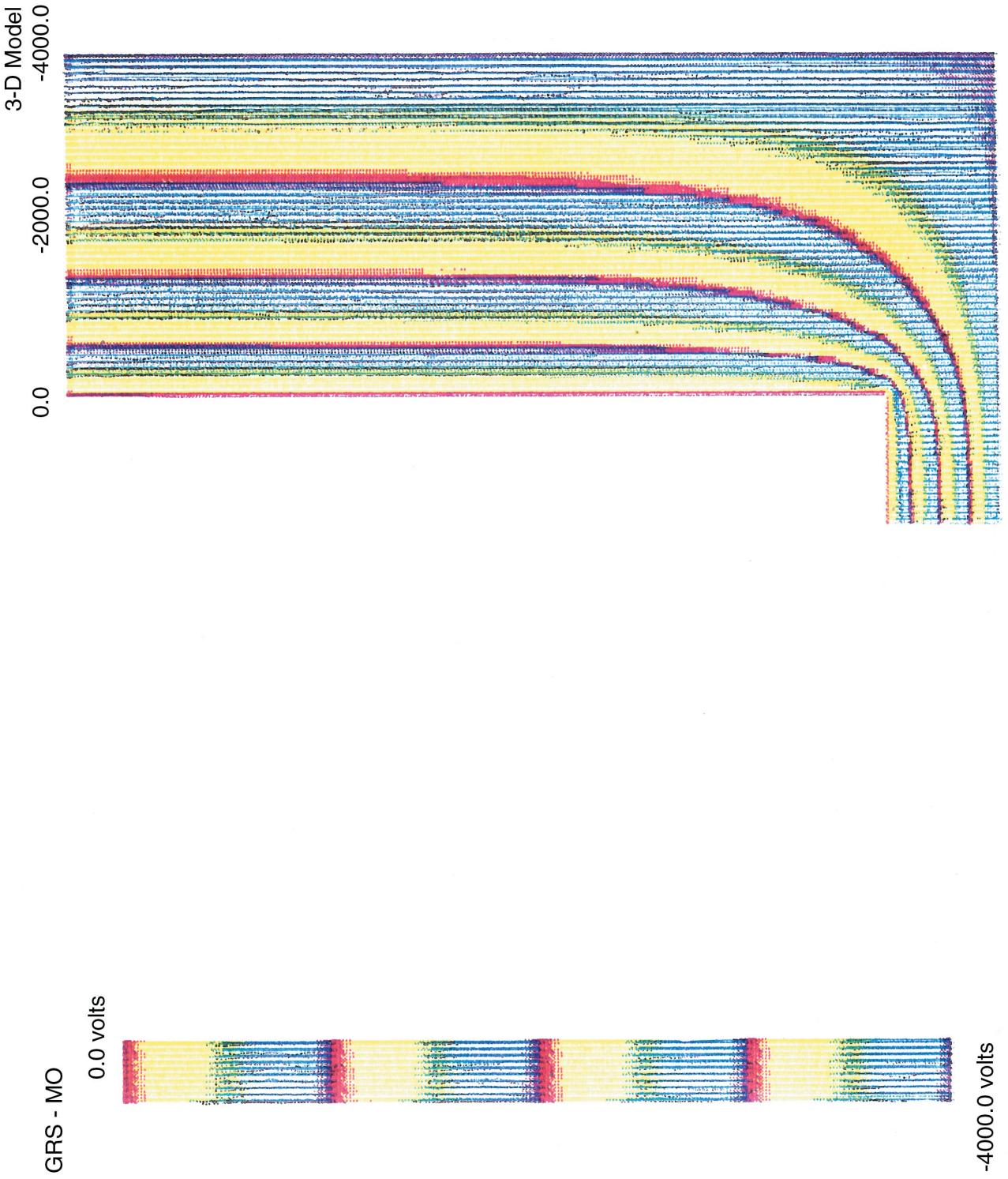


Figure 6.9. Equipotential lines for 3-D model.

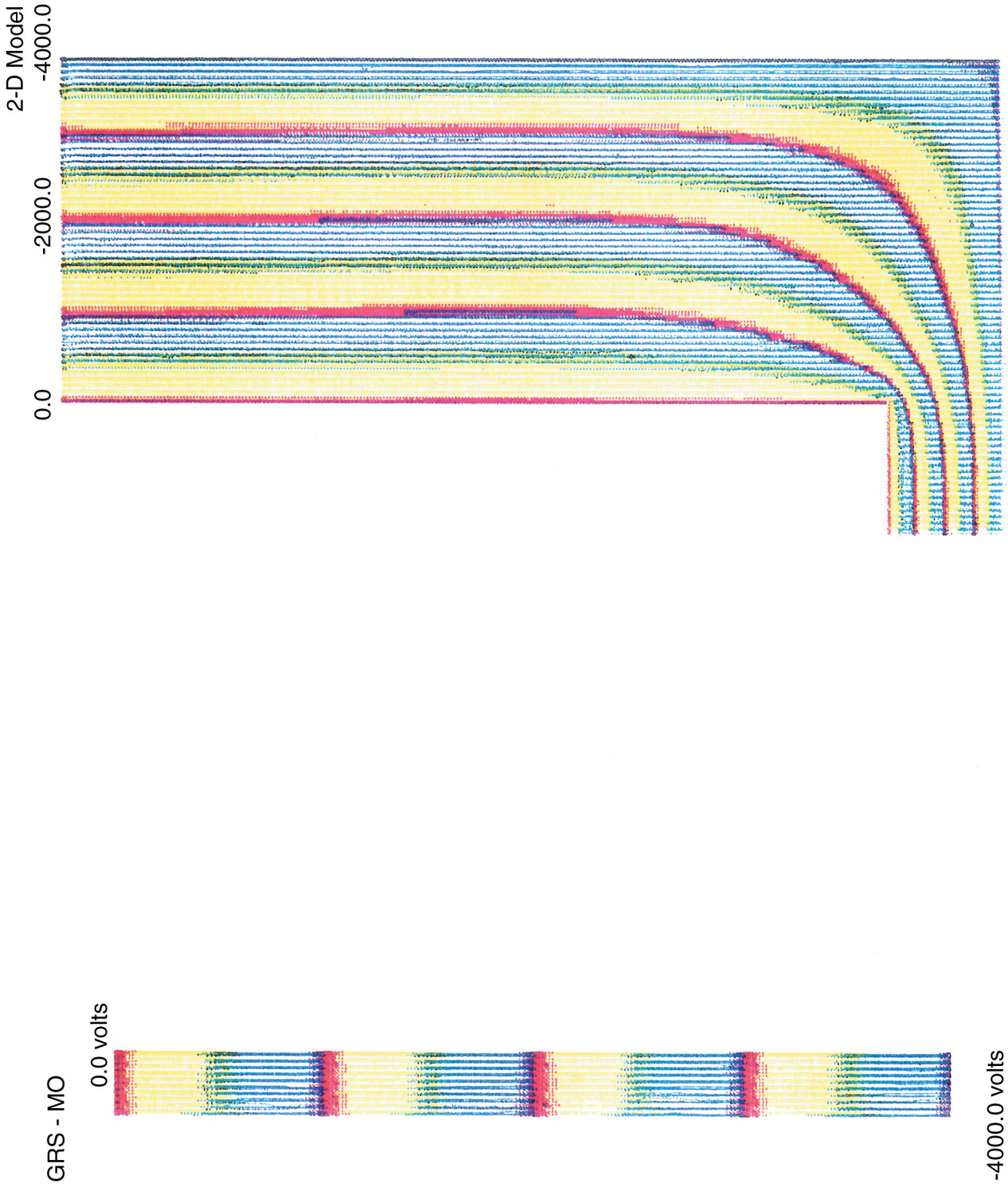


Figure 6.10. Equipotential lines with doping.

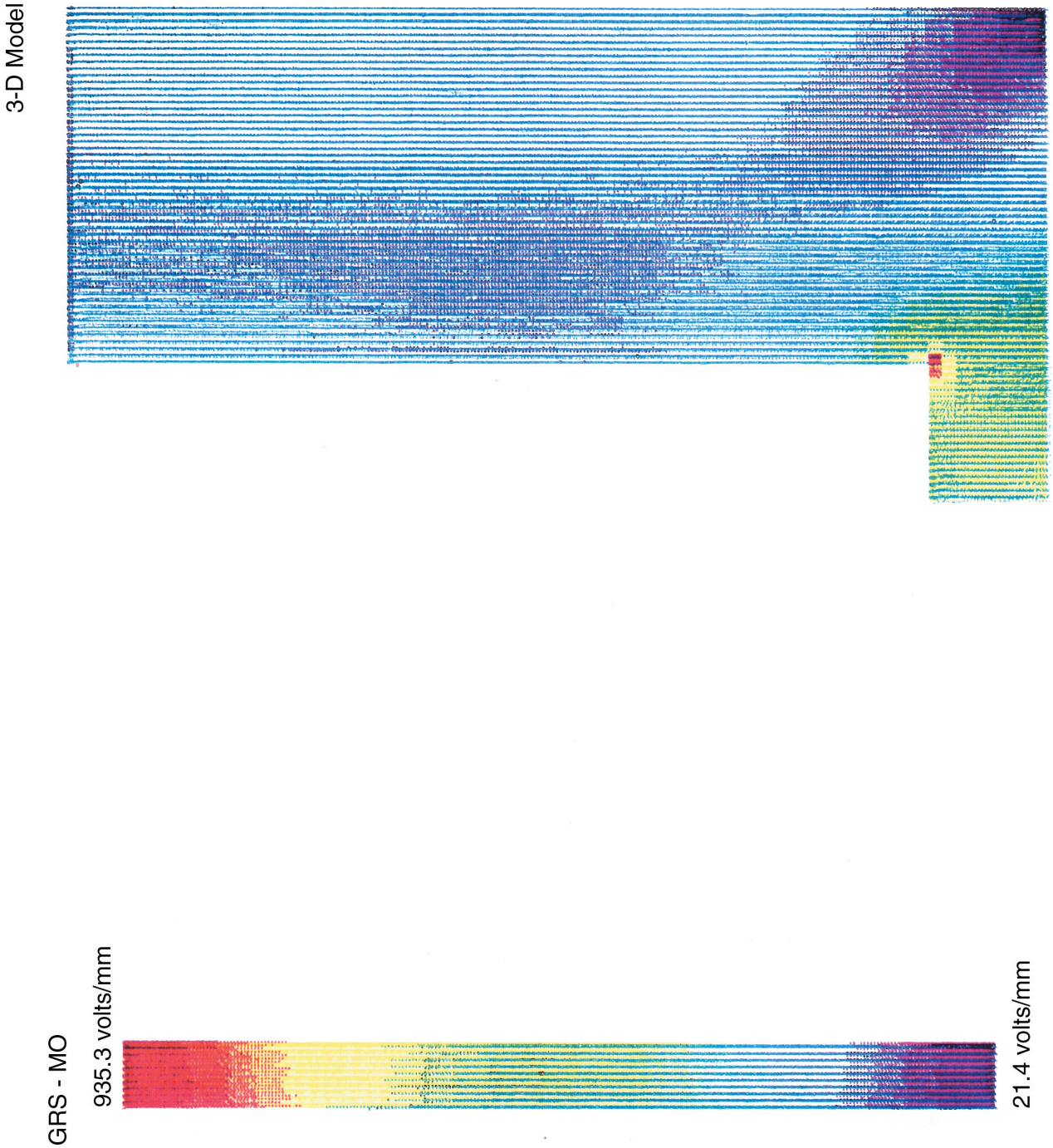


Figure 6.11. Field strength distribution with doping.

Geometry and Boundary Changes

Several refinements were made to the original detector model geometry to more closely match the actual design, and to provide a feel for how geometry changes would affect the electric field strength and voltage distributions in the detector. In detector design, sharp edges are sometimes rounded to reduce localized areas of high field strength and remove areas of low strength. In the GRS detector, the two outside corners and the lower inside corner were rounded slightly. This rounding was accomplished in the model by manually removing some elements on the outside corners, adding a elements on the inside corner, and changing the shape of the elements that became the new edges. This required the replacement of several CTRAPRG elements by CTRIARG elements. The CTRIARG is a solid axisymmetric ring similar to the CTRAPRG element, but it has a triangular cross section instead of a trapezoidal one. The restrictions discussed in an earlier section also apply to the CTRIARG specification. .The shape of the smoothed corners was approximately circular, with radii of 3.5 mm on the lower outside corner, 4.0 mm on the inside corner, and 4.1 mm on the upper outside corner. Figure 6.12 shows the rounded model geometry.

Two cases of the rounded model were analyzed. First, a model with rounding on only the inside and lower outside corners was used with the original boundary conditions (Fig. 6.4). This resulted in only slight changes in the maximum and minimum field strength values compared to the fine-mesh 3-D model. Then, a model with all three corners rounded was used with the outside boundary condition of –4000 V extended over the top of the model 9.8 mm from the outside edge. The inside edge remained at 0 V. Doping, as discussed previously, was included in this analysis. Figs. 6.13 and 6.14 show the resulting equipotential lines and field strength distributions in the detector.

One other variation of the original fine-mesh model was tested. The hole depth was changed from 49 mm to 31.65 mm to determine how much this type of geometry change would lower the electrical field strength. The additional elements needed to close up the earlier deeper hole increased the model size to 1980 elements. This model is shown in Fig. 6.15. The original boundary conditions (Fig. 6.4) and doping were used for this analysis. The maximum field strength still occurred at the lower inside corner, but was reduced to 389.0 V/mm, or by about 58%. At the same time, the field strength distribution was more uniform. A graphic representation of the field strength distribution is given in Fig. 6.16.

III. Comments

Somewhat abbreviated versions of the computer program are available for desktop computers. An example is MAGGIE by McNeil-Schwendler Company. This can be run on IBM compatible desktop computers. Even so, the data-inputting and manipulations are rather intricate and time-consuming. Also, most recently, programs called MAXWELL 2D and MAXWELL 3D, by ANSOFT Co. are available. Similar Electro-Magnetic Software can be obtained from ANSYS or INFOLYDICA or MAGSOFT.

For many purposes, use of the Chapter 2, Table 2.2 formulae to obtain approximate *maximum* field strengths at the surfaces of high voltage terminals and bus wires within a given power supply, combined with an *estimate of average* field strengths as $\Delta V/d$ where d is the separation between a given terminal or wire and the nearest ground plane, is all that is needed. The average field strength everywhere should be kept below 50 V/mil.

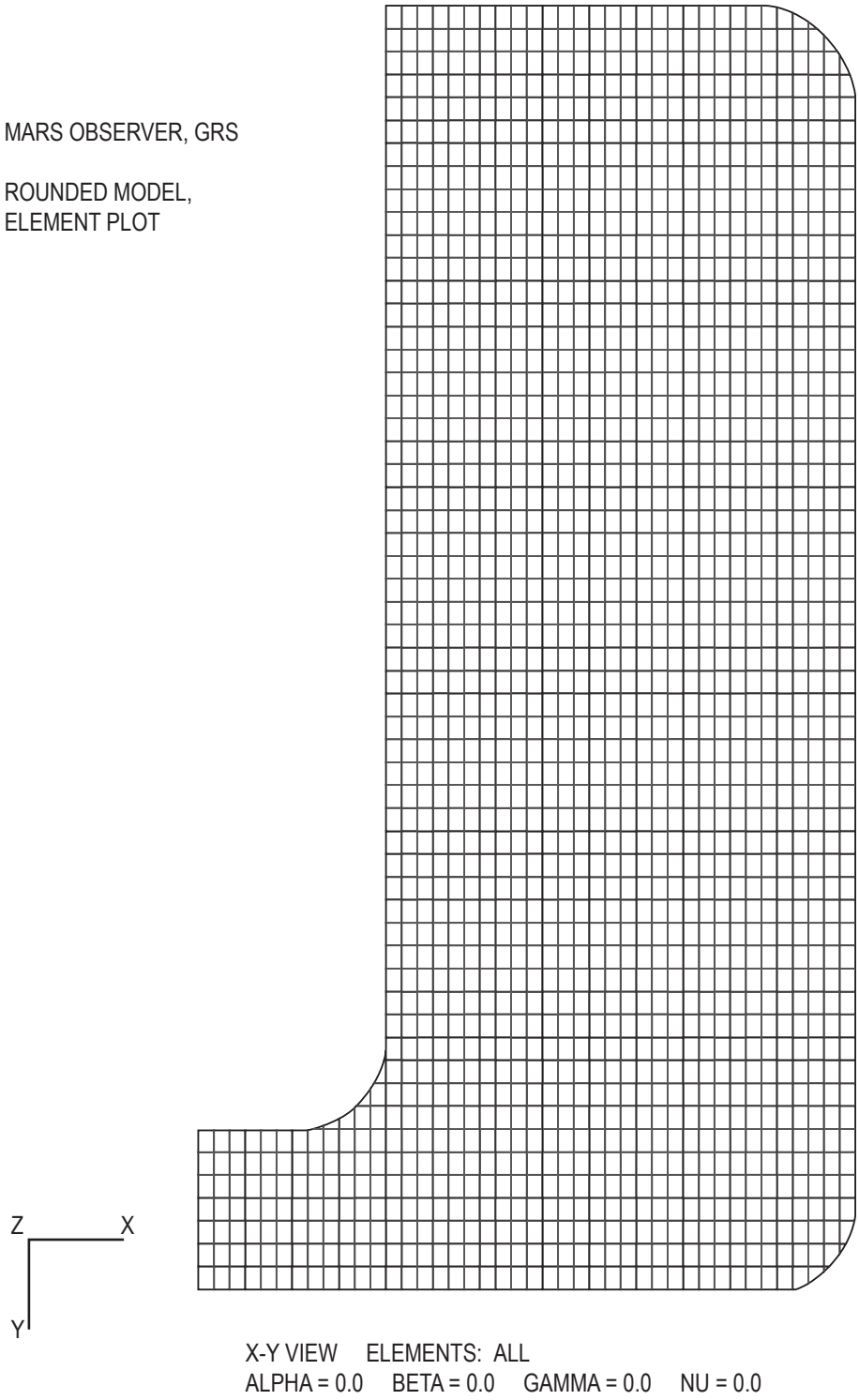


Figure 6.12. Rounded model, element plot.

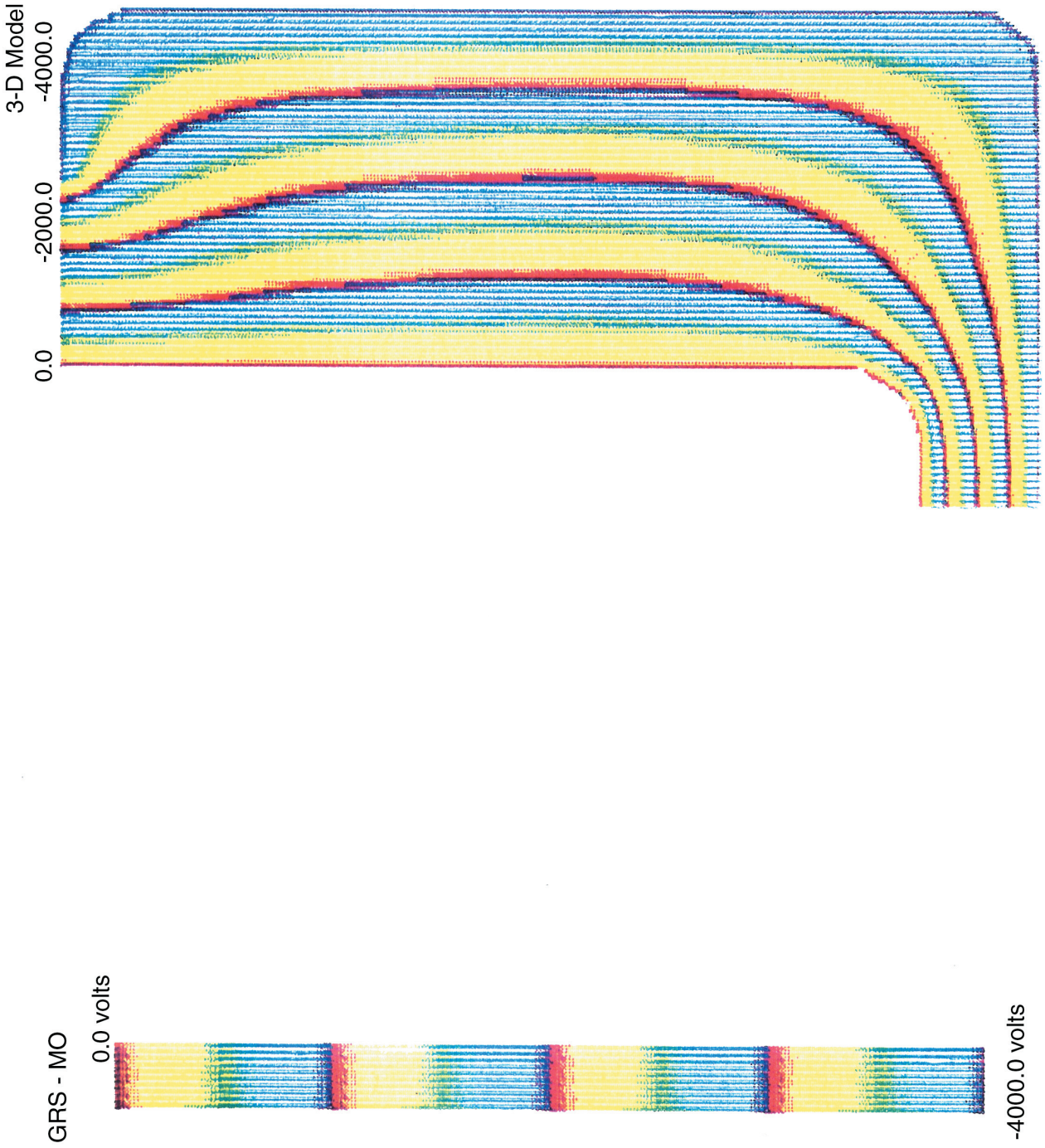


Figure 6.13. Equipotential lines for rounded model with doping.

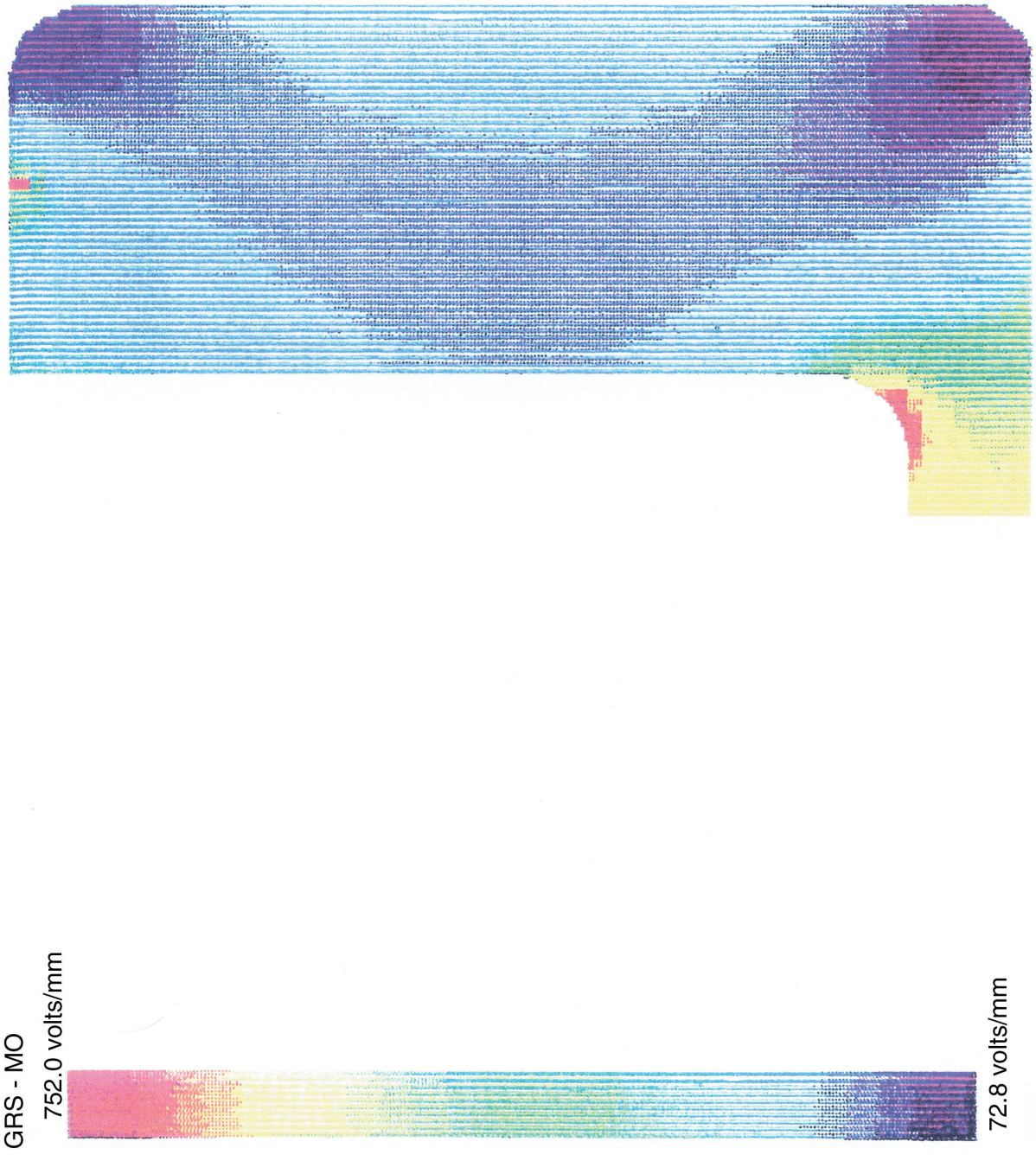


Figure 6.14. Field strength distribution for rounded model with doping.

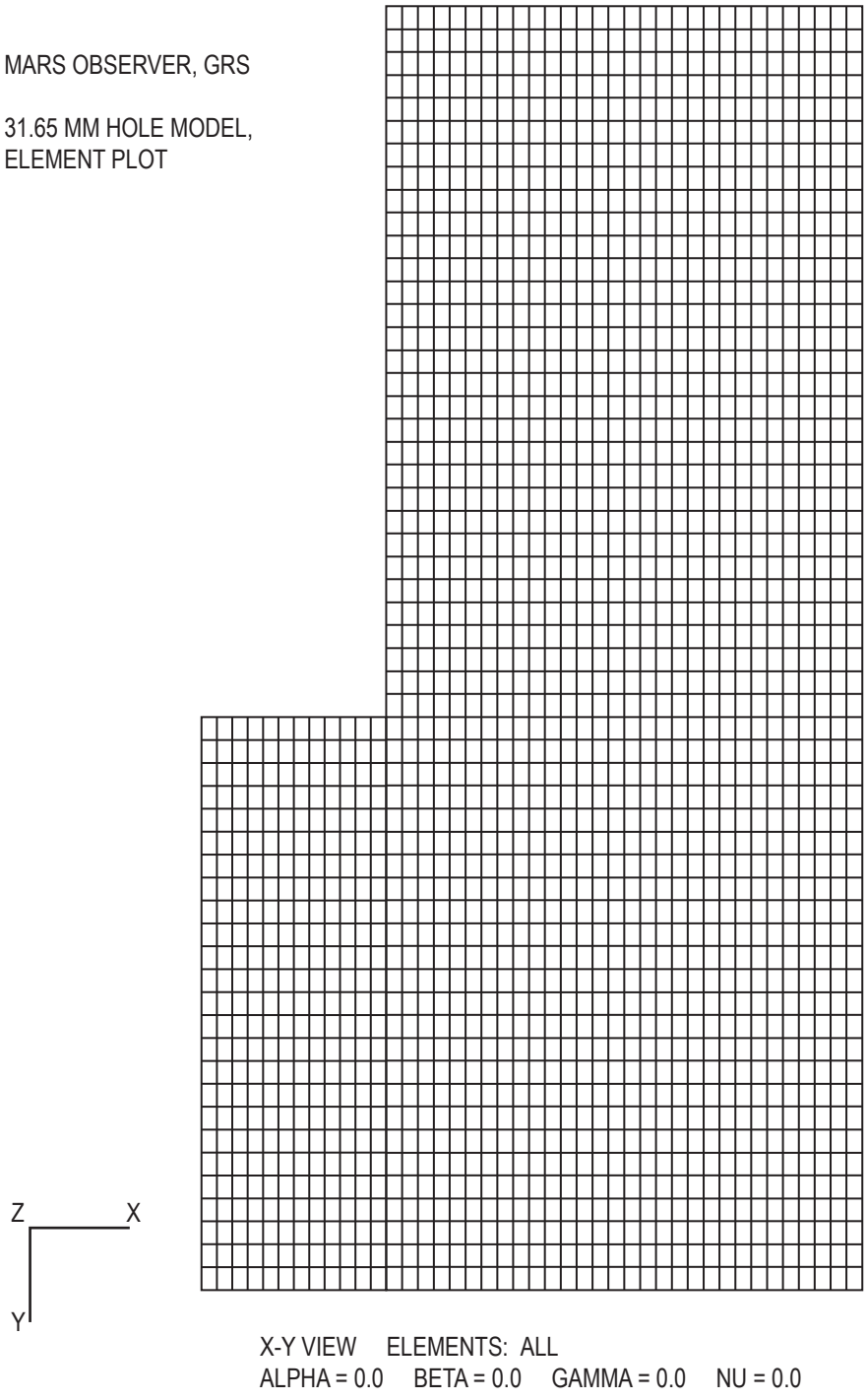


Figure 6.15. The 31.65 mm hole model, element plot.

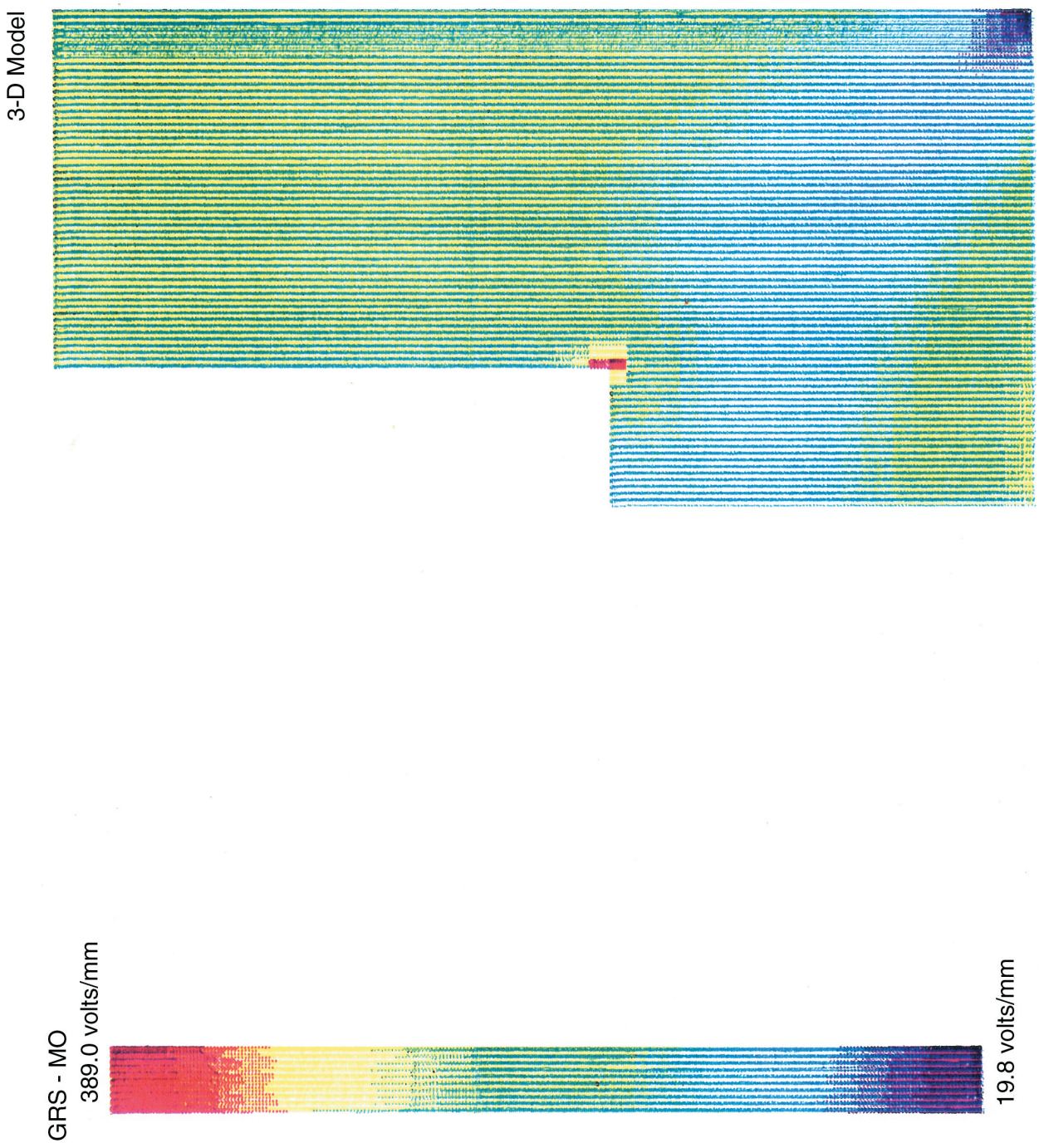


Figure 6.16. Field strength distribution for smaller hole and doping.

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Chapter 7. Design Examples of Successful High Voltage Power Supplies

Introduction

The creation of high voltage power supplies, or any other high voltage assembly or device falls, broadly speaking, into two stages:

(1) the electrical/electronic design, and
(2) lay-out/packaging/insulation build-up.

The two stages are, of course, intertwined, and both have to be kept in mind throughout the theoretical planning and the practical hardware fabrication. The emphasis of this book is mostly on stage (2), therefore, photographs and some comments on the manufacturing of several high voltage power supplies are presented. It is also deemed worthwhile to present circuit schematics and summaries of circuit analyses of one or two supplies. The latter is a concession to stage (1) mentioned above; however, a step-by-step development of *electronic* design is not intended to be done in this book.

Operational guidance for test and flight of each high voltage power supply is also very important. Therefore, a single example of one such set of instructions is included as an appendix to Chapter 7, for the ACD/GLAST High Voltage Bias Supplies (HVBS).

DESIGN EXAMPLE A

A –25 kV supply for the High Resolution Spectrograph (HRS) and Faint Object Spectrograph (FOS) of the Hubble Space Telescope Project by Joseph A. Gillis, GSFC. (Later adapted by Martin Marietta Co., of Denver, Colorado, and by Ball Brothers of Boulder, Colorado.)

Specification for a Digitally Controlled HVPS for the HRS Digicon

1. *Method of Control:* A ten bit digital word will control the voltage output of the device from 0 to –24 kV. This word may be presented to the supply either serially or in parallel, and in accordance with the interface provisions of the HST (Hubble Space Telescope) "Science Instruments to Control and Data Handling Subsystem Interface Requirements Document" (S-725-4). The eight least significant bits will control the supply's output from –18 kV to –24 kV to the specifications listed below, while the two most significant bits will permit a stepped turn-on from 0 to –18 kV with performance to specifications not being mandatory. Accuracy and linearity of the control word to output voltage function shall be ±1 LSB over the –18 to –24 kV range.

2. *Voltage Output:* 0 to –24 kV (Turn-on Procedure), –18 to –24 kV (Normal Operation)

3. *Voltage Regulation:* ±0.05% over line, constant load; that is ±9 V to ±12 V.

4. *Voltage Ripple:* ±1 V p-p

5 *Output Current:* 60 μA at 24 kV; this includes 40 μA load and 20 μA feedback.

6 *Input Voltage:* 19 V ±2%

7. *Input Power:* Less than 3 W

8. *Temperature Range:* 0°C to 40°C Operating; –20°C to 60°C storage

9. *On/Off Command:* Relay controlled switching in accordance with HST interface specifications; that is about 1.25 W.

10. *Monitor/TM Functions*

    Analog: (a) 0 to 5.10 V tracking; 0 to 24 kV output
    (b) 0 to 5.10 V tracking; –18 to –24 kV output (suppressed zero)
    (c) 0 to 5.10 tracking, full range input current

    Digital: (a) 1-bit On/Off monitor, from power switching relay
    (b) 10-bit status of D/A holding registers

11. *Other Features:* "Soft" turn-on; output voltage will require at least 2 s to reach 1% of final value.

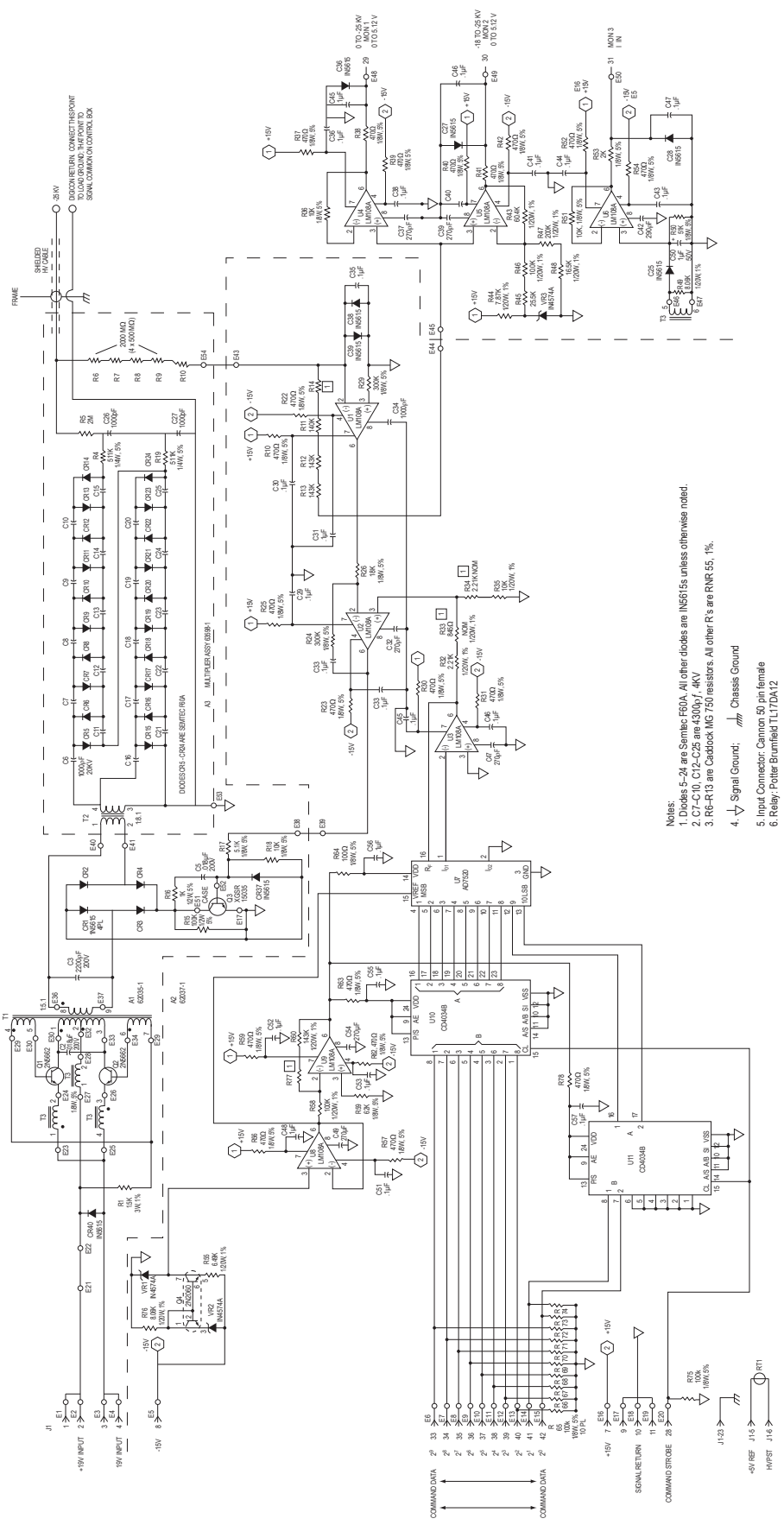

Figure 7.A.1. Circuit for HRS power supply, developmental model.

Operation of –25 kV, FOS Supply

FOS and HRS High Voltage Power Supply Circuit Operation, –25 kV

The power supply operates from a +19 V source. Ql, Q2, and associated circuitry form a current-fed push-pull sine wave oscillator whose frequency of operation is determined by the inductance of Tl, capacitors C2 and C3, and to a lesser extent, the effects of the following circuitry. The peak voltage output from T1 is approximately 160 V.

T2 is used to multiply the output of Tl and applies this to the input of the multiplier stack. The input voltage level to T2 will be the output of Tl minus the drop across Q3, which is the regulating transistor. The maximum output of T2 is approximately 1400 V peak.

The multiplier stack is a series-parallel connected 10 stage device, which boosts the T2 output to a maximum of about –25,000 V. The output of the multiplier stack is RC filtered and brought out of the unit by high voltage shielded cable rated at 30,000 V. The shield is kept at chassis ground. A load return line is also brought out at this point to ensure that the HV load current returns directly to the multiplier stack output.

The output voltage is sensed by voltage divider R6-R14 and U1. U1 nulls at zero and produces an output that is of opposite polarity and about 1/5000th of the HV output. The output of U1 is fed to U2, which nulls with the commanded reference voltage from U3. The output from U2 drives regulating transistor Q3.

Three monitor voltages are provided to check on the state of operation of the unit. U4 provides a voltage that follows the output of U1. U5 produces a voltage that goes from approximately 0 V to +5.1 V as the HV output goes from -18,000 to –24,000 V. U5 produces a voltage that follows the output voltage of T3. T3 senses the emitter currents of Q1 and Q2 and converts this to a voltage across R49. The state of the HV on-off relay can also be monitored. The resistance to ground of pin 44 will be 0 Ω when K1 is closed and infinite ohms when K1 is open.

R34, which makes up part of the voltage divider from U3, is a Texas Instrument sensistor (570 Ω) used to keep the HV output within specification over the temperature range of 0°C to +40°C.

All the high voltage areas (within the dashed line on the schematic) are encapsulated in CONAP EN-11.

R15 (100 kΩ) is placed across Q3 to ensure that the collector of Q3 stays below approximately 200 V. It was found that the collector voltage of Q3 tends to go to the peak-to-peak output of T1 when the unit is commanded to low levels (<700 V). Q3 is not within the encapsulation and the unit will be operated in vacuum. As a result of this, the minimum output voltage of the unit is approximately –500 V at room temperature. Other than for this, the unit is commandable up to –24,000 V in 1024 steps.

Circuit operating frequency is at 35 kHz cycles. Input current is 125 mA maximum.

The circuit diagram in Fig. 7.A.1 is essentially this:

> Sine wave Oscillator →Transformer→ Bridge Regulator → High Voltage Transformer → High Voltage Multiplier

The *Bridge Regulator* in the middle achieves isolation of the high voltage ground from power ground.

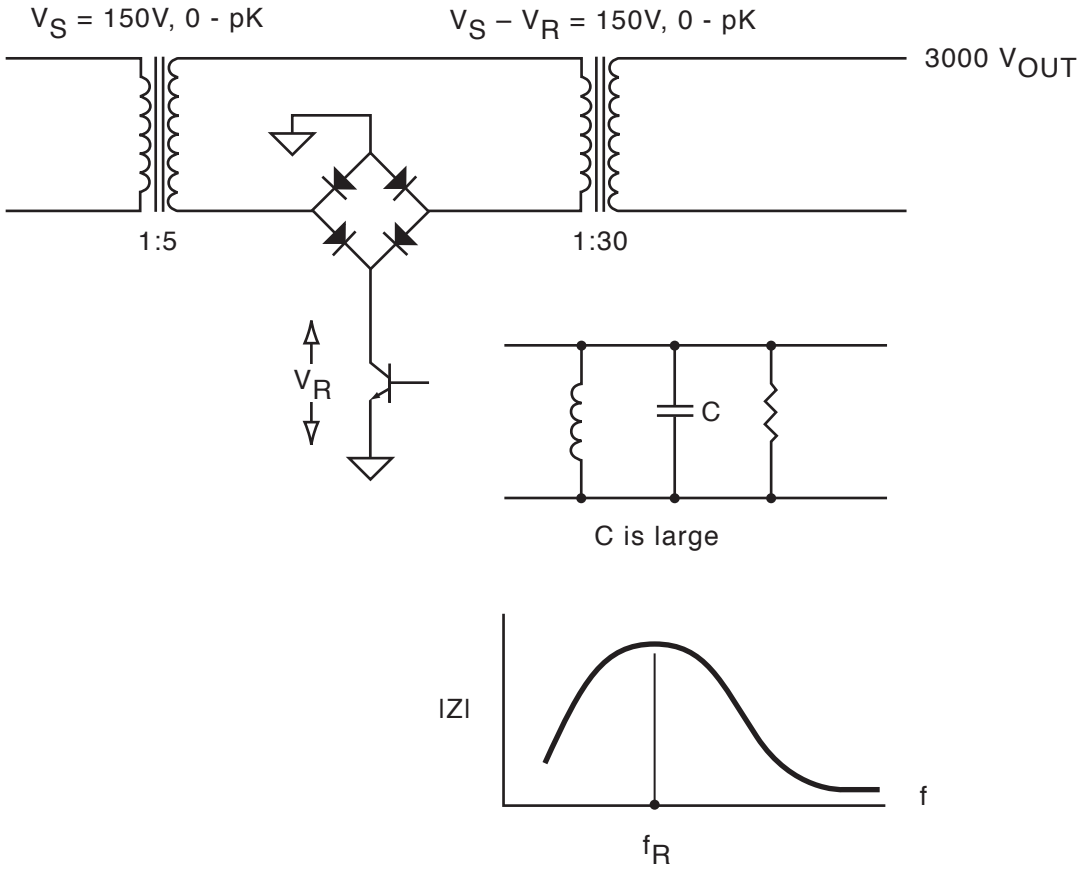

Figure 7.A.2. Bridge regulator.

This Bridge Regulator has the advantage that V_R on the transistor is relatively low, even for output voltage greater than 10 kV, and thus, it was commonly used for ground isolation up to about 1983. However, the input current can increase dramatically if the operating frequency is different from the resonant frequency of the 1:30 turn transformer. This difference can be caused inadvertently by stray capacitances of coaxial cables used or by changes in temperature cycling. So this scheme is not used much any more.

Also, in the High Voltage Multiplier:

$$\frac{V_{\text{Actual}}}{V_{\text{Ideal}}} = \frac{K}{N^2},$$

where N= the number of stages in the Multiplier. One can put the stages in a single multiplier in groups of five in "parallel" to reduce losses and ripple. Then, however, the input capacitor to the multiplier stacks will need a rating commensurate with the output voltage. The transformer itself should be able to withstand full output voltage in the event of a shorted output.

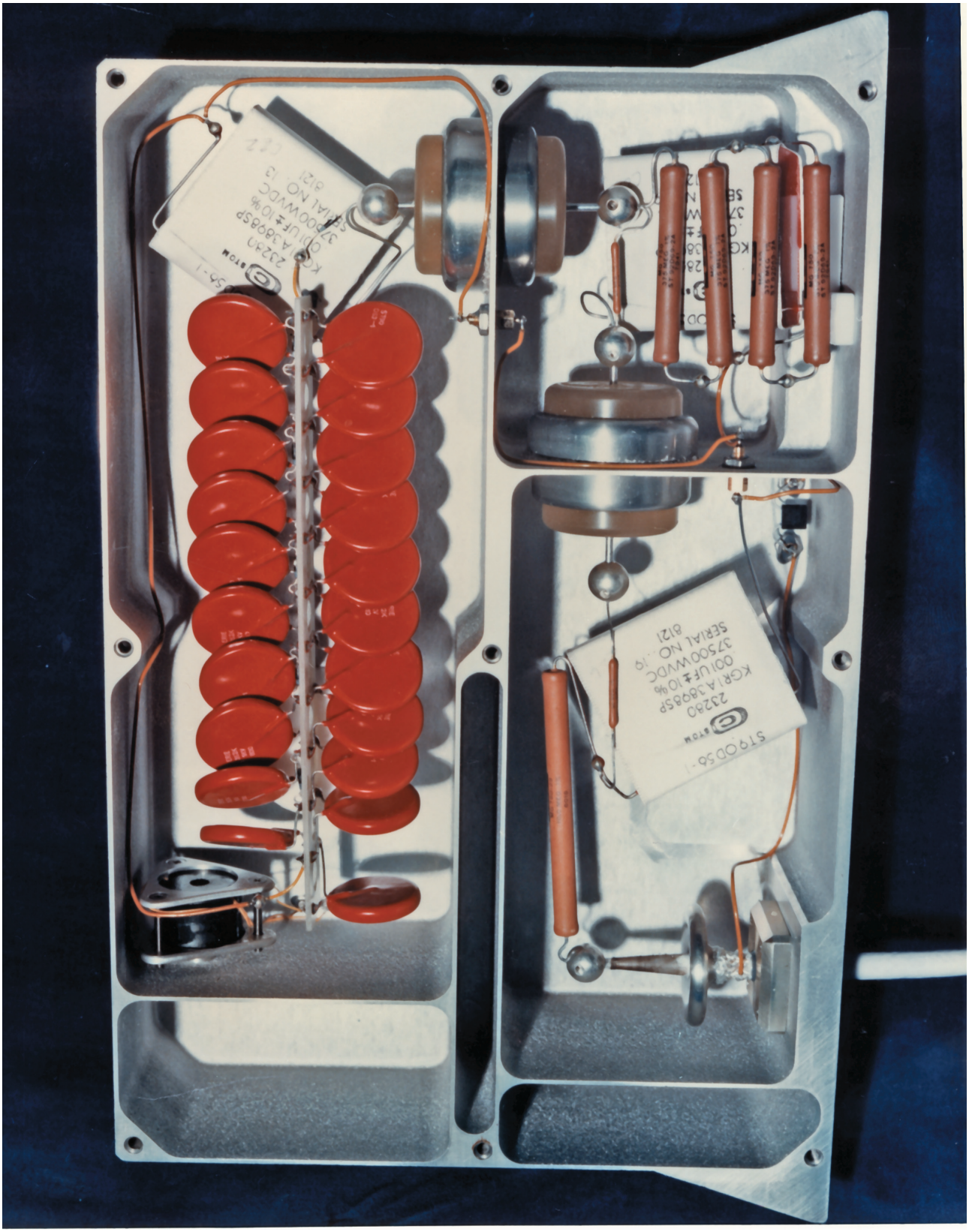

Figure 7.A.3. Photograph of the HV portion of the HRS power supply before potting.

Discussion of Fig. 7.A.3:

Several things are noteworthy in the photograph showing the construction of the high voltage portion of the power supply before potting:

1. This is an example of a high voltage portion that was later solid potted with Conathane EN-11, including the high voltage transformer, T2. The potting extended up to the top of the shielding box. (This is actually undesirable. The top of potting should be a mechanically unconstrained surface.)
2. The careful construction of the feedthru(s) through the shielding walls should be noted.
3. Hardwiring is done with bare buswire; the later EN-11 potting serving as insulation.
4. Stress relief bends and loops are on each part.
5. Use is made of three Custom Electronics Co. *impregnated* micapaper capacitors, 1000 pF, 37.5 kV rated.
6. Caddock type MG 750 resistors are used.
7. There *is* a *problem site*: Note where the high voltage cable exists from inside the box. Just before the exit there is an anti-corona donut attached to the cable where the shielding is peeled back. There was prolonged (about 6 years) storage after the Build and the Thermal Vacuum test before Flight. Failure occurred during the Thermal Vacuum test at the braid peel-back spot and at the anti-corona donut:
   (a) The EN-11 had cracked at the donut, probably induced by the differential expansion/contraction between the large metallic donut and the EN-11, probably further exacerbated by the lid pressing on the top surface of the EN-11 potting.
   (b) Black residue was seen upon cutting into the potting, where the shielding braid was bent back over the neck of the anti-corona donut.

It is believed that the problem was solved by deleting the too large anti-corona donut and using a small anti-corona ball at the braid peel-back area. This is a good example where an optimum electric field design in theory clashes with differential thermal expansion properties of the different materials involved in the actual construction, and an engineering compromise has to be reached. The theoretical design was published before the aforementioned failure was discovered.*

*High Voltage Power Electronics Packaging on NASA's Space Telescope, by, S.R. Yadavalli, J.L. Westrom, and J.W. Williams; 17th IECEC, 1982, p. 211.

DESIGN EXAMPLE B

A –15 kV Plasma Experiment Power Supply for IMP-G, by, John L. Westrom, Goddard Space Flight Center.

This –15 kV Plasma Experiment power supply for IMP-G is an earlier supply, already described in Sutton and Stern's *NASA-TN-D- 7948* Spacecraft Power Supply Construction book, and also in GSFC document *X-716-68-252*. It is briefly taken up here again because it is one of very few examples of solid potting with RTV-615 silicone rubber. Although in the last 20 years, mostly polyurethanes have been used for solid potting, nevertheless there recently (year 2004) were requests to GSFC for advice on how to make solid potting with silicone rubber a success.

The –15 kV supply was "located immediately adjacent to the instrument to which it gave the high voltage bias, thus eliminating the need for HV cables and connectors exiting from the RTV-615." For the flight units, the HV output lead in the center of the top of the circuit board was *not* the insulated wire shown in the engineering model in Fig. 7.B.l. The flight model had a bare wire helix through the encapsulant through a Kel-F insulated circular cover on top. This cover was directly above (about 1 in) the top side of the assembled circuit board and held a smooth corona ball outside and above the Kel-F barrier (Fig. 7.B.2). This barrier extended only a fraction of an inch down along the cylindrical side of the potted supply by means of a circular metal ring. The potting on the circular bottom of the assembly was only about 0.25-in thick because it had no high voltage points on it. The diameter of the power supply was approximately 9.5 cm.

All of the HV components were mounted on etched Teflon stand-offs on the top side, and the Kel-F circular disc was especially etched also. The solid disc ceramic capacitors were *not* wax-impregnated, but especially cleaned and then primed with a 50-50 mix of Epon 828/Versamid 140 and overcoated with silicone rubber DC 93-500. Probably the same treatment was done to the other HV circuit parts; this adhered well to the RTV-615 encapsulant.

The vacuum encapsulation was carried out for the entire assembly with RTV-615 in *a removable mold* of slightly smaller internal dimensions than the metal shielding chassis. The cured, potted power supply was then removed from the mold. It was then coated with a thin layer of a mix of RTV-615 and powdered carbon black, on the cylindrical and bottom surfaces, so that bleeding off of static charge to the inside of the grounded chassis box could occur. The tolerances of dimensions between the outside of the coated power supply and the inside of the grounded metal chassis box are not available to the writer any more. But it has to be such that during thermal cycling the RTV-615 silicone rubber can expand and contract with respect to the metal shielding chassis without being constrained. No adhesion is necessary of the potting to the inside of the grounded chassis box, if bleed-off of charge is assured by the carbon-containing coating. Thus, if constraining of the silicone rubber is avoided during its large thermal expansion and contraction upon thermal cycling, then the silicone rubber will not crack. The cracking and tearing loose from circuit components of silicone rubber during thermal cycling must be avoided by taking its large thermal expansion and contraction into consideration in the original design.

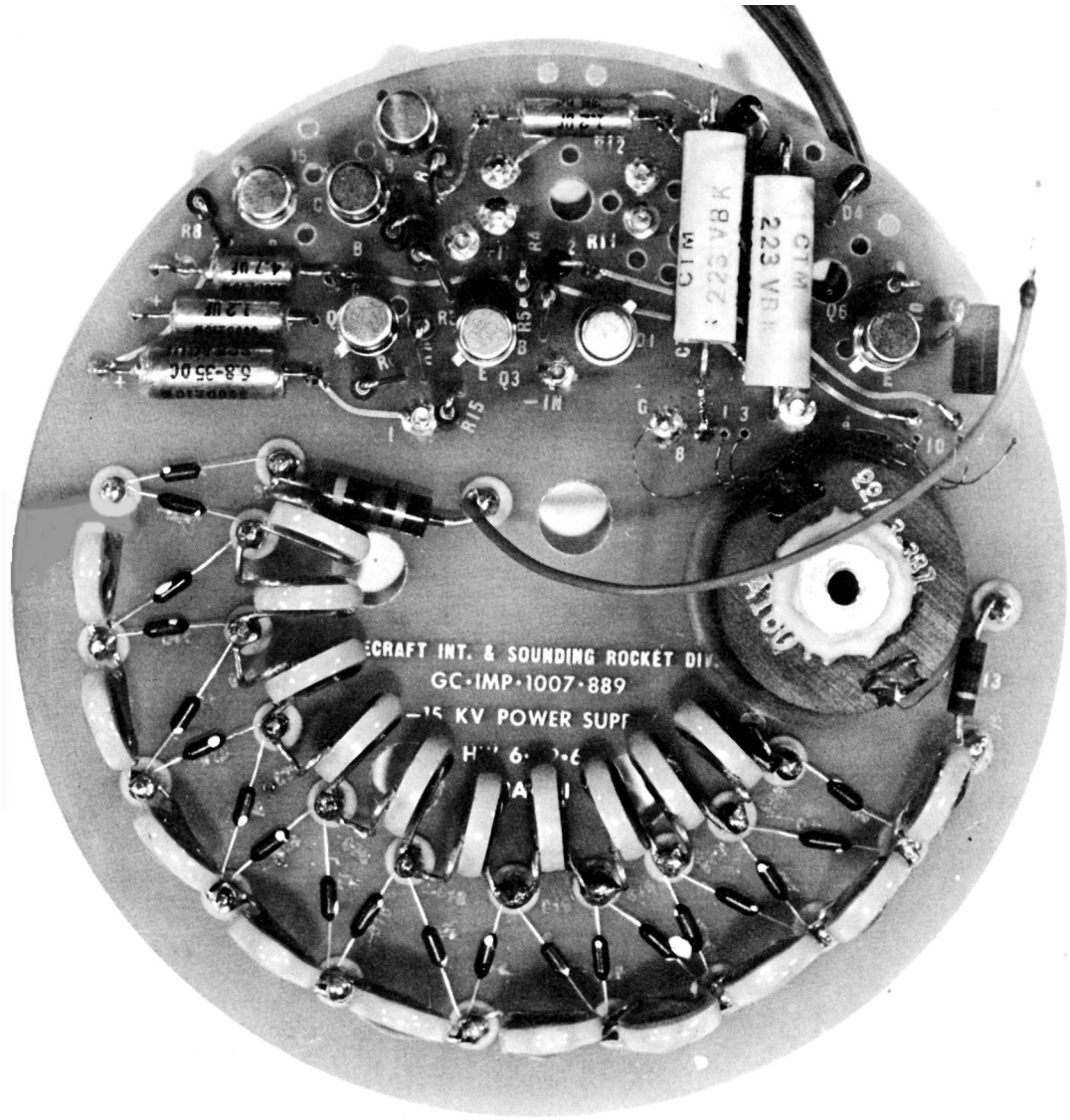

Figure 7.B.1. High voltage supply component layout, top.

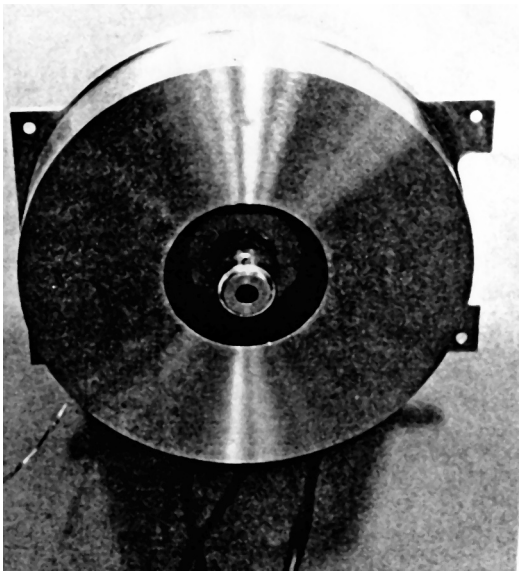

Figure 7.B.2. A 15 kV supply, top.

DESIGN EXAMPLE C

A Quick Response, 4 Decade Logarithmic High Voltage Stepping Supply, to ±2500 V (also called HAPI LAPI), by, Henry Doong, GSFC.

Packaging

The High Voltage portion of this circuit, namely the HV shunt regulators and the HV generator/modulator, were only conformally *coated* with EN-11 polyurethane, *not* solid potted. Because the maximum voltages were only ±2500 V, this packaging was successful. The coating was applied by spraying, not brushing. The parts were spot-staked. For the techniques of coating for high voltage, see *Materials Processing Document S-313-019*, NASA/GSFC: "Conformal Coating of HV Printed Wiring Boards with a Room-Temperature Curing Two-Part Urethane Resin," September 1992.

Circuit Design

The circuit discussion of this power supply is best accomplished with a document by the design engineer himself, which is herewith included. The Figure numbers of this document are left as in the original document

INTRODUCTION

The design of low power, high voltage supplies usually consists of an amplitude modulated high frequency tuned oscillator in conjunction with a voltage multiplier and filter to raise the available voltage to the desired output level. This type of circuit arrangement does not meet the design goals when a fast response time is required as the output voltage response time is prolonged by the time constant associated with the voltage multiplier-filter capacitor and load. To compensate for the fast response time, either or both the capacitor value and the load resistance must be reduced, but a reduction in resistance leads to a large increase in input power while a smaller capacitor value results in a large ripple voltage; or if operated at higher frequencies, the ripple voltage improves but the efficiency is reduced. To minimize the response time without increasing the input power or output ripple voltage, the high-voltage stepping supply uses an active high-voltage shunt regulator at the high-voltage output.

To meet the design goals of the four decade dynamic range, two innovative circuits are used. One circuit uses the 6 bit to 32 step decoder, which requires only 12 scaling resistors rather than the 32 in a conventional design. The other circuit has two complementary amplifier channels with each channel producing one-half of the 64 step staircase waveform; each channel is "gated" on at the appropriate time to produce a complete staircase voltage at the output.

The high-voltage stepping supply is equipped with a self-contained low voltage source for the internal circuits, an overload and over voltage protection circuit, and two output voltage monitor circuits. The supply, including the supply housing, weighs 1-1/2 pounds and occupies a volume of approximately 63-cubic inches.

SYSTEM DESCRIPTION

The stepping supply functional block diagram, Fig. 1 [7.C.1], consists of the following units.

- 6 bit to 32 step logarithmic staircase generator (two consecutive 32 steps per cycle)
- Reference voltage source
- Signal processor
- Oscillator, modulator, and parallel charge multipliers
- High voltage DC shunt regulators

OPERATION

Six Bit to 32 Step Logarithmic Staircase Generator

The 6 bit to 32-step logarithmic staircase generator, Fig. 2 [7.C.2], accepts the 6 bit binary input command at the basic clock rate of 64 steps per second (15.6 ms step dwell time). Each bit is passed through a buffer stage (Q_1 through Q_6) and an inverter logic IC-1 (CD4049A). The three most significant bits (MSB) interface with the multiplexer IC-2 (CD4051A). The other three least significant bits (LSB) are level shifted by Q_7, Q_8 and Q_9. Thus for the LSB, a logic "1" is zero volt and a logic "0" is –10 volts. The level shifters are necessary to interface with multiplexer IC-3 (CD4051A) as the switches are connected to the negative potential.

The two multiplexers, IC-2 and IC-3, combined with amplifier A1 and the 12 resistor matrix, constitute a multigain summing amplifier, with resistors R_f as the feedback resistor and R_{in} as the input resistor. Each switch in the multiplexers is selectively turned on by the 6 bit input code. Thus for any step, the amplifier A1 output voltage E1 can be written as:

$$E_1 = \frac{R_f}{R_{in}} x(V_r). \tag{1}$$

Where:

E_1= the output voltage of A_1

R_f= feedback resistance selected by LSB code

R_{in}= input resistance selected by MSB code

V_r= reference voltage, 7.50 volts

The circuitry provides 32 logarithmically scaled voltage levels at the output E_1. Each level is determined by two discrete switch closures. The MSB code closes a discrete switch in IC-2 and the LSB code closes another discrete switch in IC-3. Accordingly, one scaling resistor of four is chosen for R_{in} and one scaling resistor of eight is chosen for R_f. The total number of combinations available is 32. Since the basic clock rate is 64 steps per second, the logarithmic staircase will be generated twice per second. The resistive scale factors are chosen to cover two decades of voltage over the 32 levels. Table 1 [7.C.1] shows amplifier A_1 output E_1 vs. input command code and the corresponding scaling resistors.

Table 1. [7.C.1]. Six bit to 32-step voltage levels and scaling resistors versus command code.

No.	Code*	E_1	R_{in}	R_f	No.	Code*	E_1	R_{in}	R_f
1	X00000	-7.500	100K	100K	17	X10000	-0.7500	1M	100K
2	X00001	-6.495	100K	86.6K	18	X10001	-0.6495	1M	86.6K
3	X00010	-5.625	100K	75.0K	19	X10010	-0.5625	1M	75.0K
4	X00011	-4.872	100K	64.9K	20	X10011	-0.4872	1M	64.9K
5	X00100	-4.218	100K	56.2K	21	X10100	-0.4218	1M	56.2K
6	X00101	-3.654	100K	48.7K	22	X10101	-0.3654	1M	48.7K
7	X00110	-3.165	100K	42.2K	23	X10110	-0.3165	1M	42.2K
8	X00111	-2.739	100K	36.5K	24	X10111	-0.2739	1M	36.5K
9	X01000	-2.374	316K	100K	25	X11000	-0.2374	3.16M	100K
10	X01001	-2.056	316K	86.6K	26	X11001	-0.2056	3.16M	86.6K
11	X01010	-1.781	316K	75.0K	27	X11010	-0.1781	3.16M	75.0K
12	X01011	-1.542	316K	64.9K	28	X11011	-0.1542	3.16M	64.9K
13	X01100	-1.336	316K	56.2K	29	X11100	-0.1336	3.16M	56.2K
14	X01101	-1.157	316K	48.7K	30	X11101	-0.1157	3.16M	48.7K
15	X01110	-1.002	316K	42.2K	31	X11110	-0.1002	3.16M	42.2K
16	X01111	-0.8679	316K	36.5K	32	X11111	-0.0868	3.16M	36.5K

* “X” denotes a “don’t care bit.”

REFERENCE VOLTAGE SOURCE

The reference voltage V_r, Figure 2 [7.C.2], for the staircase generator is obtained from two stable 6.8 volts, temperature-compensated zener diodes, D_1 and D_2. The field effect transistor FET (Q_{10}) is employed to furnish a constant current source to the two diodes. Resistors R_1 and R_2 scale the zener voltage to exactly 7.50 volts. Amplifier A_2 serves as the buffer for the low source impedance to the load.

SIGNAL PROCESSOR

The signal processor, Figure 3 [7.C.3], has four basic functions:

1. to condition staircase waveform E_1 so that the proper polarity and format are provided at V_p and V_n
2. to amplify and deliver a pair of mirror image staircase voltages at +LV and –LV
3. to compensate for the temperature and tracking error of each mirror image voltage
4. to alternately select each of the two amplifier channel voltages which produce $+V_0$ and $-V_0$ outputs.

As shown in Figures 2 [7.C.2] and 3 [7.C.3], the 32 level staircase E_1 waveform is applied to each of the two sets of amplifiers, One set, consists of two inverting unity gain amplifiers A_1 and A_2. When the 2^5 bit logic is “Zero,” amplifiers A_1 and A_2 produce a pair of mirror image staircase voltages V_p and V_n, refer to Figure 4 [7.C.4], to set the highest two decade voltage outputs in the first half cycle of the total staircase waveform. However, when the 2^5 bit logic is “One” during the second half cycle of the total staircase waveform, the voltage E_1 is blocked from going through the amplifiers. The voltage at V_p becomes slightly positive while the voltage at V_n becomes slightly negative.

V_p is used to dynamically control the positive shunt regulator to provide the regulation output $+V_0$ during this half cycle (steps 1–32). V_p is also compared with the feedback voltage from the multiplier stack output +HV. The difference is the error voltage and is amplified to control the +HV level via the modulator.

V_n, the mirror image of V_p, controls the negative shunt regulator output $-V_0$ during the same first half cycle to provide the regulated output $-V_0$.

The second amplifier set is used to provide the logarithmically scaled voltage levels during the second half cycle (steps 33–64). It consists of amplifier A_3 (gain = –3.33) and amplifier A_4 (gain = –1) and a temperature compensation network $R_1 - D_1$, refer to Figure 3 [7.C.3].

The staircase outputs, +LV from amplifier A_3 and the mirror image –LV from amplifier A_4, refer to Figure 4 [7.C.4], are used directly as outputs $+V_0$ and $-V_0$ respectively during the second half cycle, (steps 33–64). Actually these outputs are connected to $+V_0$ and $-V_0$ by means of the high voltage steering diodes, D_{10} and D_{20}, refer to Figure 6 [7.C.6]. During the first half cycle (steps 1–32), when the highest two decades of output levels are regulated by the high voltage shunt regulators, both of these diodes (D_{10} and D_{20}) are reverse biased since ±LV outputs never exceed $\pm V_0$.

During the second half cycle, the slight positive voltage on V_p is sufficient to cut off the parallel charge multipliers; therefore, no voltage is generated at either +HV or –HV output terminals. This allows the two steering diodes D_{10} and D_{20} in Figure 6 [7.C.6] to conduct, providing the lower two decade outputs to $+V_0$ and $-V_0$. The voltage drop across each diode is compensated by an equal offset diode (D_1) voltage (V_d) to the amplifier A_3 input in Figure 3 [7.C.3]. Diode D_1 is similar to the steering diodes, and resistor R_1 provides the necessary compensating current.

The equations for defining the outputs: V_p, V_n, +LV, and –LV in Figure 3 [7.C.3] are:

First half cycle (steps 1–32)

$$V_p = (-1)(-1)\, E_1 = E_1 \tag{2}$$

$$V_n = (-1)\, E_1 \tag{3}$$

$$+LV = (-3.33)\, E_1 + (-1)\, (V_d) \tag{4}$$

$$-LV = (-1)(+LV) \tag{5}$$

Second half cycle (steps 33–64)

$$V_p = (-1)(-1)(\text{“1”}) = \text{positive voltage greater than 1 volt} \tag{6}$$

$$V_n = (-1)(\text{“1”}) = \text{negative voltage greater than 1 volt} \tag{7}$$

$$+LV = (-3.33)\, E_1 + (-1)(V_d) \tag{8}$$

$$-LV = (-1)(+LV) \tag{9}$$

Notes:

E_1 and V_d are always negative

(“1”) denotes 2^5 bit logic “One”. It is always greater than E_1 in magnitude and positive.

Using –7.5 volts as the maximum voltage for E_1 (steps 1 or 33), the following voltages yield:

First half-cycle, step 1

(From eq. 2) V_p=-7.5 volts
(From eq. 3) V_p=+7.5 volts
(From eq. 4) +LV=25 + 3 = 28 volts (assume V_d = –3 volts)
(From eq. 5) –LV= –28 volts

Second half-cycle, step 33

(From eq. 6) V_p= positive voltage greater than 1 volt

(From eq. 7) V_n= negative voltage greater than 1 volt

(From eq. 8) +LV = 25 + 3= 28 volts (assume V_d = -3 volts)

(From eq. 9) –LV = –28 volts

OSCILLATOR

The 60 kHz sine wave oscillator, Figure 5 [7.C.5], consists of transistors Q_1 and Q_2, inductor L_1 and transformer T_1, refer to Reference 2. The operating frequency is determined by the secondary inductance and shunt capacitance C_1, Inductor L_1 keeps the current through it fairly constant at all times, reducing sharp current spikes when the transistor is turned on and minimizing conducted radiated EMI to nearby circuits.

The peak primary voltage ($\pi/2$ times V_{cc}) is 57 percent higher than the standard Hartley or Colpitts oscillators. When V_{cc} equals 24 volts and the transformer T_1 step-up ratio is 3, the secondary peak output voltage of 226 volts is realized.

MODULATOR

The diode modulator is a full wave diode bridge (D_1 through D_4), Figure 5 [7.C.5]. The bridge circuit is connected in series with transformer T_2 primary, with transistors Q_3 and Q_4 acting as the variable load across the bridge arms. Transistors Q_3 and Q_4 are in parallel to share the worst case load dissipation condition.

The oscillator output from the step up T_1 secondary winding is divided between the load and transformer T_2. The voltage across the secondary winding is again stepped up to produce about 1 kV peak-to-peak. Transformer T_2 is tuned to the same frequency as the oscillator frequency with capacitor C_2 so the minimum reactive load is reflected to the oscillator and modulator circuitry.

PARALLEL CHARGE MULTIPLIERS

The relatively high AC voltage (approx. 1000 Vpp) from transformer T_2 secondary is fed into two sets of multiplier stacks, Figure 5 [7.C.5]. One set generates a positive high-voltage staircase at +HV and the other set produces a negative high-voltage staircase at –HV. Each stack, composed of 6 diodes and 6 capacitors, is connected in a parallel-charge configuration rather than in a series-charge configuration as in the Cockcroft-Walton multiplier. The parallel-charge configuration is more efficient when several voltage multiplier stages are used. The trade-off is the AC capacitor peak inverse voltage must be N-times larger in the N-th stage of the multiplier.

The positive high-voltage +HV and negative high-voltage –HV are the result of the rectified multiplier stack voltages. Their magnitude is dictated by the inputs to the summing amplifier A_1, Fig. 5 [7.C.5], namely the staircase waveform V_p and the fixed offset voltage. As each step advances, the staircase waveform at V_p immediately introduces an error signal to the amplifier A_1 input. The amplified error signal drives the base terminal of the two parallel transistors, Q_3 and Q_4, connected across the diode bridge. This drive signal determines the available collector to emitter resistance across the diode bridge. Since the oscillator signal is shared between the diode bridge and the primary winding of transformer T_2 only that portion across T_2 is stepped up and multiplied. The multiplier output voltage +HV adjusts accordingly until the feedback current through resistor R_f cancels the error signal that has been generated by the V_p staircase waveform.

Thus summing amplifier A_1, combined with the diode modulator and the parallel charge multiplier, Fig. 5 [7.C.5], may be considered as an operational amplifier with a gain equal to:

$$+HV = -V_p\, R_f/R_{in} + (V_s)\, R_f/R_b \qquad (10)$$

where

R_f = 110 MΩ,
R_{in} = 301 kΩ,
R_b = 3.3 MΩ (offset input resistance), and
V_s = 3 V (offset voltage).

Therefore, +HV = –365.4 V_p + 100.

As mentioned earlier V_p in step 1 is –7.50 volts, substituting this voltage in equation 10 yields +HV equal to 2840 volts. This is the maximum voltage developed at +HV, with the same negative voltage occurring simultaneously at the –HV terminal.

Normally, the +HV and –HV outputs can be used as the final output voltage for the external load if the step time is at least several times larger than the transient time. The transient time is the rise or fall time of the RC time constant of the multiplier stack used and is typically about 20 milliseconds. When the step time is small, as in this application (15.6 ms/step), several alternatives can be used to meet the requirement. Some examples follow below.

Reduce the Load Resistance

Assuming that the equivalent capacitance of the multiplier stack is 1000 pF, to obtain a time constant of 1 millisecond a 10^6 ohm resistor must be used from the +HV output to ground. The 10^6 ohm resistor will dissipate 6.25 watts of power at +HV when the +HV equals 2500 volts. A similar resistor must be used between the –HV output and ground which dissipates an additional 6.25 watts.

Decrease the Multiplier Capacitance

Assuming the load resistance is 10^8 ohms, to keep the power dissipation to a reasonable level for the same time constant of 1 millisecond it would require the equivalent capacitance on the multiplier to be no larger than 10 pF. A multiplier stack with such small capacitors in the chain would be inefficient with a large ripple voltage that may exceed the magnitude of the step voltage itself. Although the ripple voltage may be reduced if the oscillator frequency is near one MHz, but operating at this frequency would create many new problems such as: diode leakage in the multiplier, RF shielding, and excessive core loss in the transformer, etc.

Add an Active Circuit to the Load

By adding a dynamic dc shunt regulator to the load, the low resistance shunt would discharge the excessive charge during transition times but then would act as a very high resistance during the steady state condition. This shunt regulator is described in the following section.

HIGH-VOLTAGE DC SHUNT REGULATOR

The use of two shunt regulators, one to regulate the positive voltage output from +HV and the other to regulate the negative voltage output from –HV, are coupled through isolation resistors R_d as shown in Figure 6 [7.C.6]. The resistors allow the regulated outputs $+V_0$ and $-V_0$ to track the input waveform V_p faithfully with a fixed gain; Figure 7 [7.C.7] shows the improvements to these waveforms. The transition time between steps of the +HV waveform is measured to be about 20 milliseconds. For high-level steps, the shunt regulator output $+V_0$ is less than 1 millisecond. For low-level steps, the transition time for both +LV and $+V_0$ are approximately 100 microseconds.

Operation of the DC Shunt Regulator

Amplifier A_1, Figure 6 [7.C.6], receives waveform V_p via input R_1 connected between V_p and the virtual ground input. It also receives the stepping supply output $+V_0$ as a feedback signal via resistor R_2. The shunt regulator and amplifier A_1, when combined, have a negative overall gain determined by the ratio of R_2 to R_1. The voltage $+V_0$ is then

$$+V_0 = \frac{-R_2}{R_1} V_p = -333\ V_p \cdot \tag{11}$$

Compare equation 11 with equation 10; (+HV) – (+V_0)= 0.1 V_0 + 100 or the difference of 100 volts plus 10 percent of the output voltage. The difference is the drop across the resistor R_d which provides a margin of regulation for the shunt regulator.

Because of the relatively high maximum voltage (2500 volts) appearing at $+V_0$ and the limited breakdown voltage of available solid-state devices, the shunt regulator, Reference 3, is composed of 9 stages connected in a totem pole configuration. The NPN transistors (Q_1 to Q_9) are rated at 400 volts, and the zener diodes (D_1 to D_9) are rated at 300 volts. This arrangement permits the voltage $+V_0$ to be divided across the 9 transistors.

Each shunting zener diode limits the voltage across its companion collector to emitter junction to about 300 volts. The emitter and base of each transistor are connected by a separate resistor for shunting transistor leakage current in a conventional manner. All bases are coupled to amplifier A_1 output via separate high-voltage diodes (D_{11} to D_{19}) in series with current limiting resistors (R_5 to R_{13}). These diodes are reverse biased whenever their connecting base-to-emitter junction resides at 300 volts or greater. Amplifier A_1 output can drive each base (Q_1 to Q_9), one at time, into active linear conduction. If the base is overdriven, the transistor saturates and pulls the next series transistor into conduction.

The composite shunt regulator is variable driven into conduction by the output of amplifier A_1 to a voltage at terminal $+V_0$, refer to equation 11. Current conducts from +HV, through dropping resistor R_d, into the shunt regulator. This current at $+V_0$ passes through all zener diodes whose companion transistors are biased off. It then passes through the transistors to the –10 volt return. For discussion purposes, it is assumed that that the zener diodes have a breakdown voltage of 300 volts and that the instantaneous voltage of $+V_0$ is 1400 volts. Starting from terminal $+V_0$, the first four zener diodes (D_1 to D_4) are in conduction and provide a voltage across diodes D_1 to D_4 of 1200 volts. The remaining diodes (D_5 to D_9) and the first four transistors (Q_1 to Q_4) are at cutoff. The conduction path then passes through the fifth until the ninth transistor (Q_5 to Q_9). Q_5 is dynamically controlled by the output of amplifier A_1 so that it has a collector-emitter voltage drop of approximately 200 volts. Transistors Q_6 to Q_9 are saturated and have a voltage drop approaching zero volts producing the 1400 volts from terminal $+V_0$ to ground. The first four transistors (Q_1 to Q_4) are maintained at cutoff because the emitter voltage established by the first four zener diodes are higher than the small base voltage established by amplifier A_1.

Thus for any instantaneous voltage $+V_0$, not more than one of the transistors is dynamically controlled by amplifier A_1. All transistors above the controlled transistor are at cutoff and the transistors below the controlled transistor are saturated. Each transistor assumes control in different adjoining 300-volt ranges, whereby transistor Q_1 dynamically controls $+V_0$ between zero and 300 volts, transistor Q_2 dynamically controls $+V_0$ between 300 volts and 600 volts, and so forth. The shunt regulator is returned to a –10 volt source rather than to ground in order to enable the low gain amplifier output +LV to pass through the steering diode D_{10} to the output $+V_0$, when $+V_0$ is less than 25 volts. As mentioned before, when the output $+V_0$ is between the range 2500 volts and 25 volts, it obtains its voltage from the parallel charge multiplier output +HV through the dropping resistor R_d. When it is in the 25 volt or less range, it obtains its voltage from the low gain amplifier output +LV through the steering diode D_{10}. The control for this process is a logic "OR" function. The inputs to the "OR" are +HV and +LV and the output is the $+V_0$ voltage. For the MSB range, a staircase voltage at E_1 (Figure 1 [7.C.1]) is amplified by a gain of –333 to become $+V_0$ by controlling the paral-

lel charge multiplier voltage +HV and the dc shunt regulator gain. For the LSB range this amplification gain is only –3.33 by controlling the low-gain amplifier. Therefore, $E_1 = –7.5$ volts, $+V_0$ would be 2500 volts via the high channel and +25 volts via the low gain channel. The LSB range covers the second half cycle (steps 33 to 64) of the 64 step cycle. During this period, the $+V_0$ output is obtained via the low gain channel and is equal to:

$$+V_0 = +\text{LV-steering diode drop} \tag{12}$$

$$= 28 – 3 = 25 \text{ volts.}$$

Also during this period all the transistors in the shunt regulator are saturated on and the diode modulator is turned off, effectively blocking any voltage build up at +HV. This condition is created by the 2^5 bit that causes a slight positive voltage at V_p. The shunt regulator is dormant during this period with a passive load from $+V_0$ to –10 volts of 100 kilohms.

The negative voltage shunt regulator operates similar to the positive voltage shunt regulator. There two additional circuits used in the negative voltage regulator to bring its voltage $–V_0$ exactly equal to, but opposite in polarity from the $+V_0$ voltage. One is the "BAL. ADJ." trimming resistor coupled to the input of the amplifier A_2 in Figure 6 [7.C.6]; this adjustment is for the high gain channel. The other is the low gain adjust (LGA) resistor network coupled to the input of amplifier A_4, Figure 3 [7.C.3], to adjust for the low gain channel output. This slight difference in voltage between the two outputs is due to component tolerance error in each channel. A to be determined (TBD) capacitor across R_2 in the feedback loop of each shunt regulator is used to adjust for critical damping in the operational amplifier loop.

CONCLUSION

Although the high-voltage stepping supply described here pertains to step-down staircase voltages, a step-up staircase voltage may be constructed by using the same design principles.

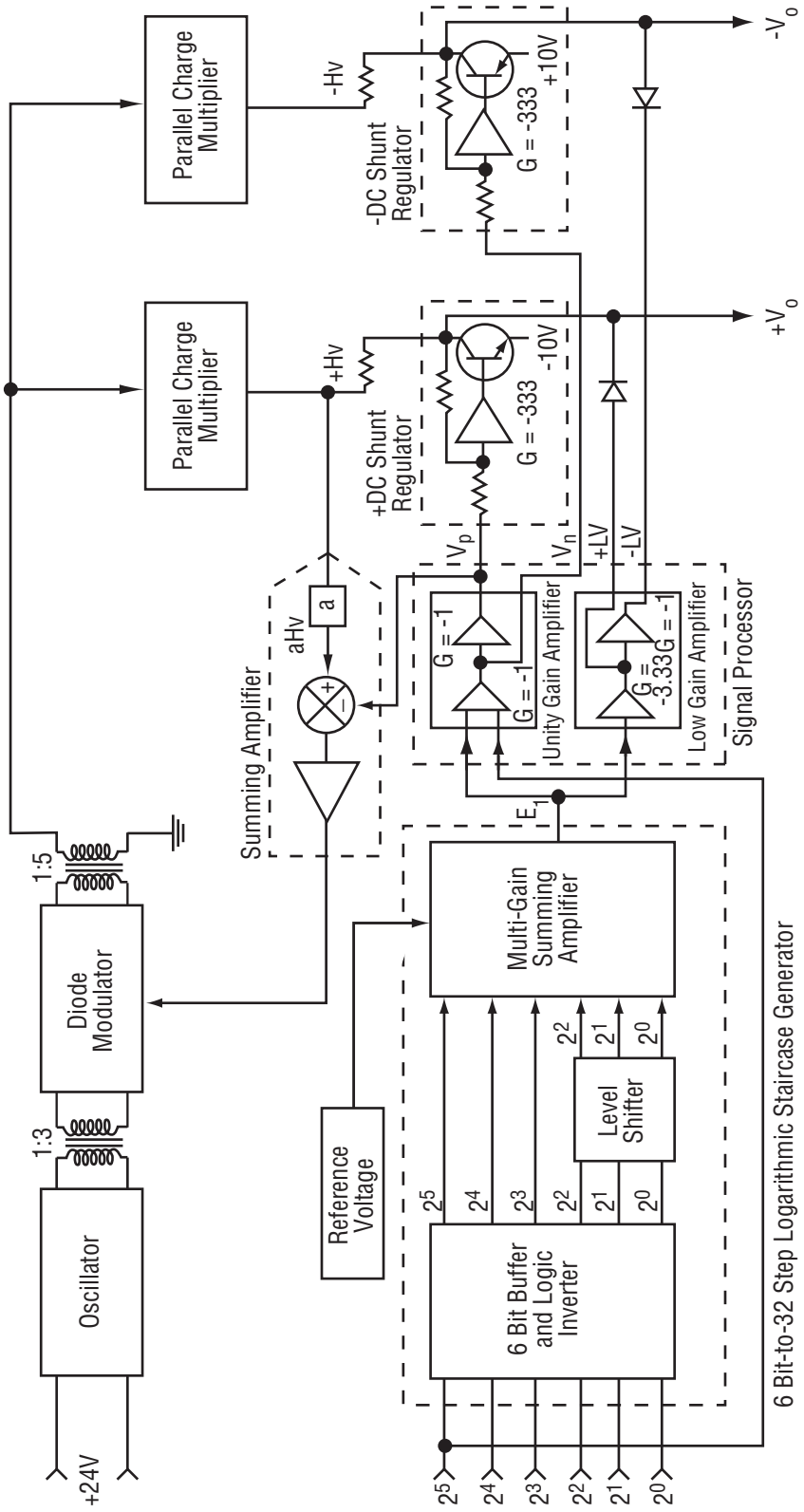

Figure 1 [7.C.1]. Stepping supply functional diagram.

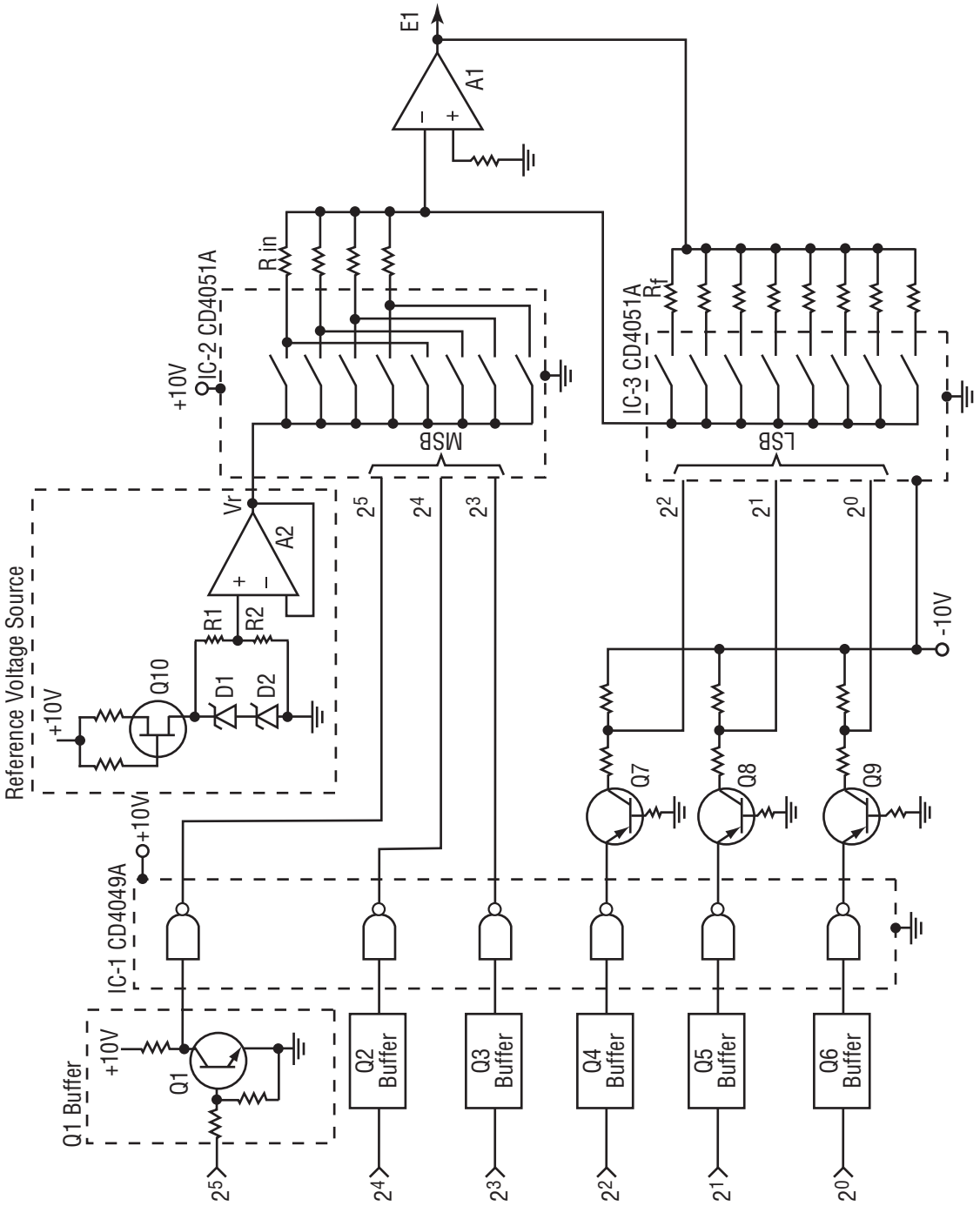

Figure 2 [7.C.2]. Six bit to 32-step logarithmic staircase generator.

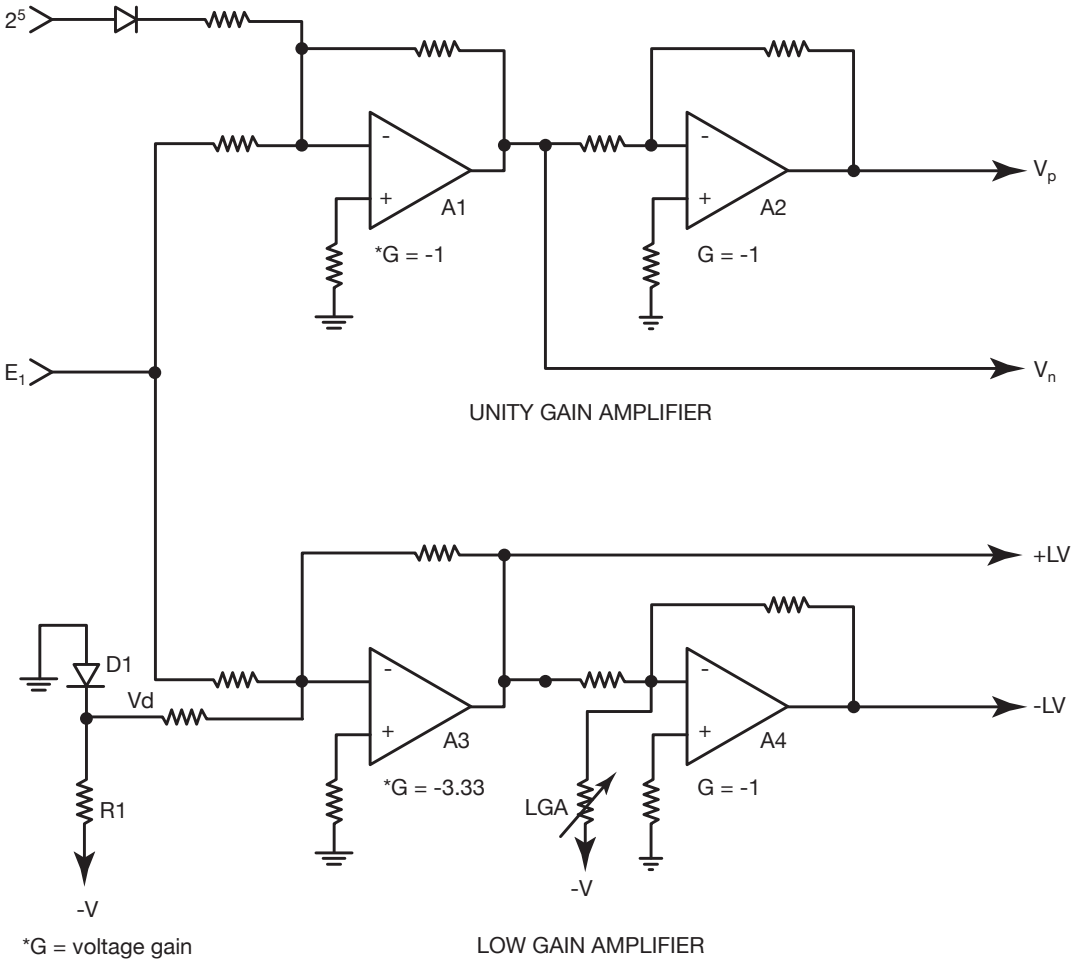

Figure 3 [7.C.3]. Signal processor.

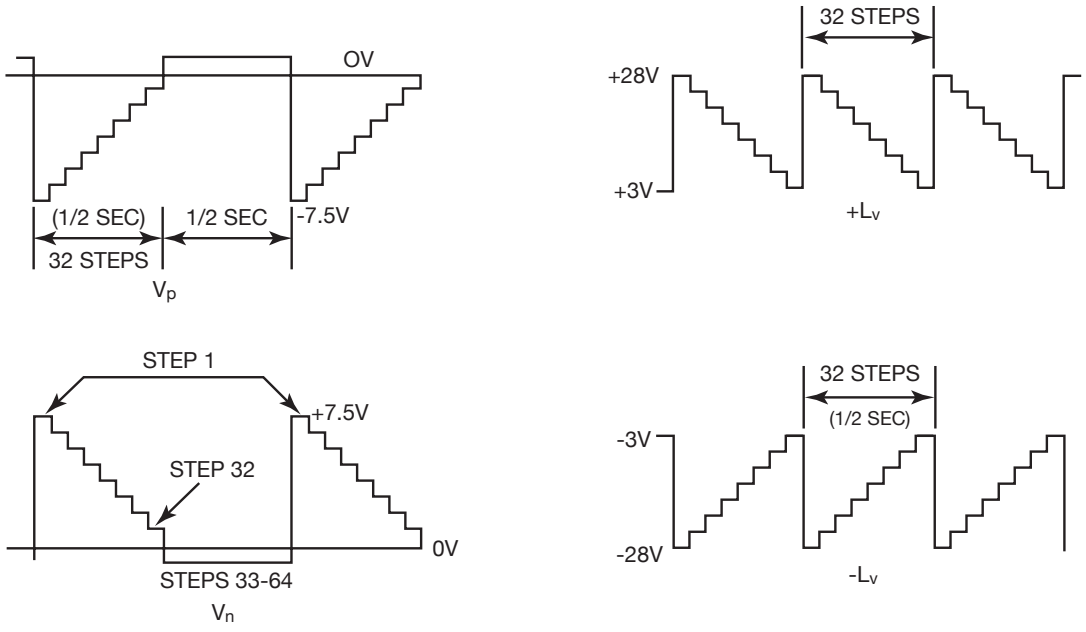

Figure 4 [7.C.4]. Signal processor output waveforms.

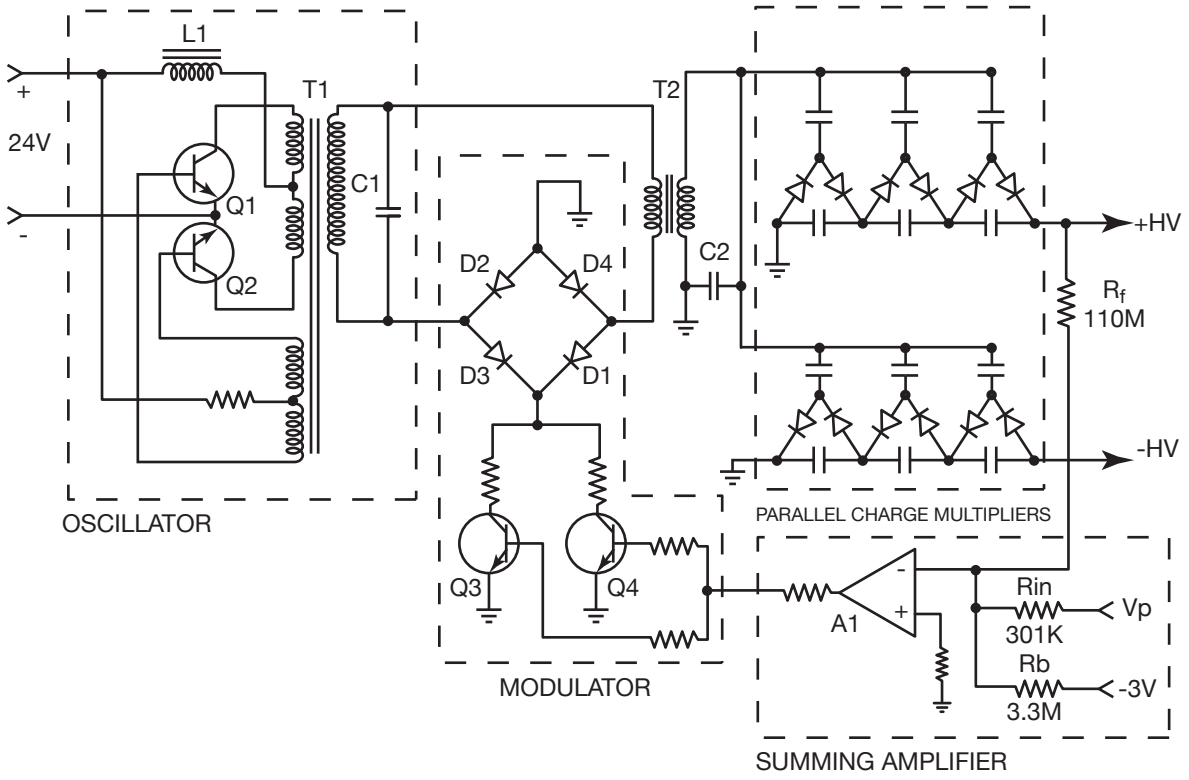

Figure 5 [7.C.5]. Oscillator, modulator, and parallel charge multipliers.

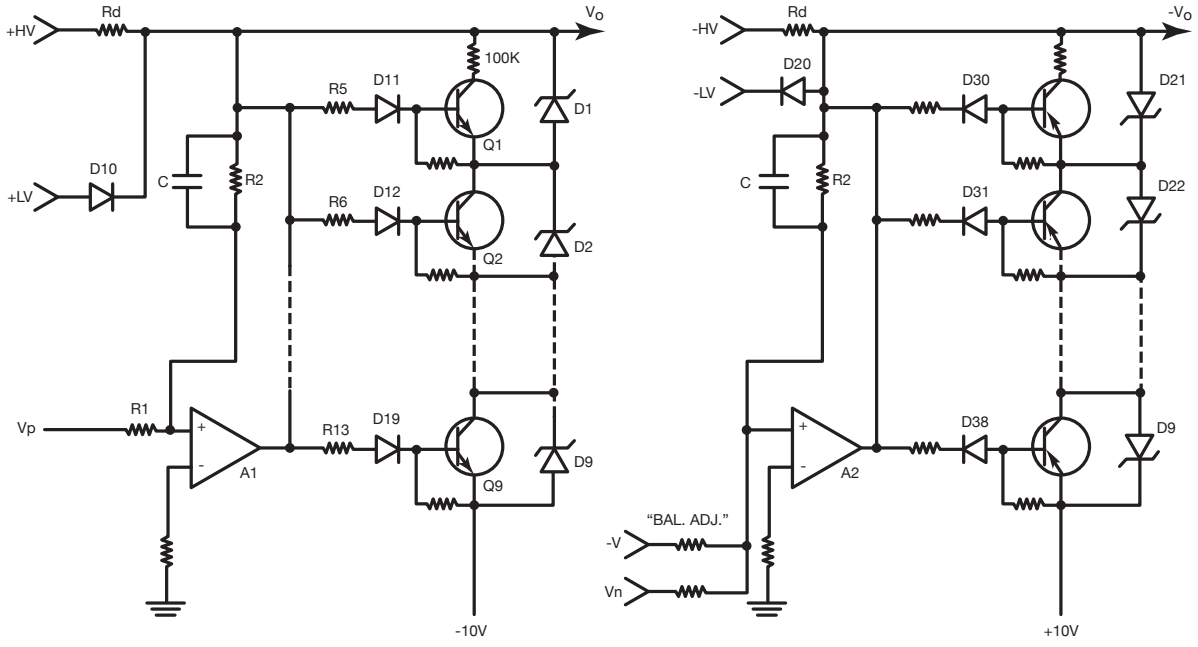

Figure 6 [7.C.6]. High voltage DC shunt regulators.

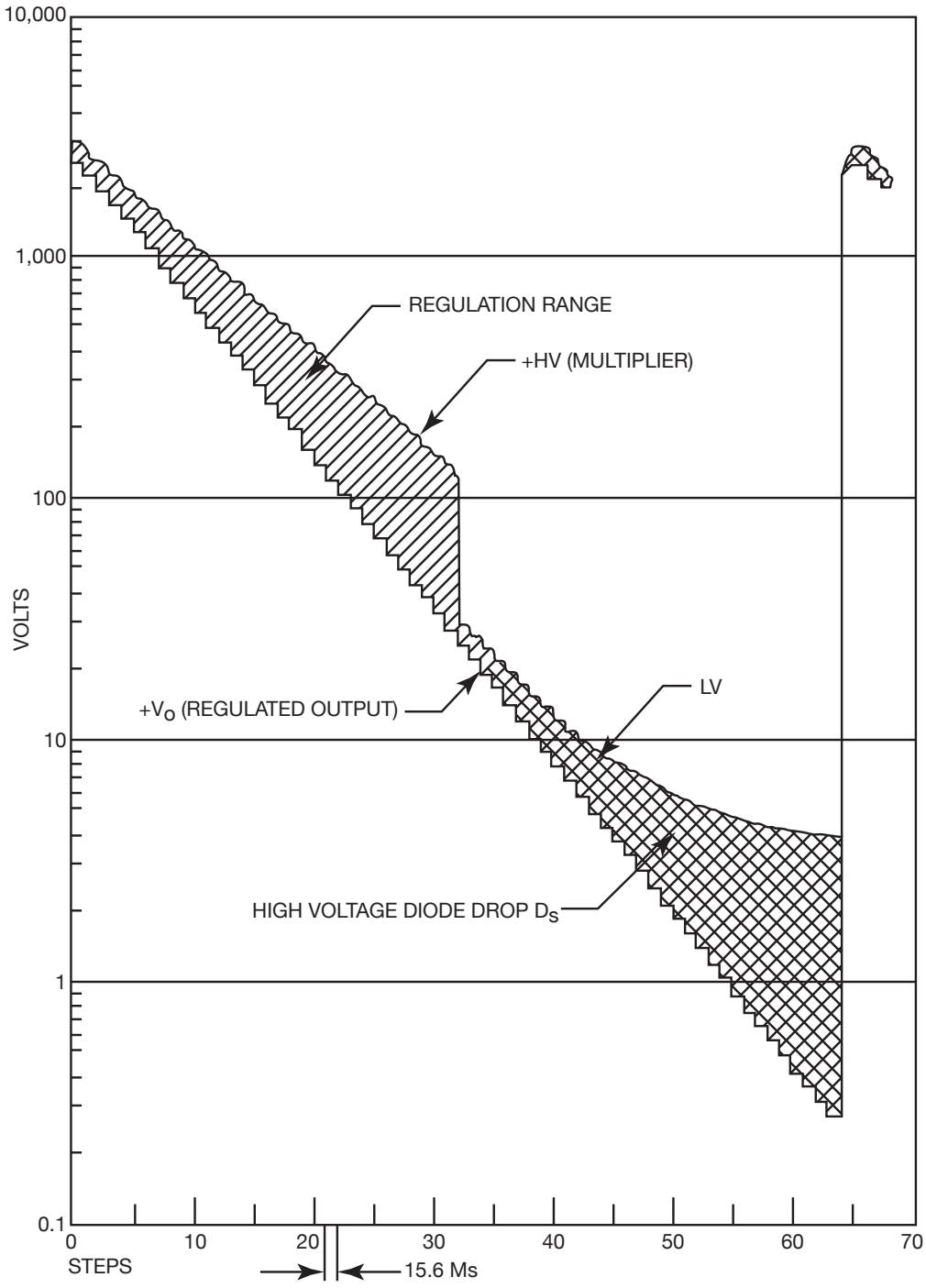

Figure 7 [7.C.7]. Multiplier, low level, and regulated outputs.

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2. Peletier, D.P., "A High Performance 4500 Volt Electron Multiplier Bias Supply for Satellite Use," presented to *IEEE Nuclear Sci. Symp.,* Miami, Florida, December 5, 1972.
3. R. Greenburg. Motorola Power Transistor Handbook, Chapter VI

End of Document by H. Doong.

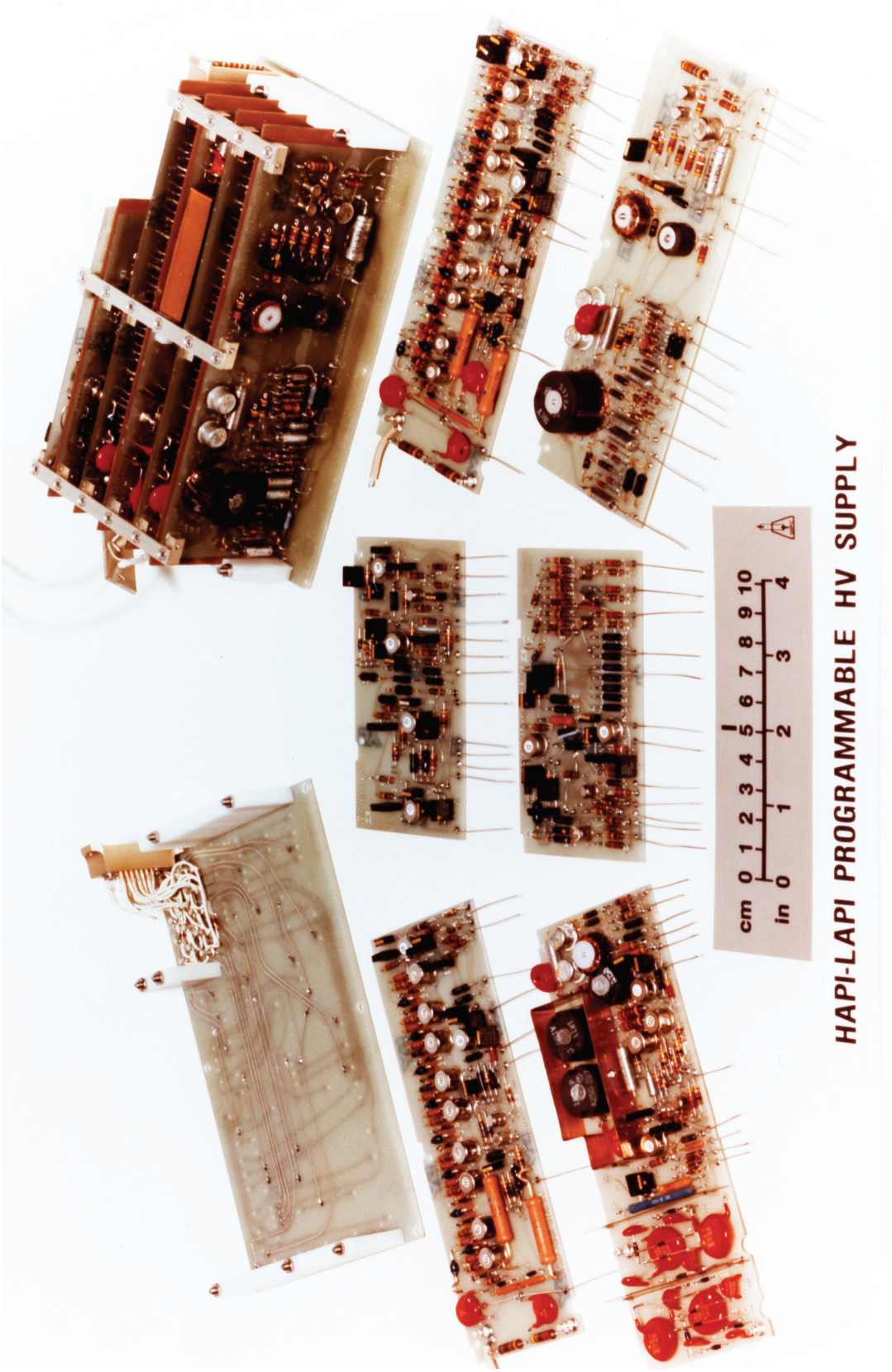

Figure 7.C.8. HAPI-PAPI programmable HV supply.

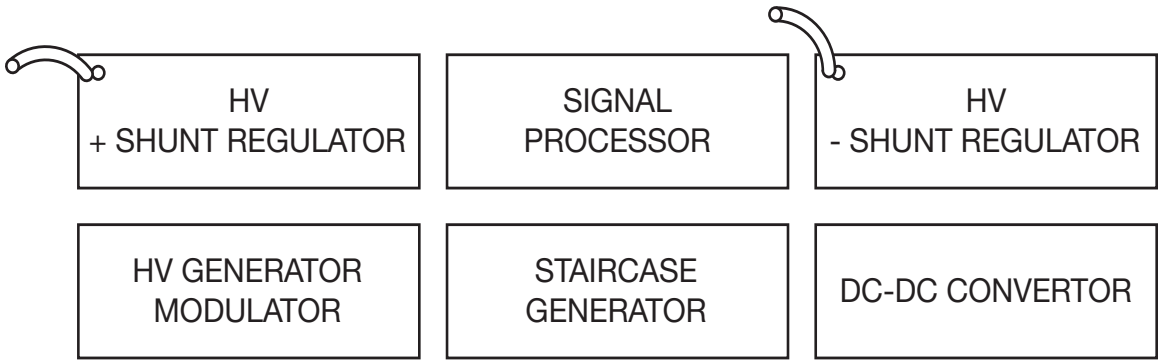

Figure 7.C.9. Identifying the circuit boards in Figure 7.C.8.

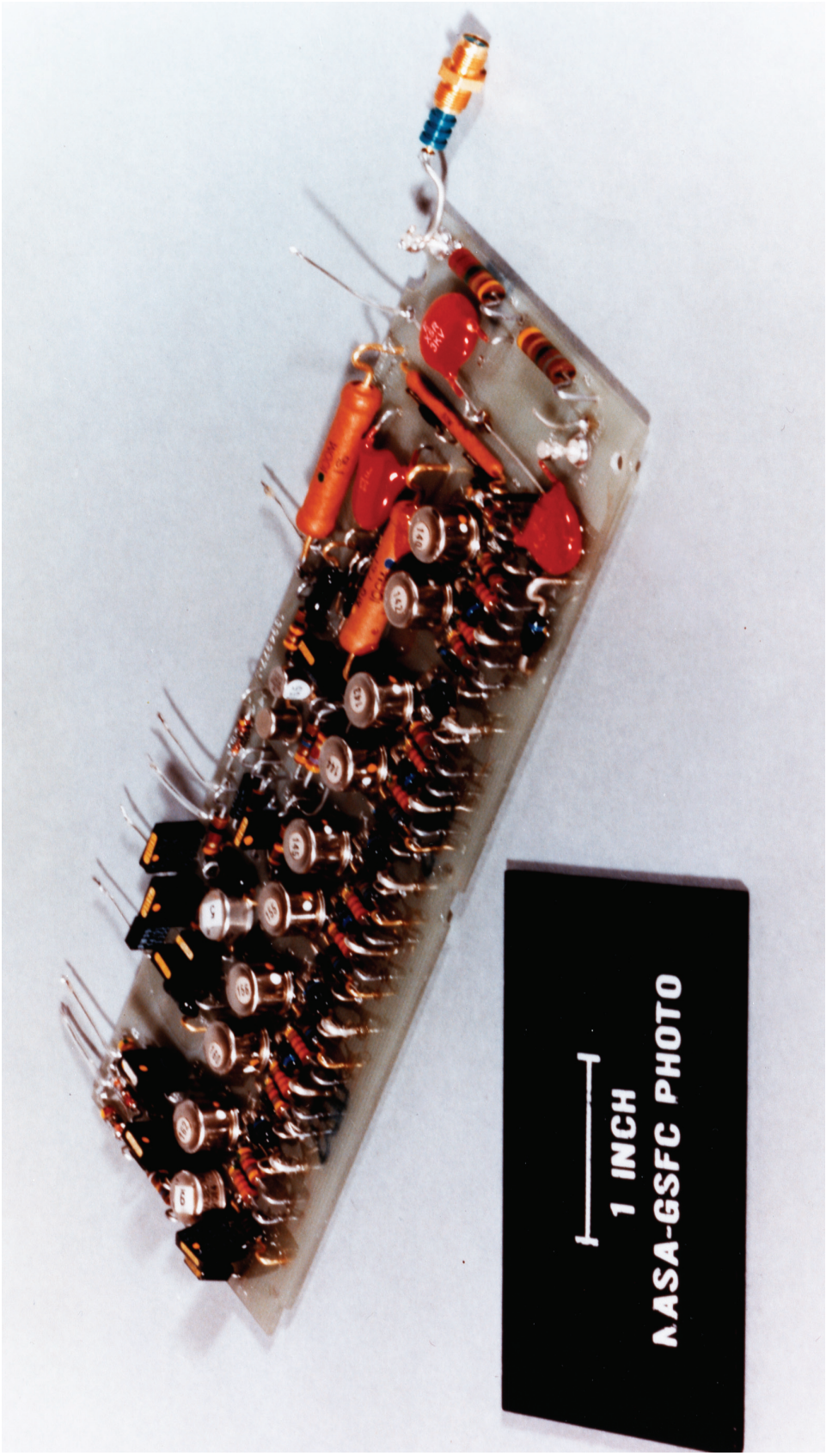

Figure 7.C.10. HV shunt regulator, enlarged.

Comments on HAPI LAPI:

In certain spacecraft, such as HAPI LAPI, DE and ISEE, the particle detectors need *stepped* high voltage power supplies to rapidly change the DC voltage on the detecting plates over 3 or 4 orders of magnitudes. This is done many times during each orbit.

In the HAPI LAPI supply presented here the speedy stepping occurs on the decrease of V_{out}. In other words, it takes 20 ms to reach maximum V_{out}, and then decreases at the faster rate of 300 V/ms.

In Figs. 1 and 6 [Figs. 7.C.1 and 7.C.6, respectively], as shown on the previous pages, the high voltage DC shunt regulators are actually 9 transistors each, to obtain a 9 x 300 V or 2700 V capability each. The output load is about 50 to 100 pF capacitance.

To get a wide V_{out} range, the lower voltage steps are derived from +LV and –LV low voltage supplies while the high voltage is turned off. This occurs between V_{out} equal to 0.3 to 10 V.

To ensure the high speed of downward stepping, the HV DC shunt regulators were *not* potted, but only conformal coated and staked. The dielectric constant k_e of the potting would reduce the speed of stepping by a factor of k_e. Also the k_e distorts the wave shapes. The coating was applied by spraying, not brushing. The parts were spot-staked.

This supply had no capability of changing polarity. It also was quite large in physical size.

By contrast, the ISTP stepping supply of 1993, has to go + and – on each output; also the output voltage has to be ±5 kV on each output, or twice that of HAPI LAPI. Furthermore, ISTP has to step fast on increasing voltage, as well as decreasing, at 500 V/ms; therefore, a new version of shunt regulator is being used, namely Optocouplers, instead of varying conductivity of transistors (Fig. 7.C.11).

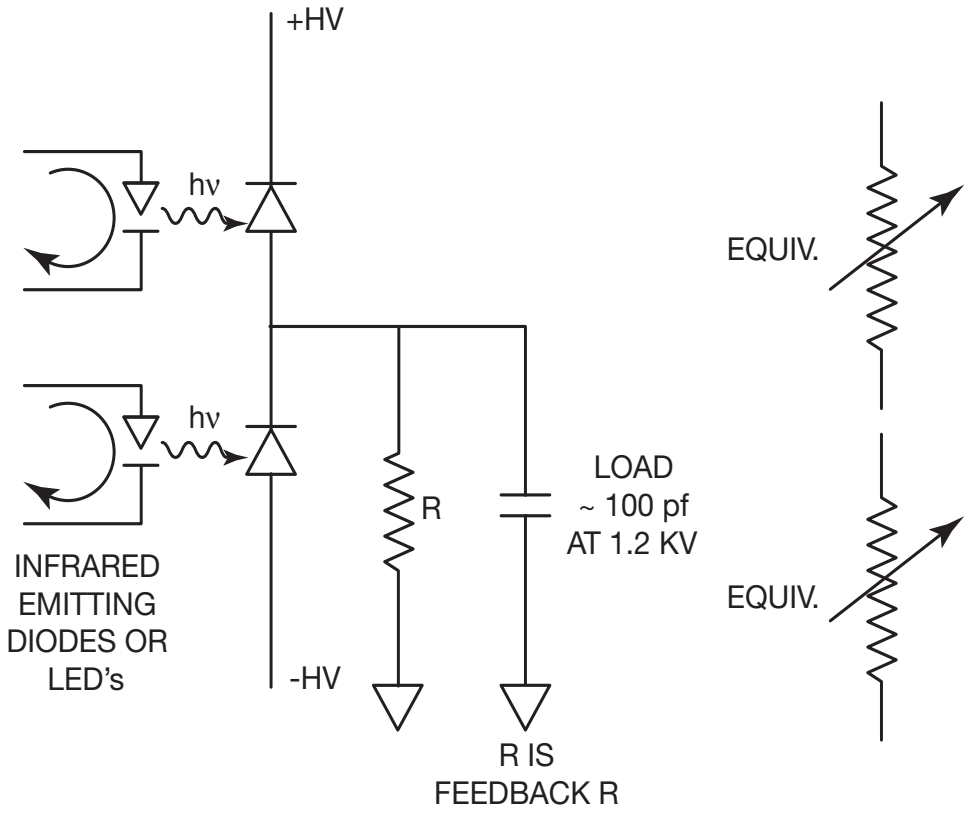

Figure 7.C.11. Basic optocoupler concept.

The Optocoupler uses infrared diodes to shine light. The reverse bias leakage current of a second set of high voltage diodes is enhanced when infrared light is shed on them. High voltage diodes such as 15 kV diodes of sufficient peak inverse voltage (PIV) rating should be used. Diodes of the worst switching times are best for this application (developed in Germany, and used by Jim Van Diver at the Univ. of New Hampshire). The LEDs were bonded to the HV diodes with Uralane 5753 and the resin acted as a light pipe and enhanced the effect, rather than weakened it by light absorption. Of course, the LEDs require power, that is 200 mA peak at 3 or 4 V.

Whereas originally, technical information on optocouplers products was obtainable from Hewlett Packard Co., at this time, Micropac Industries, Inc. is one of the suppliers of Optocouplers.

Again, just as in HAPI LAPI, the supply must only be coated, to maintain speed of voltage change. At a possible voltage difference here of 10 kV maximum, this presents problems. Meticulous cleanliness and excellent adhesion is required.

DESIGN EXAMPLE D

–30 kV DC Power Supply for the Charge, Energy, and Mass (CHEM) experiment on the Active Magnetospheric Particle Tracer Explorer (AMPTE, also called "Ulysses") mission. Space Physics Group, Department of Physics, Univ. of Maryland, College Park, Maryland 20742.

An interesting –30 kV DC power supply was built by the University of Maryland for the CHEM experiment on the AMPTE project. It had several AC voltages riding on the –30 kV DC, such as ±1 kV AC pk-pk. This supply was almost bare, not potted and not conformal coated, with exception of one transformer discussed further on. The high vacuum of space was relied upon as insulator during the mission, and in order to obtain and maintain this high vacuum within the shielding box, these things were done: (1) one month of outgassing before turn-on in orbit; (2) large, screened-over vent hole in the shielding box; and (3) use of low vapor pressure parts and materials—avoidance, as far as possible, of polymer coatings.

In Fig. 7.D.1 (photo) of five figures, the transformer shown on the right-hand side, on the underside of the board, is the pot-core transformer (output of l000–l500 V, pk-pk) in a cylindrical aluminum shielding can. This output gets multiplied by the HV multiplier stack. In Figs. 7.D.1 and 7.D.4, the large transformer on the left-hand side is the transformer for the "smaller" AC voltages. This transformer is also at –30 kV DC with respect to "ground," and therefore, has to be of physically larger dimensions to try to prevent corona to ground. In the background of Fig. 7.D.1, the cylindrical insulating liner can be seen, containing the longitudinal rails upon which the entire circuit board rides. The metallic cylindrical shield goes around it. On several of the photos, the "field smoothers" or "hoops" are seen. Another term for these could be corona rings or corona doughnuts.

Figure 7.D.2 is a closer view of the HV multiplier stack. Note that the multilayer ceramic capacitors (Johansen) are not coated and have no lead wires. They are soldered to rectangular short trails on the G-30 circuit board, 20 mils up from the board with SM 63 solder at 600°F. In other words, before soldering, a 20 mil shim is slipped under the capacitor lying flat, to be later removed. The capacitors thus ride on 20 mil high stilts of solder which serve as a thermomechanical stress relief between the capacitor's ceramic and the polyimide circuit board. Also, the 20 mil gap helps the outgassing. The diodes in the HV stack were Semtech SS4710.

Figures 7.D.3 and 7.D.4 show the other side of the circuit board. In Fig. 7.D.3, the resistors are seen to be mounted up, off the board; they are Victoreen MOX type. They are spot-bonded in the middle to the board, with very low vapor pressure material, Chemglaze Z004 (or could be Epon 934).

Figure 7.D.4 shows the circular High Voltage transformer on the left, having several high voltage outputs. The transformer wire was bought from Phelps-Dodge with Polythermaleze 2000 magnet wire insulation. The particular transformer shown here was in addition coated with a Parylene coating of 1 or 2 mil thickness. This coating was *not successful* on the particular serial number shown here; it is seen to have bad adhesion and is peeling. The Parylene later was made to adhere in other serial numbers. On the right-hand side of Fig. 7.D.4, one can see, around the threaded golden screw hole, the pads for the pins of the output connector to ride on. This is a custom designed, special connector by the Univ. of Maryland. Figure 7.D.5 shows an outside view of it.

Cleaning of the circuit board was done with hot ethyl alcohol, but *not* the transformers. All screws/screw holes were vented to prevent corona from forming in the dead-end holes under the screws. This power supply was tested for 3 or 4 weeks, continuously in high vacuum, with thermal cycling from –45°C to + 45°C. In summary, this type of bare construction on a –30 kV DC power supply requires great care in handling, meticulous cleanliness, and long vacuum testing.

Nearly identical versions of the –30 kV DC power supply described above were flown as integral portions of time-of-flight (TOF) ion composition spectrometers designed to measure plasma composition and energy spectra in various

space environments. These TOF instruments were flown successfully on AMPTE (launched August 1984), Ulysses (launched October 1990), Wind (launched November 1994), and ACE (launched August 1997). After an outgassing period of four to six weeks following launch, the –30 kV supplies were slowly ramped up to operating voltage over a period of about five to seven days. Operation voltage was typically –23 to –28 kV. The AMPTE instrument (Gloeckler et al., 1985) and its –30 kV supply operated flawlessly until the end of mission, about four years after launch. The –30 kV supply of the TOF instrument (Gloeckler et al., 1995) on the Wind Spacecraft was of a slightly modified design. It operated initially at –23 kV and later at –28 kV until May 27, 2000 when a reset of the instrument Data Processing Unit occurred and the instrument ceased to operate. The Ulysses (Gloeckler et al., 1992) and ACE (Gloeckler et al., 1998) TOF instruments (the Solar Wind Ion Composition Spectrometers, or SWICSs) have been operating flawlessly since turn on. Currently, the Ulysses instrument is at –24 kV and the ACE at –26 kV. To the best of our knowledge, none of the –30 kV supplies described here and developed and flown by the Maryland Space Physics Group have failed. Together, these –30 kV supplies have, as of April 2005, a combined flawless record of operation of 31 years and 9 months.

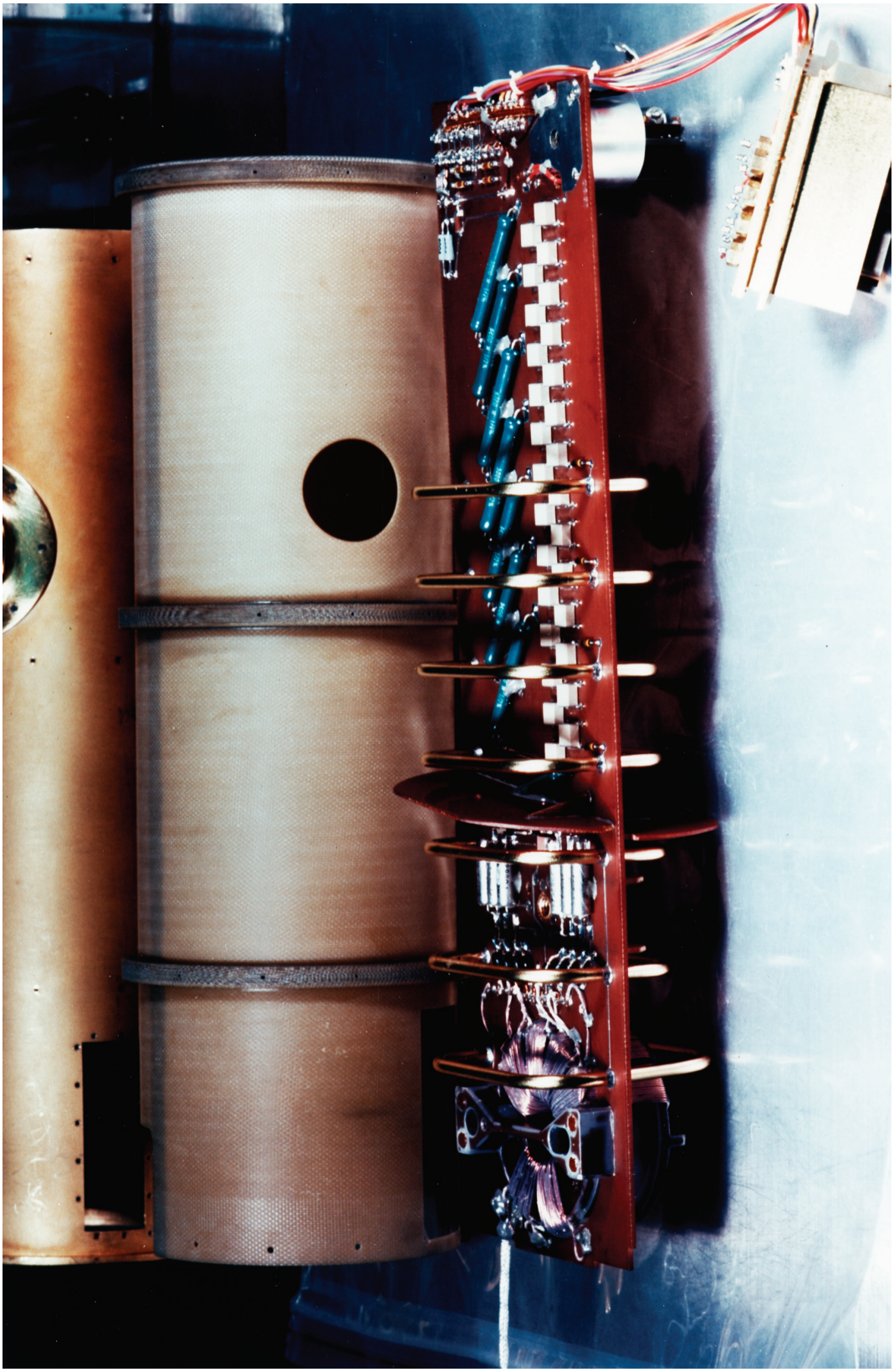

Figure 7.D.1

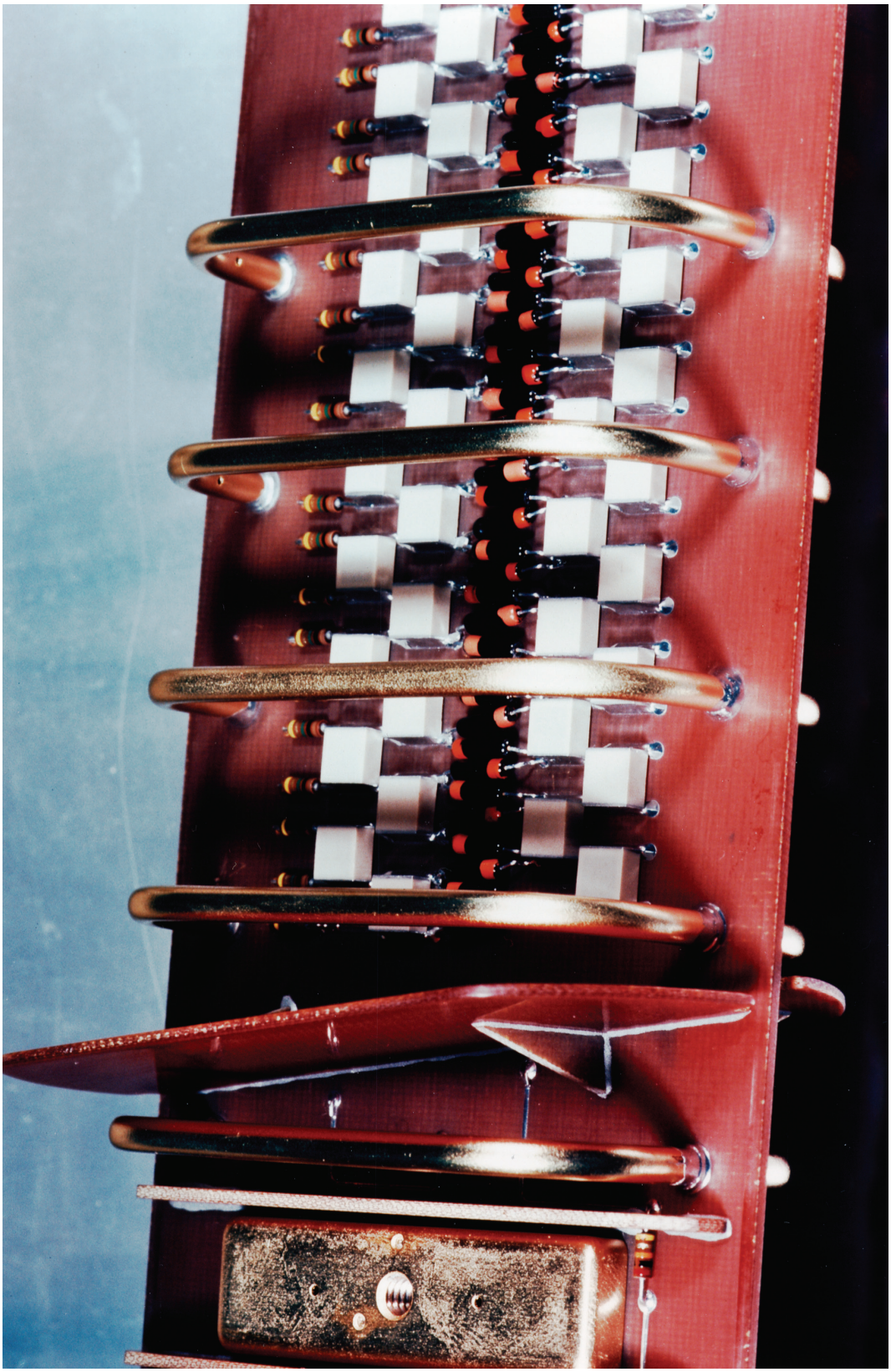

Figure 7.D.2

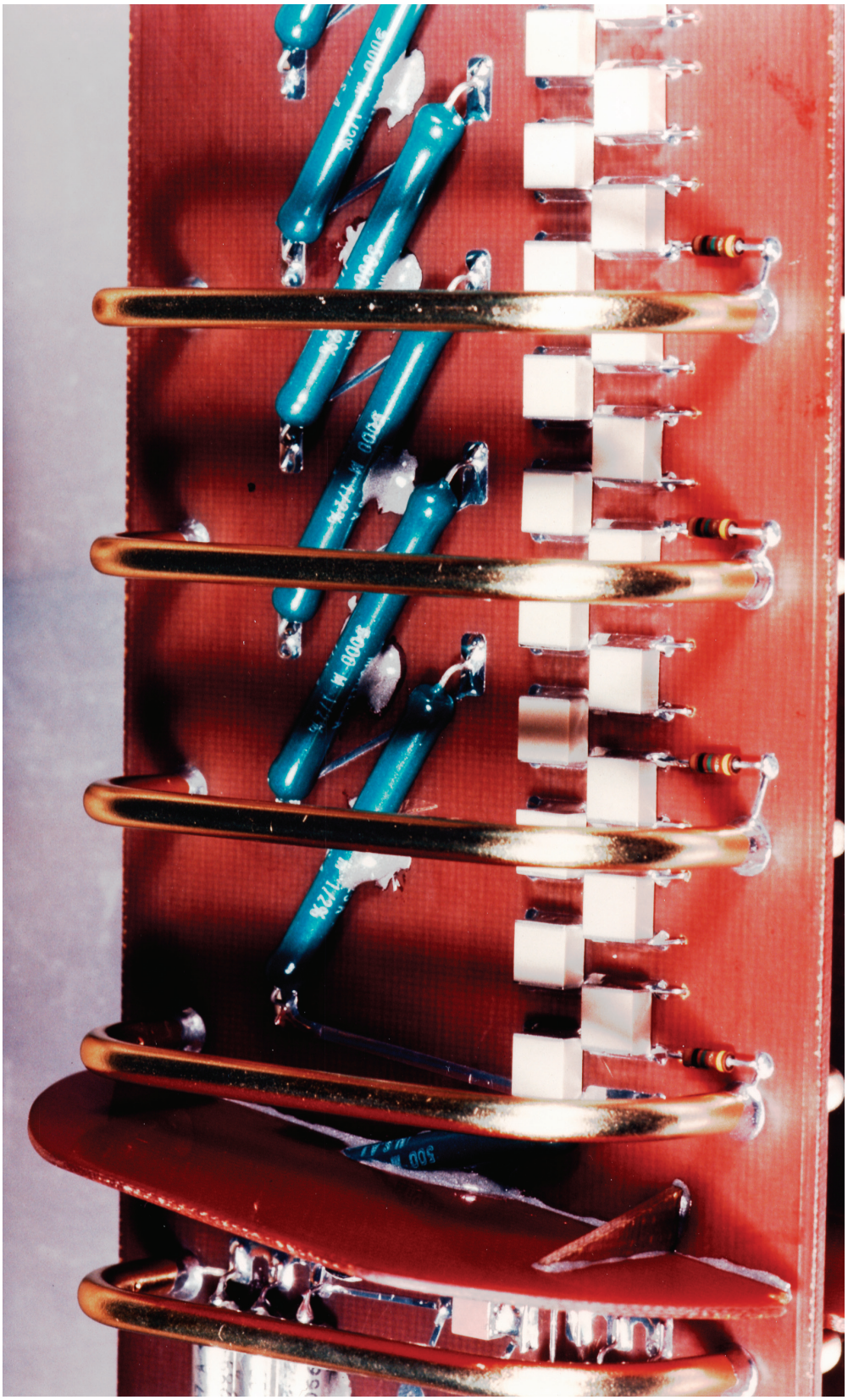

Figure 7.D.3

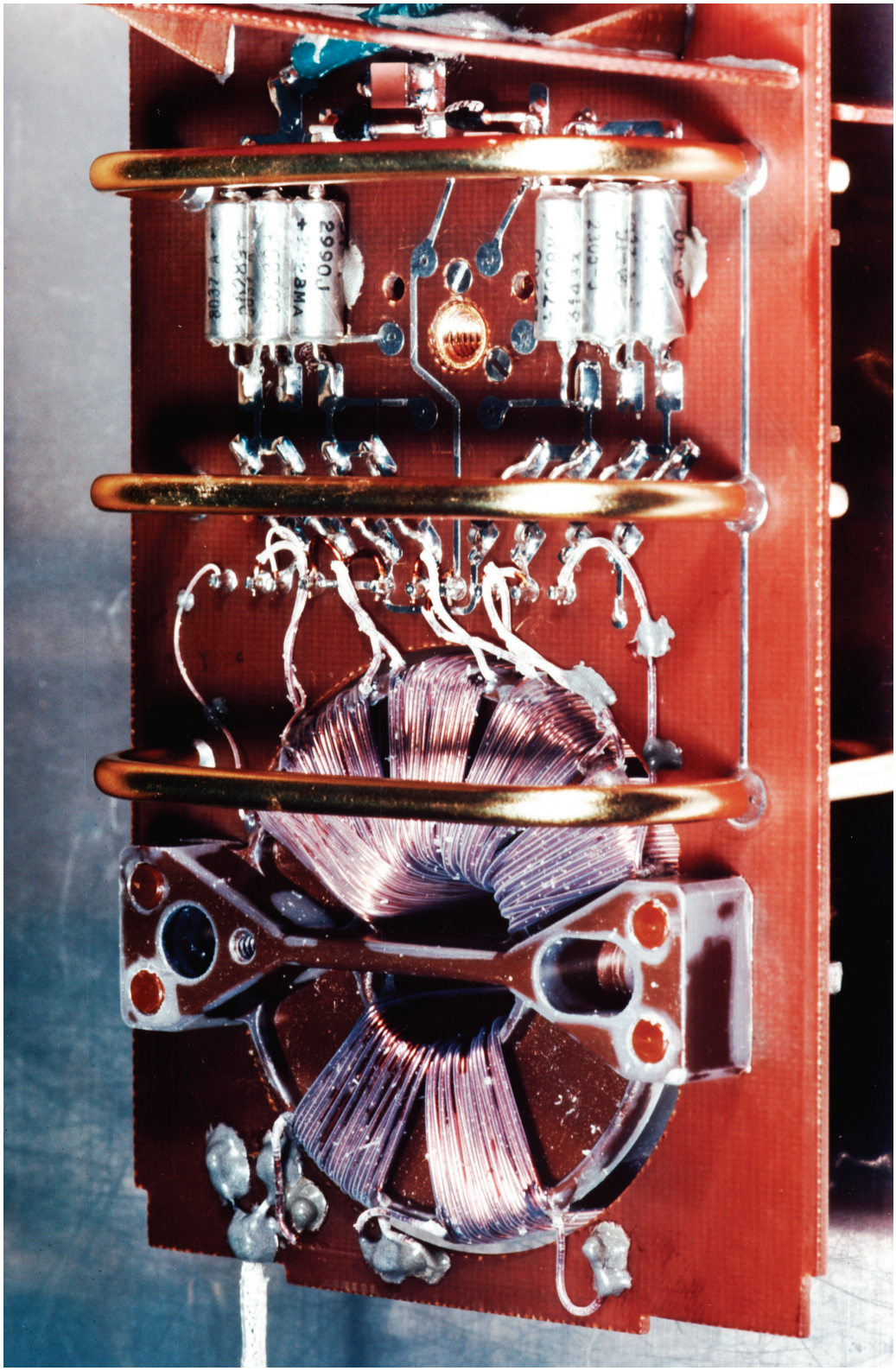

Figure 7.D.4

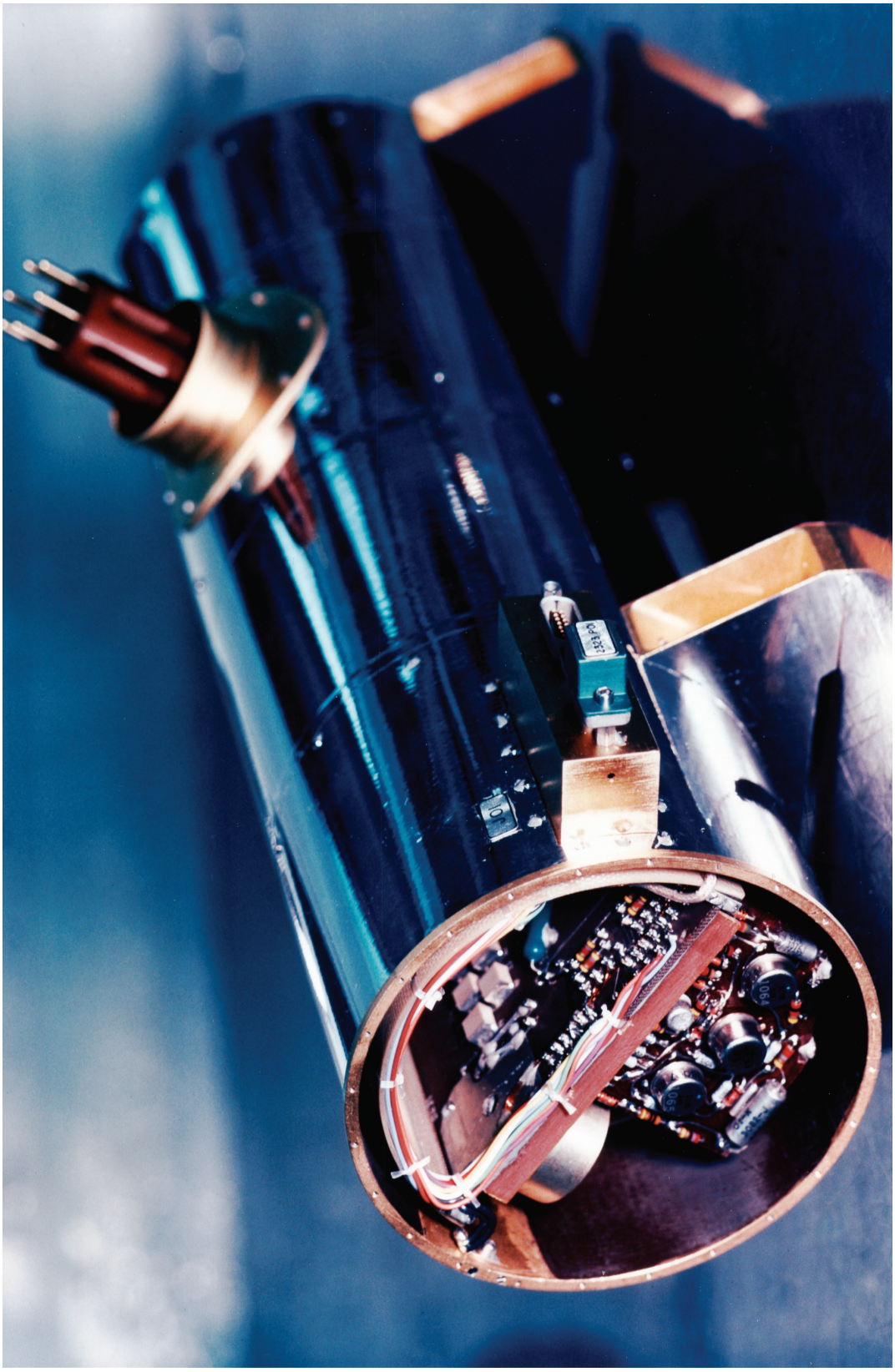

Figure 7.D.5

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DESIGN EXAMPLE E

A commercial, –700 V power supply. BBXRT Project, Short Mission, by, Renate S. Bever, NASA/GSFC.

If the mission duration lasts only a short time, such as one week on a shuttle flight, or a rocket flight, some project offices have recommended certain commercial small power supplies. They are already internally solid-potted and can then be modified either at the output or at the input terminals to meet required specifications.

In the lower half of Figs. 7.E.2 and 7.E.3 is a Velonex Company solid-potted power supply, variable from –300 to –700 V DC by means of a small accessible variac screw at the top of the housing. Next to the Velonex supply sits a circuit board at the output end, with high voltage capacitors and resistors to serve two purposes: (1) slow application of voltage to the instrument, about 20 s rise-time, and (2) filtering. All this is mounted in a rectangular shielding box approximate size 6.5 in x 2.5 in, to be primed and solid-potted.

Several new experiences were gained here:

(1) It had to be roughed on the five surfaces (not the top) with 400 grade emery paper and well-primed with PR 420 before potting with Conathane EN-11, all to enhance adhesion.
(2) Thermal analysis had shown that EN-11 did not have sufficient thermal conductivity to remove the heat from the Velonex supply buried in the potting compound. Therefore, powdered Cho-therm was added to some EN-ll, and the Velonex supply pasted with a thin layer of this mix to the bottom of the shielding box *before* the general potting. This then enhanced good thermal conduction to the outside shielding box.
(3) The output cable from the Velonex supply was polyethylene, which does not adhere well to EN-ll. It had to be roughed up and primed, as well as the other circuit components primed before potting by vacuum pouring with EN-ll, just below the level of the top of the Velonex supply.
(4) After the Project office decided on the output voltage, (first specified as –500 V, but after one year determined to have to be –700 V), the variable screw at the top was fixed with a few drops of EN-ll.
(5) The output was by means of a *female* Reynolds series 600 connector on a cable pigtail. The *male* Reynolds bulkhead connector is much more difficult for obtaining good adhesion.

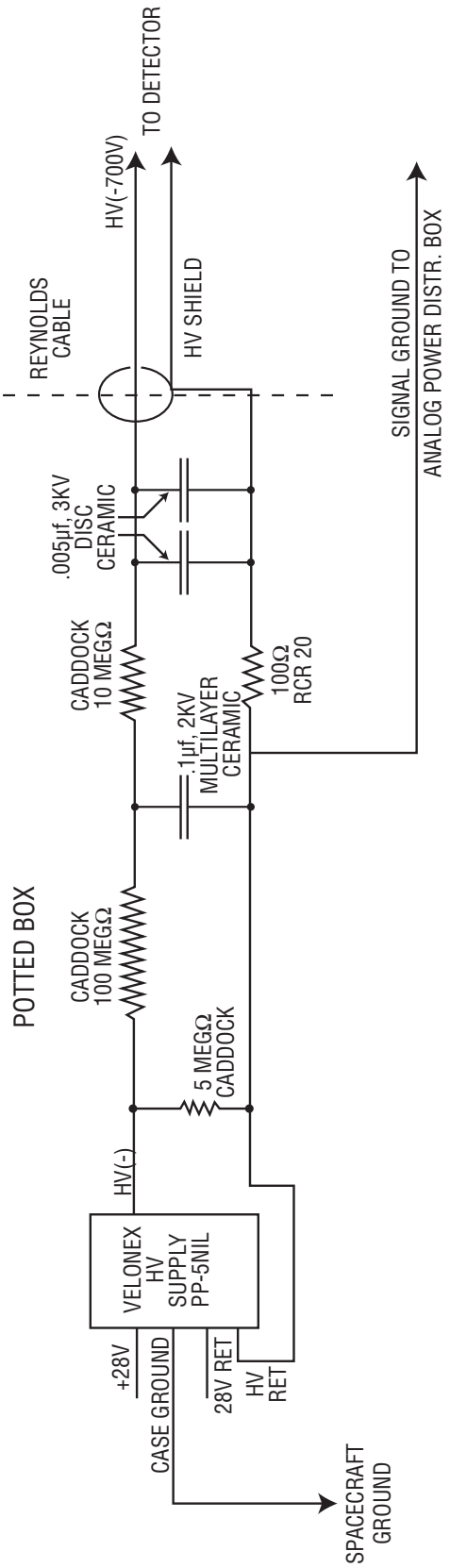


Figure 7.E.1. Velonex supply; filtering and grounding externally.

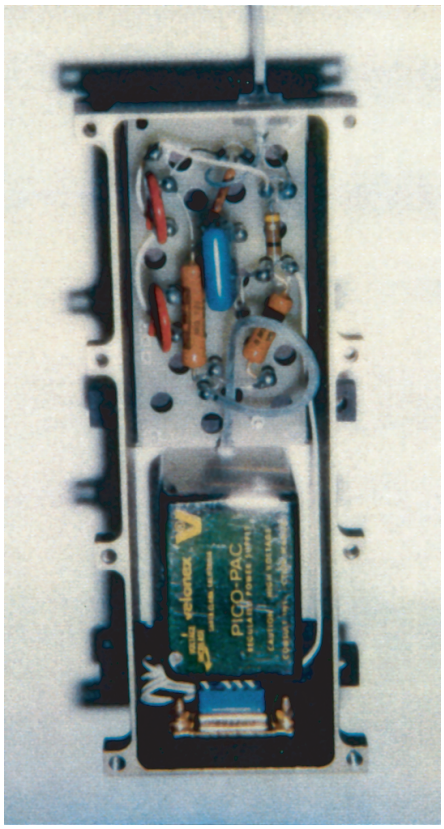


Figure 7.E.2. BBXRT supply before potting.

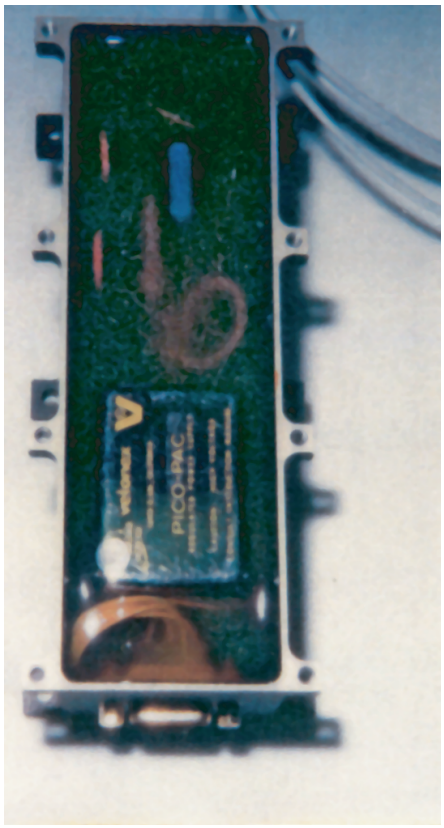


Figure 7.E.3. BBXRT supply after potting.

DESIGN EXAMPLE F

A 3–5 kV, also 1.3 kV High Voltage power supply for the EGRET/GRO project. Design Engineer: Arthur Ruitberg, GSFC, Code 563.

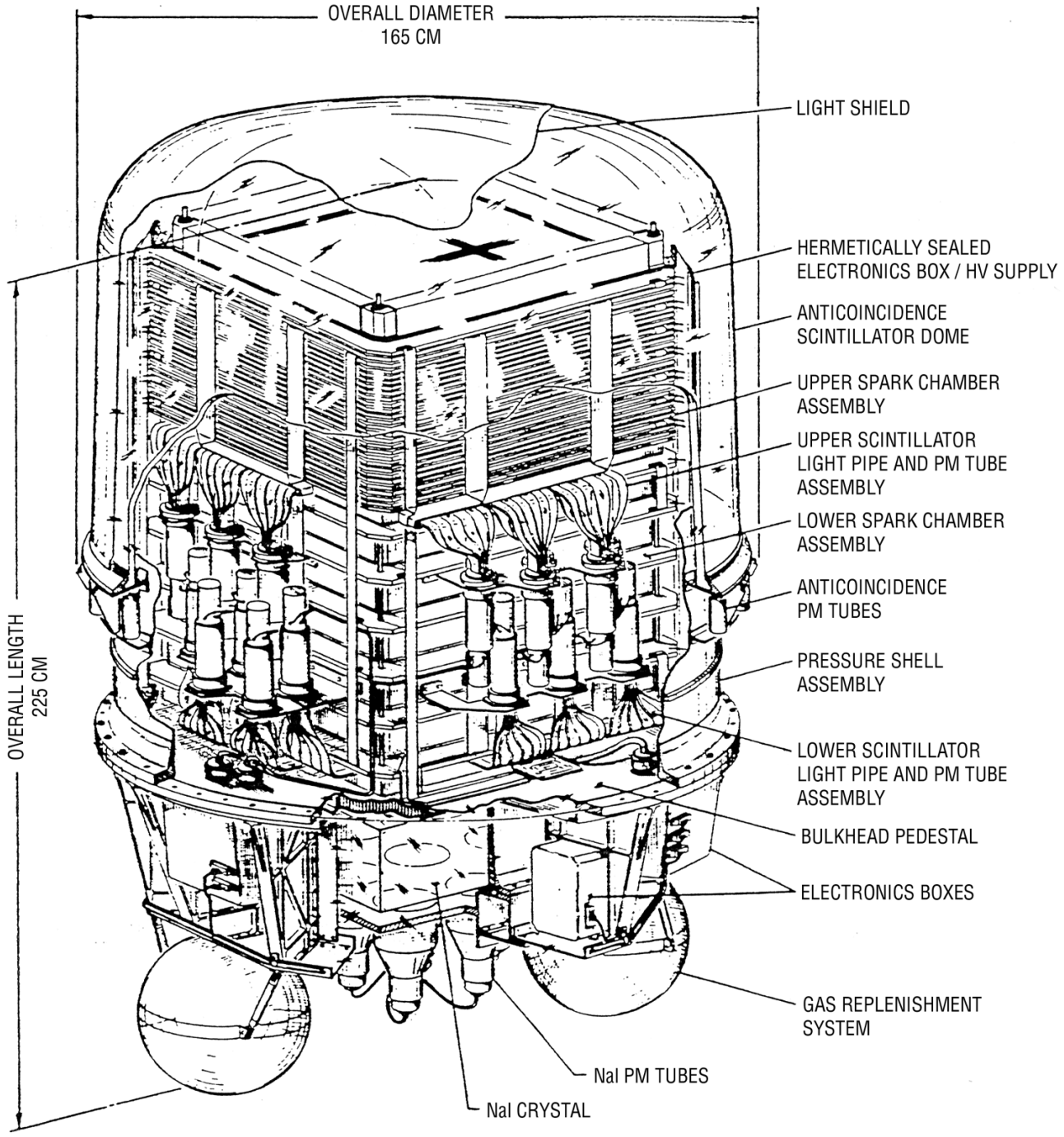


Figure 7.F.1. EGRET Spark Chamber (PM=PhotoMultiplier).

The EGRET Spark Chamber high voltage power supply has really two high voltage supplies in it, as can be seen on the circuit schematic:

(1) The Spark Chamber Supply giving between 3–5 kV output and taking over 50 ms to restore the output voltage after a spark.
(2) A separate 1300 volt generator: The Spark Chamber supply works on a fly-back transformer design. The fly-back transformer is T_1 with a 1:10 turns ratio. The controlling amount of energy is in T_l; when transistor Q_3 is turned off, the negative current in the primary of T_l continues. The low voltage portion is a Jensen oscillator with transformer T_3 controlling the frequency.

The high voltage portions of this power supply were solid potted with EN-ll polyurethane as seen in the Figure 7.F.8 photograph, below the "cut end" of the photo. This was *in addition* to the fact that the entire high voltage power supply for the EGRET Spark Chamber was pressurized at more than atmospheric pressure (probably with dry nitrogen gas). In case pressurization would be lost, that way the power supply would still function, even when the pressure would drop through the dangerous "corona region."

Please note that Figure 7.F.2 actually has two power supplies on it: the bottom, righthand part of the page is the 1.3 kV supply. The other three-fourths of the page is the 3–5 kV supply (originally to be 2–4 kV).

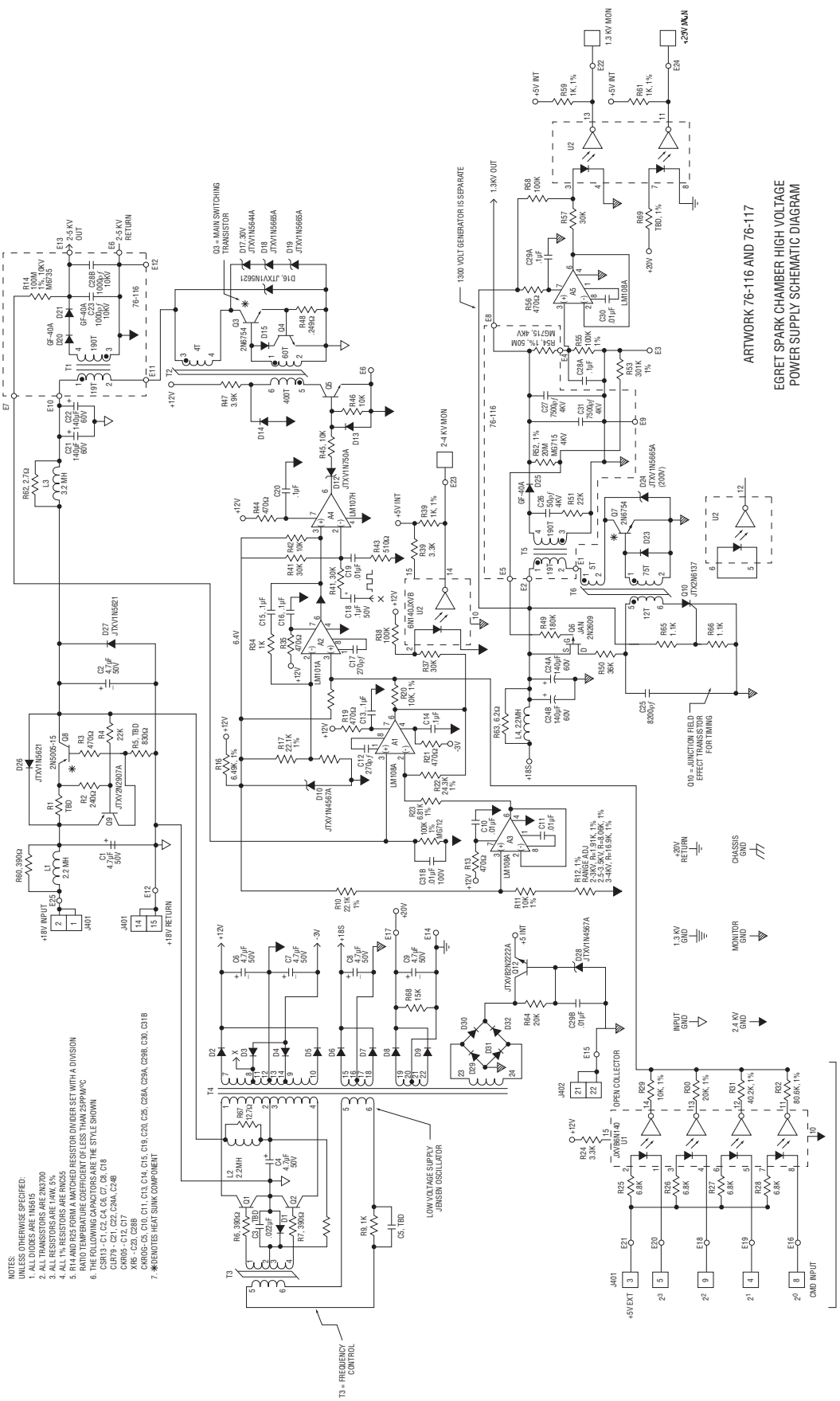


Figure 7.F.2. EGRET Spark Chamber high voltage power supply schematic diagram.

Controlling amount of energy is in T_1; when Q_3 is turned off, then the negative current in the primary continues.

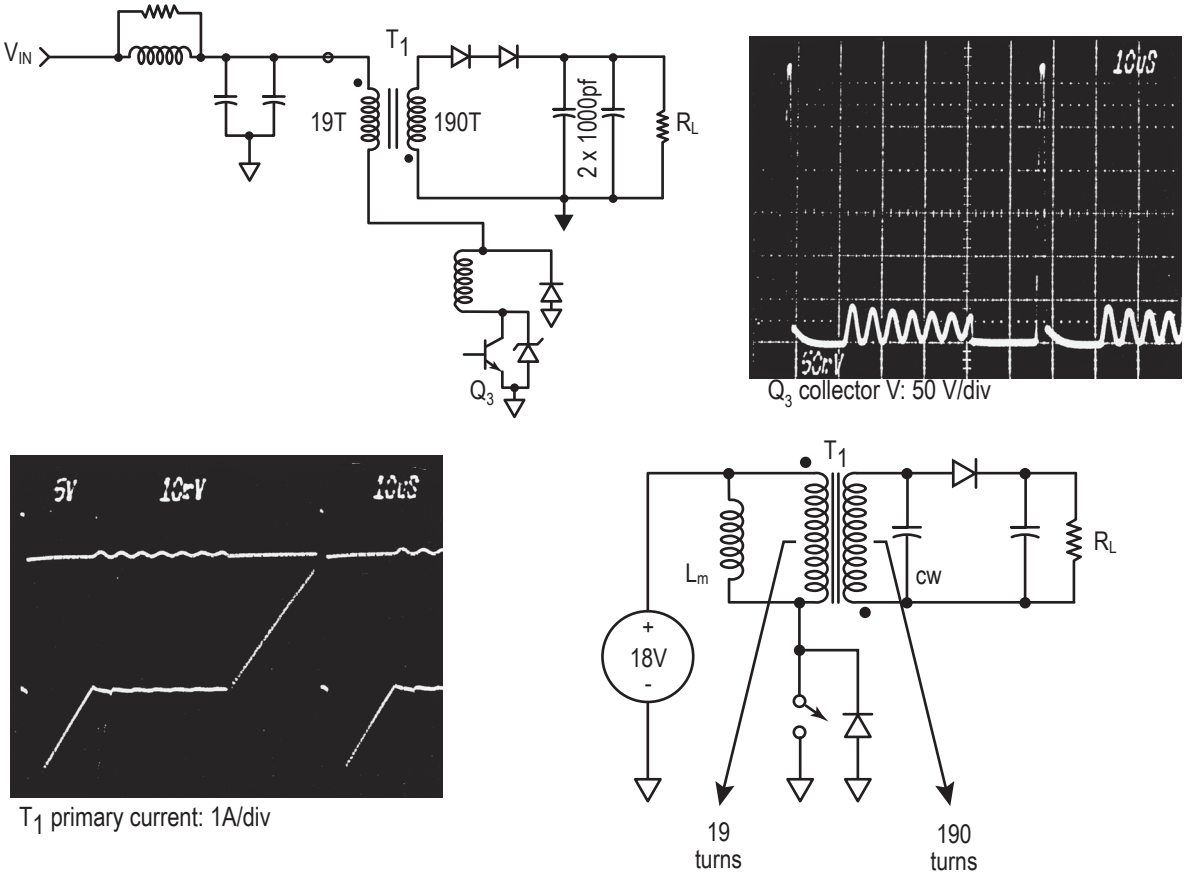


Figure 7.F.3. Power transformer parasitic capacitance is the “heart” of the circuit as in Figure 7.F.2.

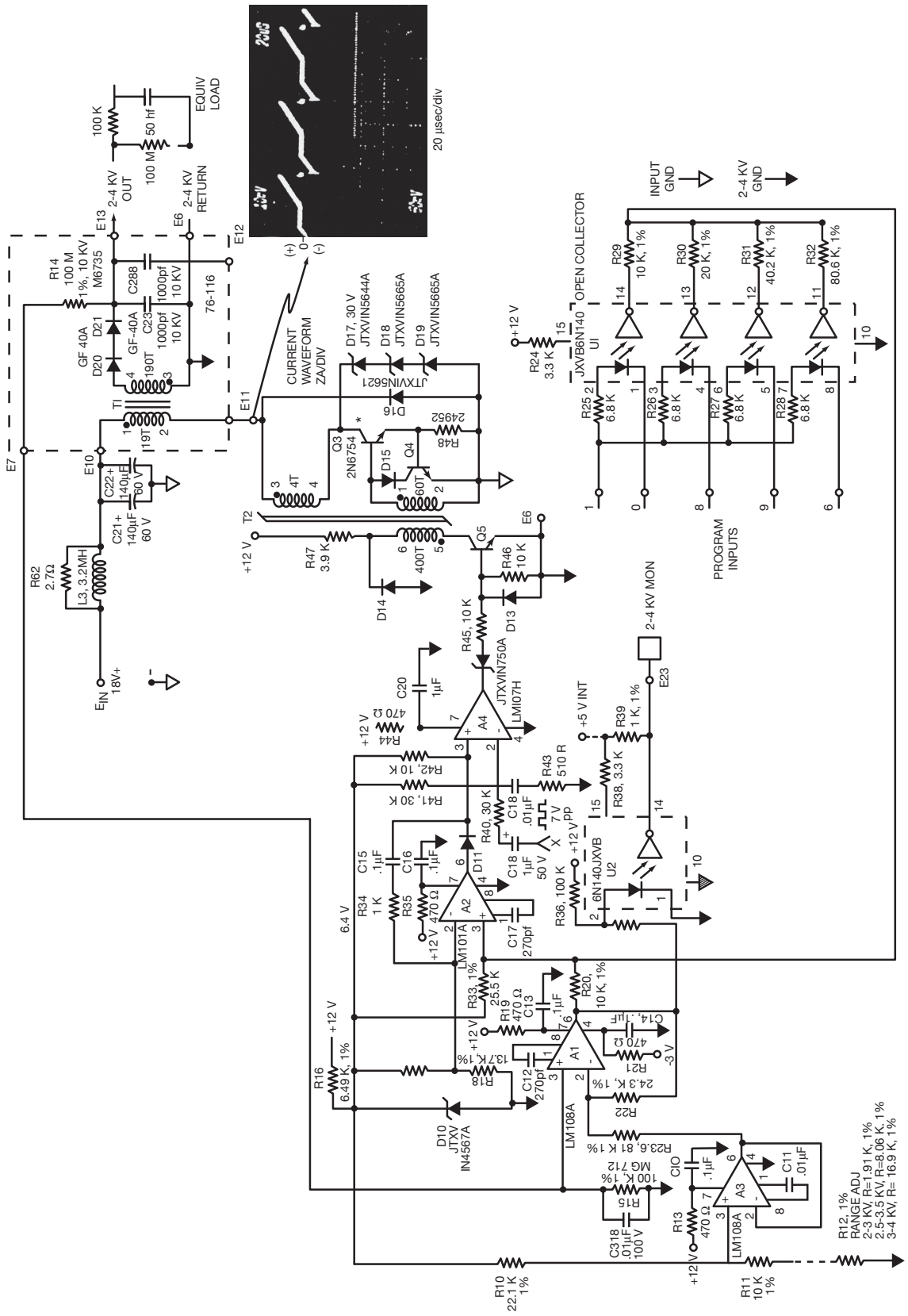


Figure 7.F.4. Control loop; detail of Figure 7.F.2.

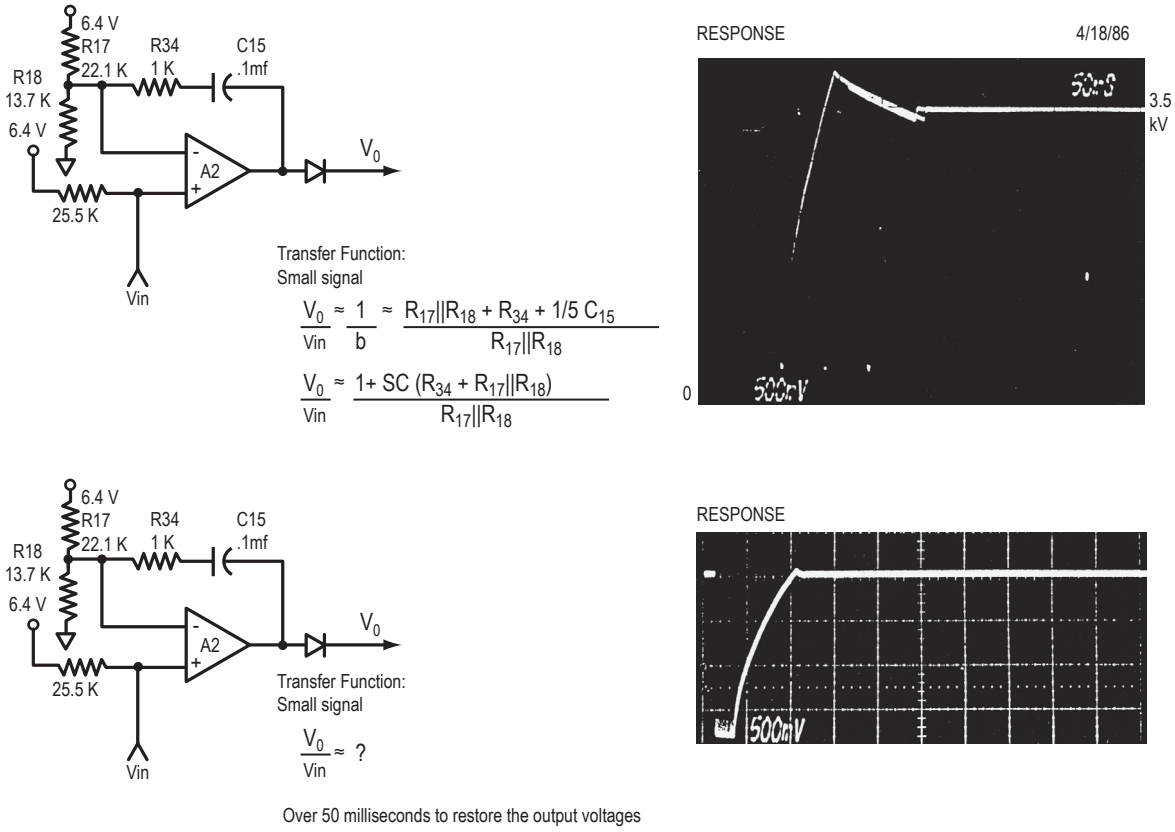


Figure 7.F.5. Integrator Performance versus Ability to Calculate.

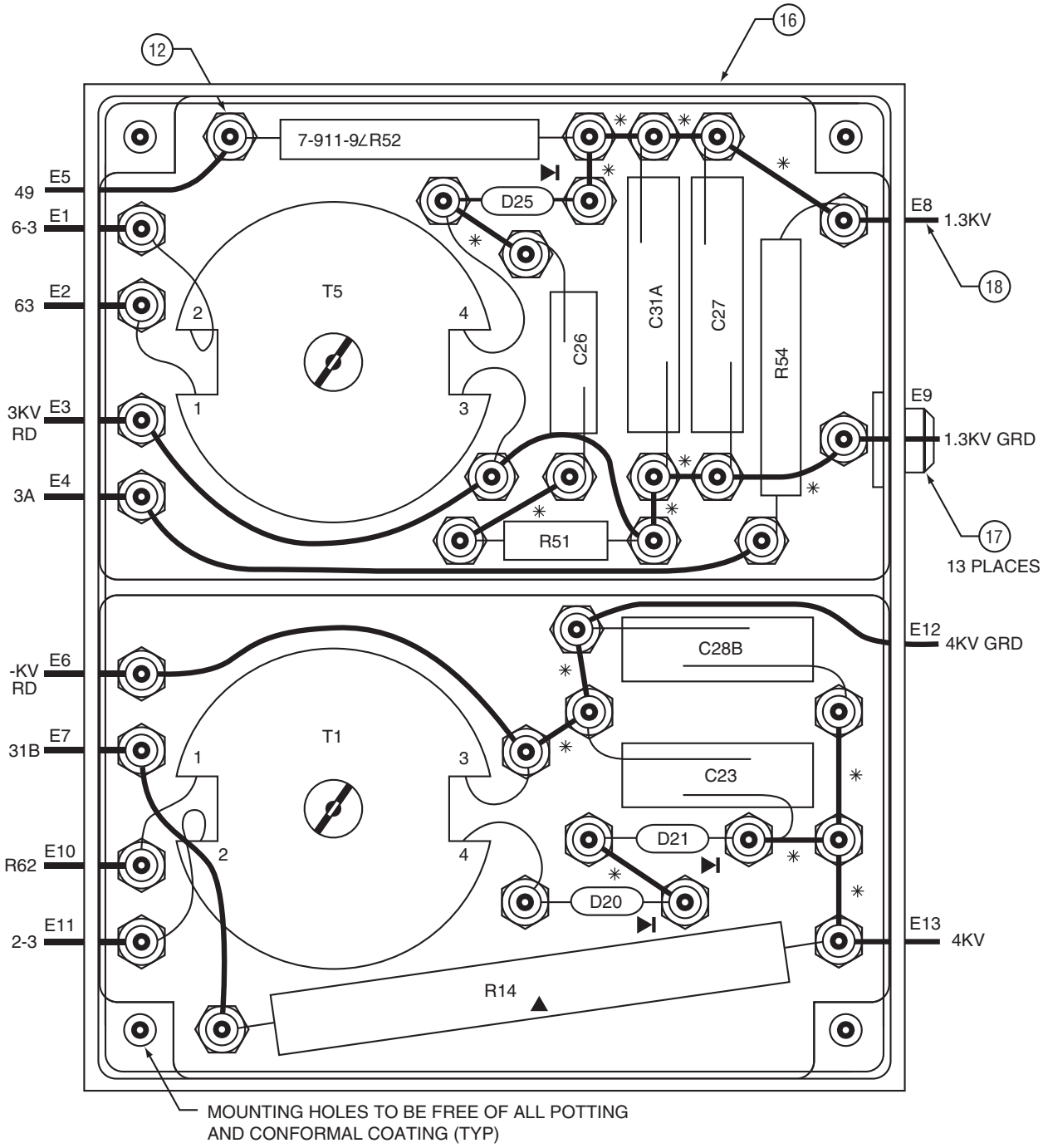


Figure 7.F.6. HV layout, i.e., top of Figure 7.F.7.

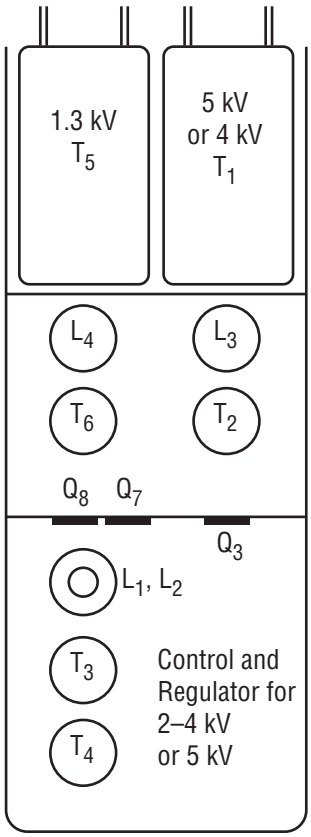


Figure 7.F.7. Identifying major parts of the layout.

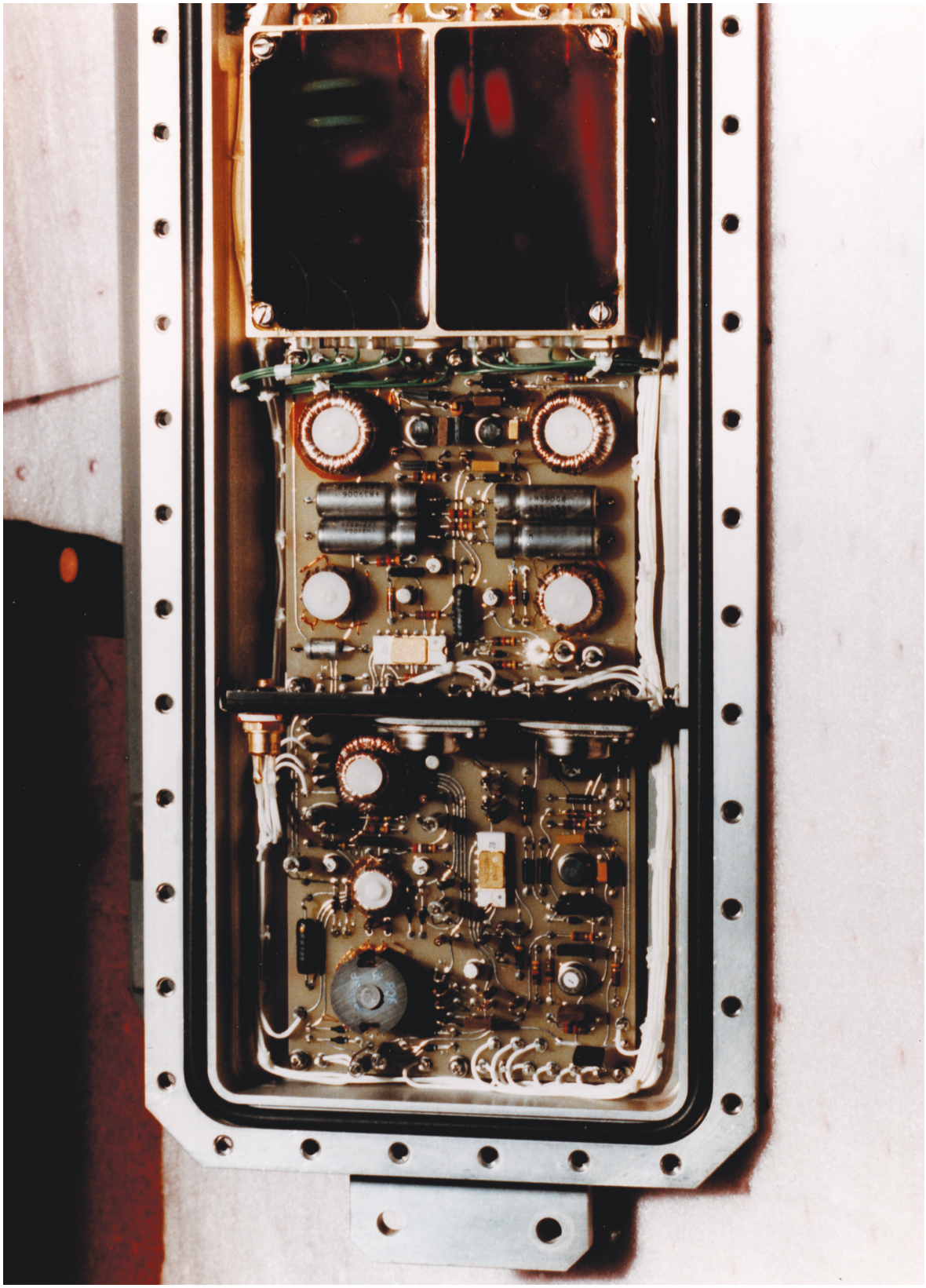


Figure 7.F.8. Photograph of EGRET HV supply.

DESIGN EXAMPLE G

XTE/PCA High Voltage Power Supply (really two power supplies to about 2200 V and 2900 V, Design Engineer: Karen Castell-Stewart, NASA/GSFC

FEATURES

- Two independent, isolated high voltage power supplies packaged in one box.
- Each output is programmable (with 4 bits) to 16 voltage levels.
- An additional bit command the output on or off.
- Xenon Output: 980 V unregulated; 1910 V–2190 V regulated, 20 V steps.
- Propane Output: 1430 V unregulated; 2580 V–2860 V regulated, 20 V steps.
- Output Voltage Regulation: ±0.2% over temperature and input voltage variations.
- Output Ripple and Noise: <1m V p-p over temperature and input voltage variations.
- Operating Temperature Range: –10°C to +40°C.
- Isolation: The input and output power returns shall be isolated from each other and the chassis.
- Transient Response: <4% overshoot to worst case step command with a time duration of <400 ms.
- Slow Turn On: Upon turn on, the output shall rise in >100 ms to prevent damage to the detectors.
- Control Loop: In the event that the control loop opens, a second, passive loop shall prevent the output voltage from exceeding the maximum step voltage.
- Output Voltage Monitoring: A telemetry readout shall provide a –5 V to +5 V output, proportional to the high voltage; that applies to the upper 8 and lower 8 settings independently.
- Short Circuit Protection: The supplies must limit the output current in the case of a short applied to the output.

This spacecraft flies through the South Atlantic Anomaly (SAA) again and again.

In this region over the Southern Atlantic Ocean, the Earth's magnetic field is abnormally large, and thus, there is an abnormal concentration of high energy particles or a radiation belt. To protect the detectors from damage, the high voltage needs to be turned down, hence the detectors off, on every passage through the SAA.

GENERAL DESCRIPTION

The XTE/PCA instrument requires two high voltage sources to bias the wire grids of its x-ray detectors. There is one High Voltage Power Supply (HVPS) box to supply these voltages on each power control unit (PCU). It is located on the PCU bottom cover, in electronic box stack #1. Each HVPS box consists of two high voltage supplies, one for the xenon and one for the propane chamber. The supplies convert the filtered +28 V DC spacecraft bus voltage, from the Remote Interface-Power Supply (RIF-PS), to the regulated, high voltage DC needed for the detectors.

Each supply is individually programmable from a 5-bit command interface. This consists of single bit enable/disable signal and an additional 4 bits that command 16 different output voltage levels. The upper 15 levels (0001-1111) are 20 V apart and the lowest step (0000) is about 1000 V below step (0001). Specifically, the xenon side is capable of producing a 1910–2190 V regulated output, along with the lowest level, a 910 V unregulated output. Similarly, the propane output ranges from 2580–2860 V for the upper 15 levels and 1400 V for the lowest level. This bottom step, called the South Atlantic Anomaly (SAA) response, is intended to protect the detectors from damage as it flies through this radiation belt by lowering the supplied high voltages by about 1000 V. Because the detectors will not be taking data during this time, unregulated power was sufficient.

Another safety feature of the HVPS is the enable/disable bit. It will turn off the high voltage output of the power supply with power still applied to the input. This serves to protect the detector against possible damage from the

high voltage without needing to turn off the power at the HVPS input. (The input power can be turned off as well by signaling a relay on the RIF-PS board. Thus, the high voltage output can be turned off in two different ways and can be turned down with the SAA signal.)

The output enable/disable circuitry is located at the front end of the power supply. As stated above, this is commanded externally by one bit in the command interface. When its level is low, the high voltage supply operates normally. When the level goes high, an optocoupler output shorts a zener diode in the preregulator, bringing the output down to zero. Thus, the high voltage output falls to zero with input power still applied. An optocoupler is used in order to maintain primary to secondary isolation in the PCU.

The board layout and component assembly for both the xenon and propane units was designed to be identical, to increase the efficiency in schedule and budget. Some of the component values differ in order to accomplish the different voltages required. Each assembly consists of a printed circuit board (PCB) and a high voltage assembly, sometimes called the "bathtub." The PCB is a two-sided board on which the low voltage and control circuitry is mounted. The bathtub unit houses all of the high voltage components, except for the high voltage transformer, which is mounted on the PCB. The bathtub compartment is encapsulated with CONAP EN-11 to reduce the risk of partial discharge in areas of high electric field gradient.

CIRCUIT OPERATION

As described, the inputs to each high voltage supply are the +28 V line and 5 digital command bits (command interface) to set the high voltage level. As the +28 V line enters the HVPS, it sees an inrush current limiter, a common mode choke and an input filter. This filtered line then passes through a pre-regulator that brings the voltage down to 20 V DC. This DC voltage appears at the front end of Hartley oscillator, whose output is a 40 V p-p sinusoid. The sinusoidal voltage is seen across the primary winding of a step-up transformer, which increases the AC voltage to about 600 V p-p to 80 V p-p, depending on whether the supply is a xenon or propane.

On the secondary side, the stepped-up sinusoid drives the high voltage section of the power supply. The high voltage is entirely contained on the secondary side of the transformer. Regulation is accomplished by placing two regulating transistors in series with the transformer secondary and the voltage multiplier. In effect, the voltage at the input of the voltage multiplier is adjusted by the regulating transistors. This then determines how much voltage appears at the output. The voltage multiplier is a 4-stage Cockcroft-Walton multiplier, so its output is approximately 4 times the voltage seen at its input. An output filter follows the multiplier and filters this DC high voltage in two stages in order to achieve low noise output. At this point, a high voltage connector supplies the output to the detector through cabling designed for high voltage use.

The high voltage output is divided down within the supply to provide a feedback signal to the feedback and control circuitry. Several operational amplifiers use this error signal, along with a multiplexed signal from the 4 command bits to set the level of the high voltage output. These signals can independently change the conduction of the regulating transistors to adjust the output up or down.

Another feature of the supply is an output voltage monitor which provides a low voltage level output corresponding to the high voltage output. The monitor output is restricted to the range –5 V to +5 V with at least 0.5 V needed between output steps. In actuality, the upper eight levels range from –0.5 V to +5.0 V with 0.7 V between output steps. The lower seven levels are also in this range with the same increment between steps, but the lowest level, the SAA, is about –4.5 V, a value far below the other steps, in order to easily distinguish this output condition from the others.

PACKAGING CONCEPT

The HVPS packaging concept was designed with a modular approach, such that all the high voltage components are contained in a separate, removable unit. This high voltage container, also called the "bathtub" because of its shape,

is installed on top of the PCB with the other, low voltage circuitry, and can be replaced with another bathtub unit if a failure occurs. Thus, rather than having to replace the entire power supply in the case of an integrated design, the modular approach saves most of the supply while allowing replacement of only the high voltage assembly.

The high voltage unit is divided into several compartments. This is to reduce noise coupling between sections and to the output. The first chamber is the voltage multiplier section, which houses a 4-stage Cockcroft-Walton voltage multiplier. These are Maida ceramic X7R capacitors, chosen for their successful space flight history. Additionally, Renate Bever has done extensive testing of these parts. To reduce noise, the AC and DC capacitors where placed on separate boards. The DC side is placed closer to the output in order to reduce cable length. The next two chambers have output filters that reduce the high frequency AC noise. Two stages are needed to meet the ripple requirement of <lmVp-p. A large series resistor in the second filter section provides short circuit protection in the event of a short in the load. Because the transformer secondary winding is *not* in the high voltage section its HV winding had to be wrapped in Kapton. The leads, where they come out, were coated and staked. Also, special attention had to be paid to the parts in the HV Regulation portion of the circuit. The output connector is a Reynolds series 167-3771 connector rated for 10 kV. The last section contains two Caddock high voltage resistors that divide down the high voltage for the feedback control loop.

The entire high voltage enclosure is made of Noryl, which exhibits excellent insulating properties, but is very rigid, and therefore, difficult to machine. It is also a lightweight material. The outside shielding is done with copper tape with conductive adhesive. (Experiments were done with depositing aluminum coating on the Noryl, but the long term adhesion was not good.) The shields separating the compartments are made of copper-clad epoxy, which are all connected to signal ground.

The weight budget on XTE/PCA allowed for the encapsulation of the high voltage assembly. The encapsulant chosen was CONAP EN-11, based on recommendations by Art Ruitberg and Renate Bever.

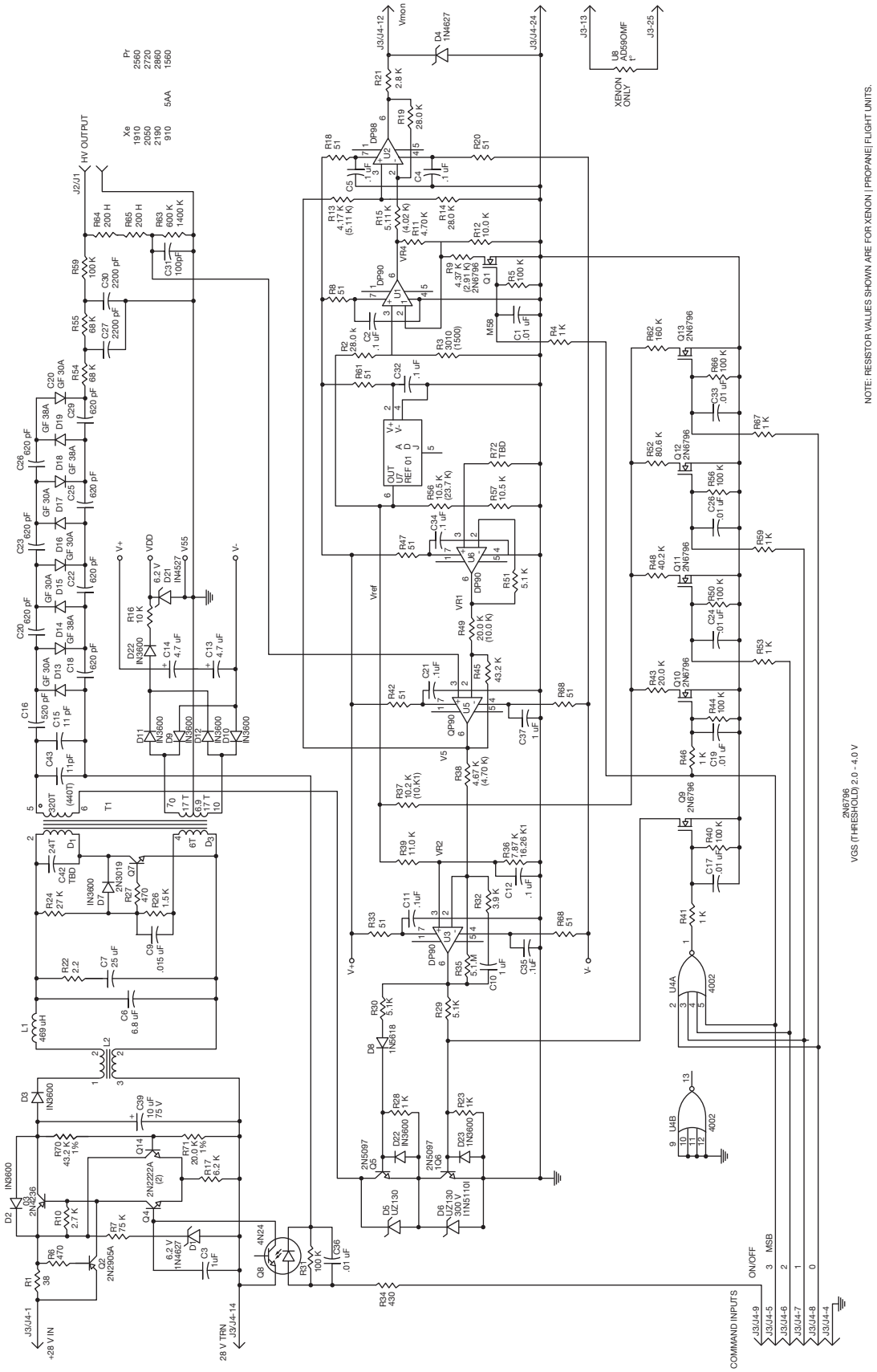

HV OUTPUT
J2/J1
Pr
2560
2720
2860
1560
Xe
1910
2050
2190
910
5AA
J3/J4-12
Vmon
J3/J4-24
J3-13
J3-25
XENON ONLY
U8 AD590MF
NOTE: RESISTOR VALUES SHOWN ARE FOR XENON | PROPANE| FLIGHT UNITS.
2N6796
VGS (THRESHOLD) 2.0 - 4.0 V
+28 V IN
J3/J4-1
28 V TRN
J3/J4-14
COMMAND INPUTS
ON/OFF
MSB
J3/J4-9
J3/J4-5
J3/J4-6
J3/J4-7
J3/J4-8
J3/J4-4
Vref
V+
V-

Figure 7.G.1.

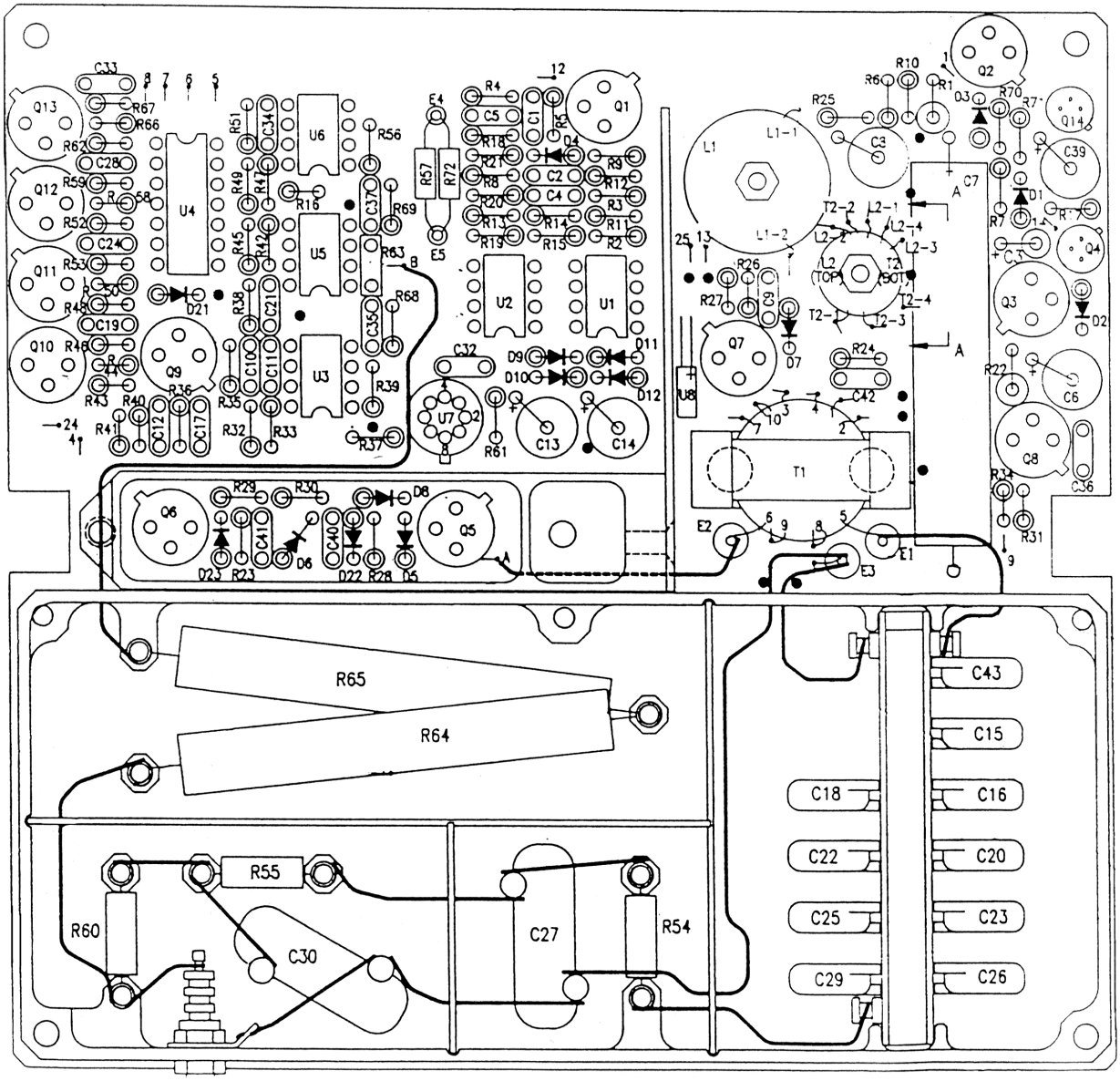


Figure 7.G.2. High voltage before potting (lower half of figure).

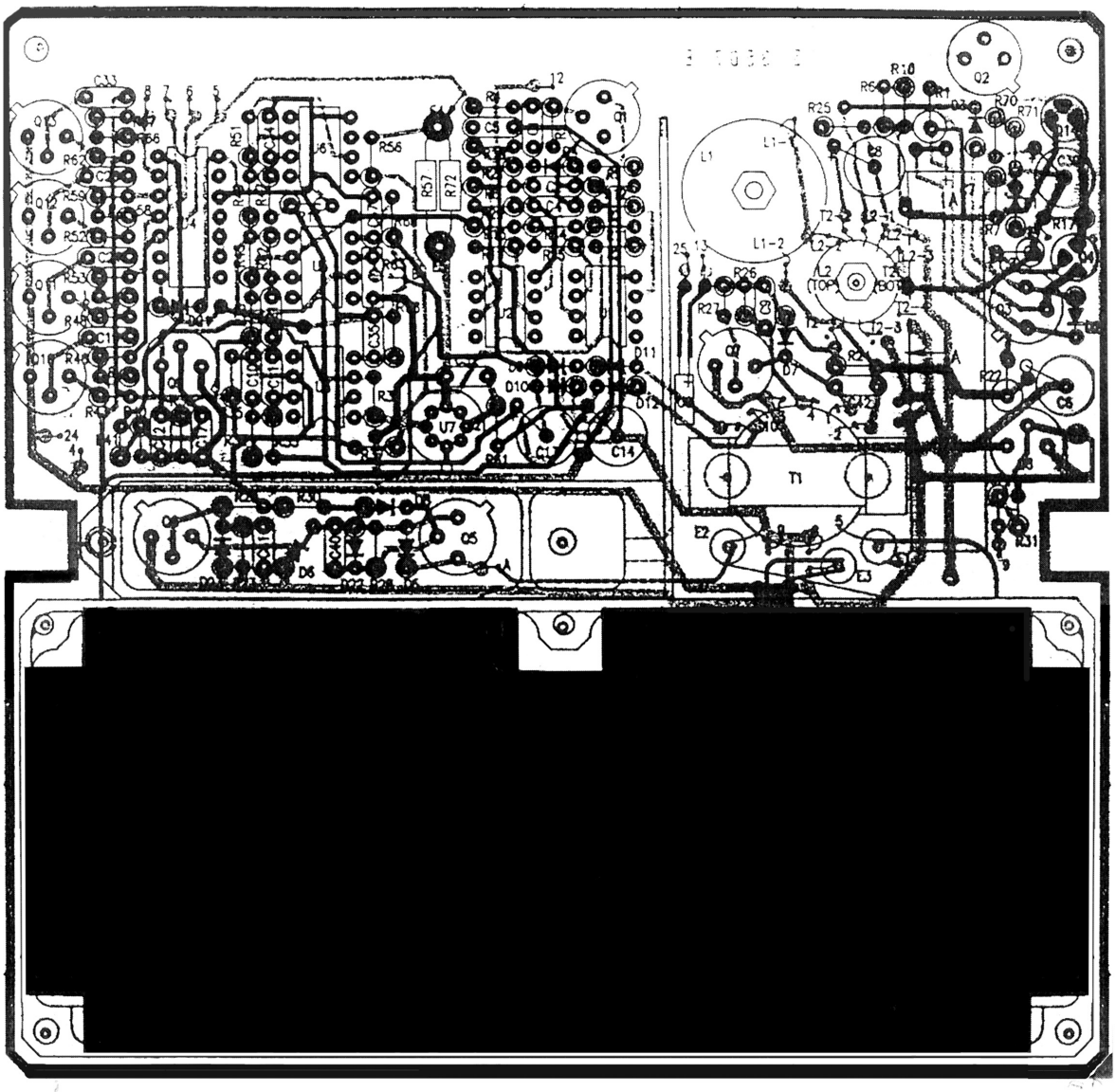


Figure 7.G.3. High voltage after potting (lower half of figure).

DESIGN EXAMPLE H

Cassini/CAPS: –16 kV and +16 kV High Voltage Power Supply. Modular Construction. Design Engineer: Arthur Ruitberg, NASA/GSFC

REQUIREMENT SUMMARY

- Two outputs, linearly controlled by separate eight bit command:
  (1) 0 to +16 kV
  (2) 0 to –16 kV
- DC regulation: 1%, ripple: < .01%
- Third output for mcp controlled +1.2 kV above negative output
- Operates from +30 V s/c bus, oscillators lock to 100 kHz input sync signal, 2.25 W available
- Qualification temperature range: –35 to +45°C
- Size: 8” x 6” x 1.9”, Weight: 1.24 kg
- Radiation level: 100 krad

The Cassini/CAPS (Cassini Plasma Spectrometer) power supply is, in very short form, included here. It has a –16 kV, and a +16 kV, and also a +1.2 kV above the negative voltage, outputs. As the photograph shows, it is of *modular* construction. That is, even within the high voltage section, it is *neither all* solid potted *nor all* just conformal coated. The two filter sections at the left side of the photograph are potted with EN-11 polyurethane as rectangular “blocks.”* The two high voltage stacks have the capacitors and diodes placed or “stuffed” within premachined housings. The transformers at the right-hand side are contained in molds made of Ultem 1000 by GE. Connections between these circuit elements are made with smooth surface, bare metal rods. Junctions of these rods are made within smooth, small metal corona balls, rather than soldered. Where these rods penetrate shielding box walls, they go through porcelain smooth surface insulators, etc. The entire voltage supply was assembled, certain areas were masked (see Appendix II of Ch. 3), and then the assembly was Parylene-coated, also according to Appendix II of Ch. 3. The reason that this packaging technique could be done for a 16 kV supply was that during the seven year flight to the vicinity of planet Saturn, the inside of the power supply would have been thoroughly outgassed, and the pressure within the supply would then be deep-space vacuum, an excellent insulator. The obvious advantages were the saving of weight, the ease of removal of a failed component during construction/testing, and also a considerable reduction of thermomechanical stresses during thermal excursions, which always exist within a large potted volume. At the time of this writing, the HV supply has already been operating well for five or six months.

* Instead of EN-11A/B, it was EN-4A used with EN-11B. EN-11A is no longer available. See Chapter 4, Appendix II.

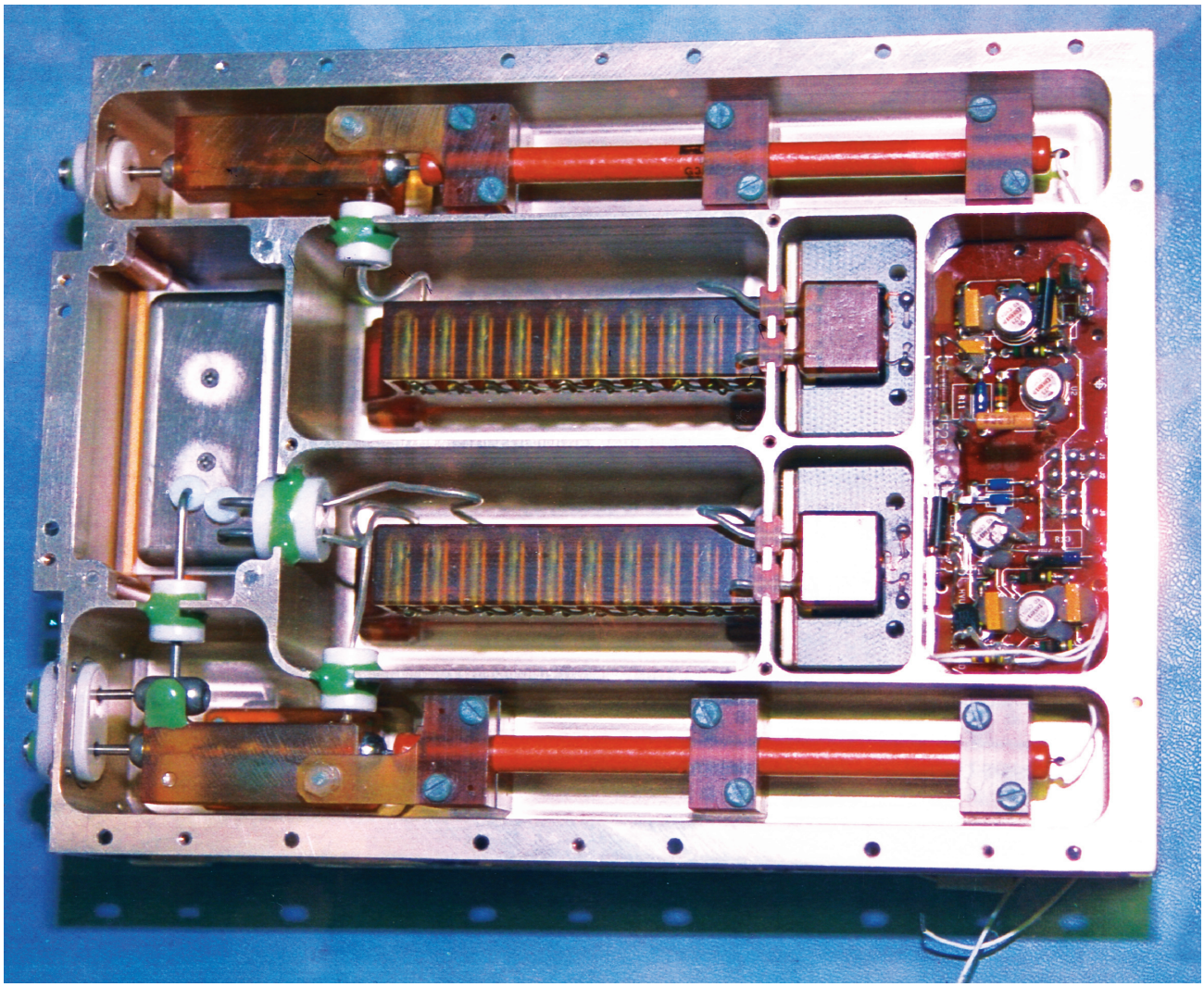


Figure 7.H.1. Cassini/CAPS HVU-1.

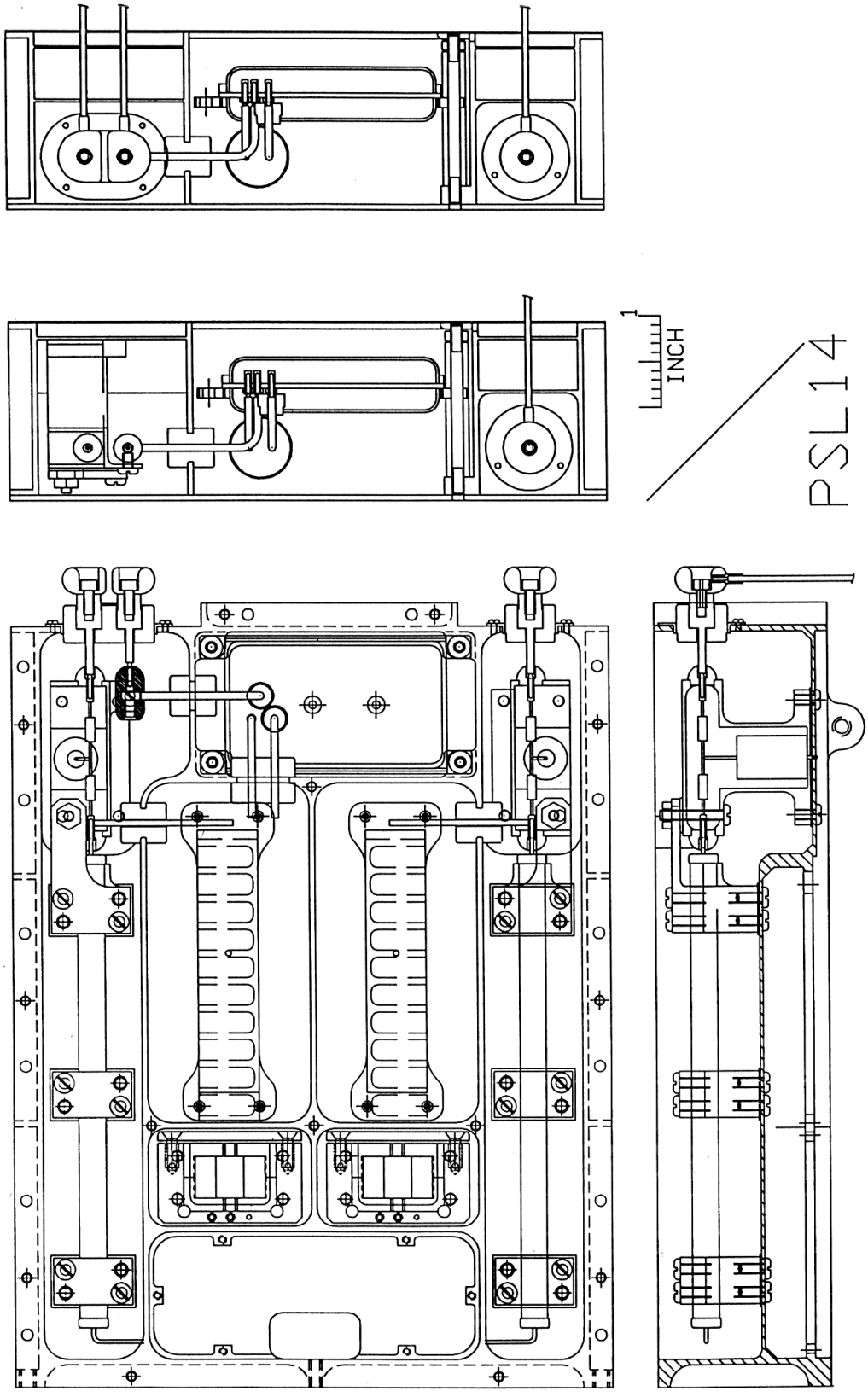


Figure 7.H.2.

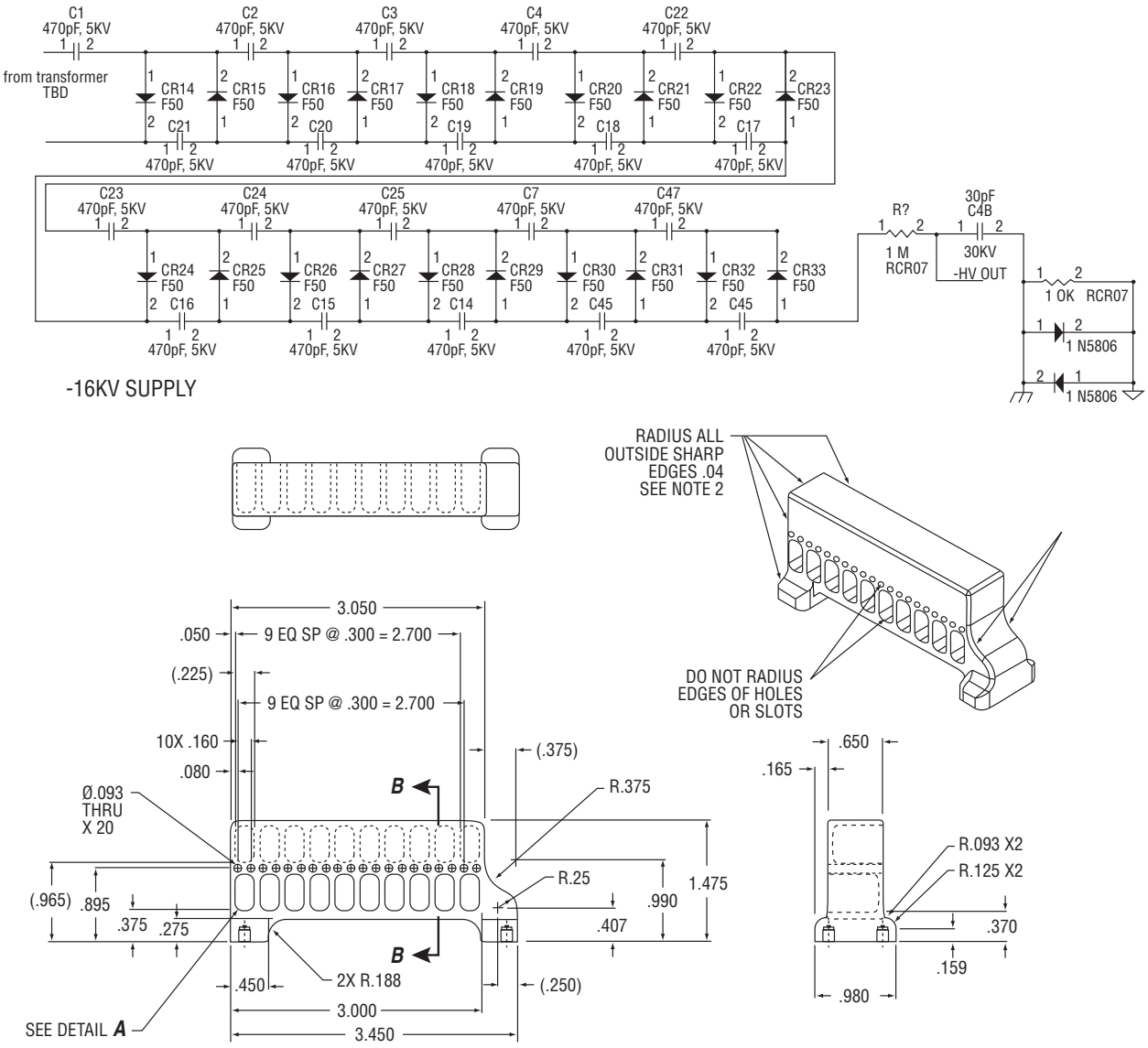


Figure 7.H.3. 10-stage HV multiplier.

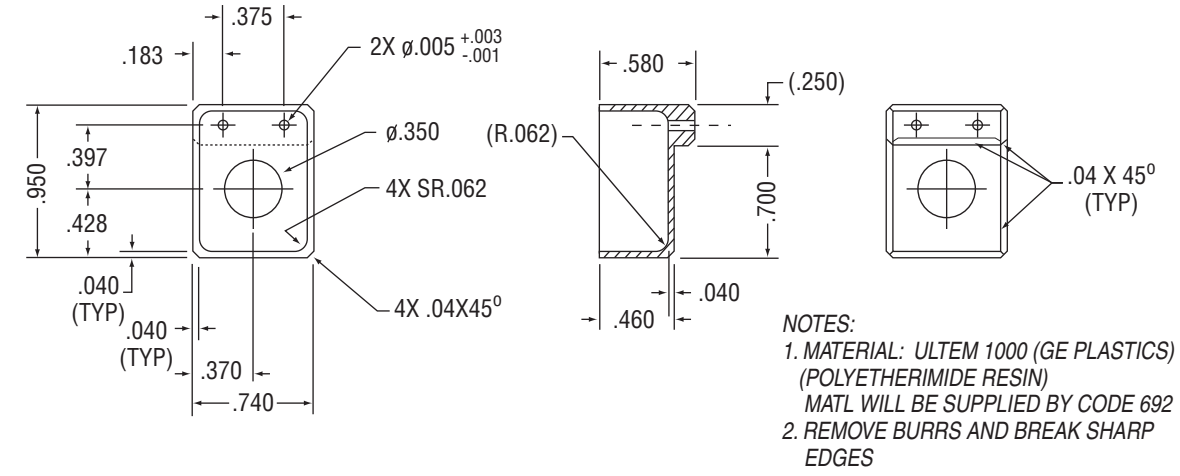


Figure 7.H.4

DESIGN EXAMPLE I

Anti-Coincidence Detector (ACD) High Voltage Bias Supply for ACD/GLAST project. Up to 1,300 V DC
Design Engineer: Arthur Ruitberg, NASA/GSFC

1.1 High Voltage Bias Supply (HVBS) Specification for ACD/GLAST

1.1.1 There shall be 24 HVBS, one for each eight phototubes

1.1.2 The high voltage bias supply shall operate from a +28 V ±6 V power supply. The ripple specification on this input power is < TBD mV rms.

1.1.3 The HVBS shall dissipate no more than 150 mW

1.1.4 The output shall be adjustable from 0–1300 V, ±5%

1.1.5 The output current shall limit at 40 μA

1.1.6 The ramp-up time constant shall be greater than 5 s and less than 30 s.

1.1.7 The ramp-down time constant shall be greater than 5 s and less than 30 s.

1.1.8 The mass shall be less than 100 g.

1.1.9 The overall volume of a single HVBS shall not exceed TBD mm x TBD mm x TBD mm.

1.1.10 The temperature stability of the HVBS shall be <5000 ppm/°C

1.1.11 The temporal stability of the supply shall be <0.5%/day

1.1.12 The HVBS shall provide an output monitor of 0–2.5 V that is proportional to the HV output to within 1%.

1.1.13 The HVBS oscillator frequency shall be >100 kHz

1.1.14 The output ripple/noise shall not exceed 2 mV peak-peak from 50 Hz to 50 MHz

1.1.15 The HV return shall be isolated from both chassis and HV supply ground by 100 Ω ±20 Ω. The HV return shall be grounded to the analog ground at the PMT with a DC resistance of < 100 mΩ.

1.1.16 All flight electronics surfaces shall be conformally coated with a NASA-approved polymer.

1.1.17 The HVBS will be enclosed in a conductive housing to provide EMI/EMC shielding. The enclosure surfaces will be plated with a non-oxidizing conductor.

1.1.18 A 1.5 mm ±0.5 mm diameter vent hole will be provided in the housing to ensure rapid venting.

Abbreviations to make subsequent pages readable:

ACD Anti-Coincidence Detector
BEA Base Electronics Assembly
BFA Base Frame Assembly
DAC Digital to Analogue Converter
EC Electronic Chassis
FREE Front End Event Electronics
GAFE GLAST ACD Front-end Electronics
GARC GLAST ACD Readout Chip
GLAST Gamma-ray Large Area Space Telescope
HVBS High Voltage Bias Supply
LAT Large Area Telescope
PCB Printed Circuit Board
PCU Power Control Unit
PMT Photo-Multiplier Tube
RN Resistor Network
SAA South Atlantic Anomaly

TDA Tile Detector Assembly
TSA Tile Shell Assembly

Packaging Considerations

Since the maximum voltage on anyone of these power supplies is only 300 V, then conformal coating with Parylene by vacuum vapor deposition was used. A process specification for Parylene coating is included in this book as an Appendix to Chapter 3. Although that particular specification is for Cassini/CAPS portions, the basic process is the same, although the parts to be "masked" are different.

General Comments

The ACD/GLAST High Voltage Bias Supply (HVBS) for the Photomultiplier Tubes (PMT) is an example of *Mass Production*. As seen on the Specification page: "There shall be 24 HVBSs, one for each of eight phototubes." In other words, there are 24 HVBSs *and* 24 x 8 or 192 high voltage distribution boxes from the 24 power supplies to the phototubes. This then is the reason for using the relatively new, in high voltage work, Flex Circuit Board. This has three layers of insulation adhered together, namely 0.002-in Kapton Flex between three layers of rigid Polyimide, for finished rigid thickness of about 0.062 in; and 4 layers of metallization trails and pads: Namely one layer on each side of the inner Kapton Flex and one layer on the outside of each of the Polyimide layers. These metallizations are deposited "to order" by the manufacturer. See the accompanying drawing and the color print of the Corona Test Object. The two 0.002-in thick "ribbons" of Kapton Flex connecting the three small square circuit boards have straight metallization trails on them, thus making electrical connections between proper points on the small square circuit boards. The Kapton "ribbons" are flexible and can be bent into U shapes or semicircular arcs. This enables several of the small square circuit boards to be stacked above each other into a relatively small shielding box, so some of the tedious assembly work for the large number of units in ACD/GLAST is done with relative ease.

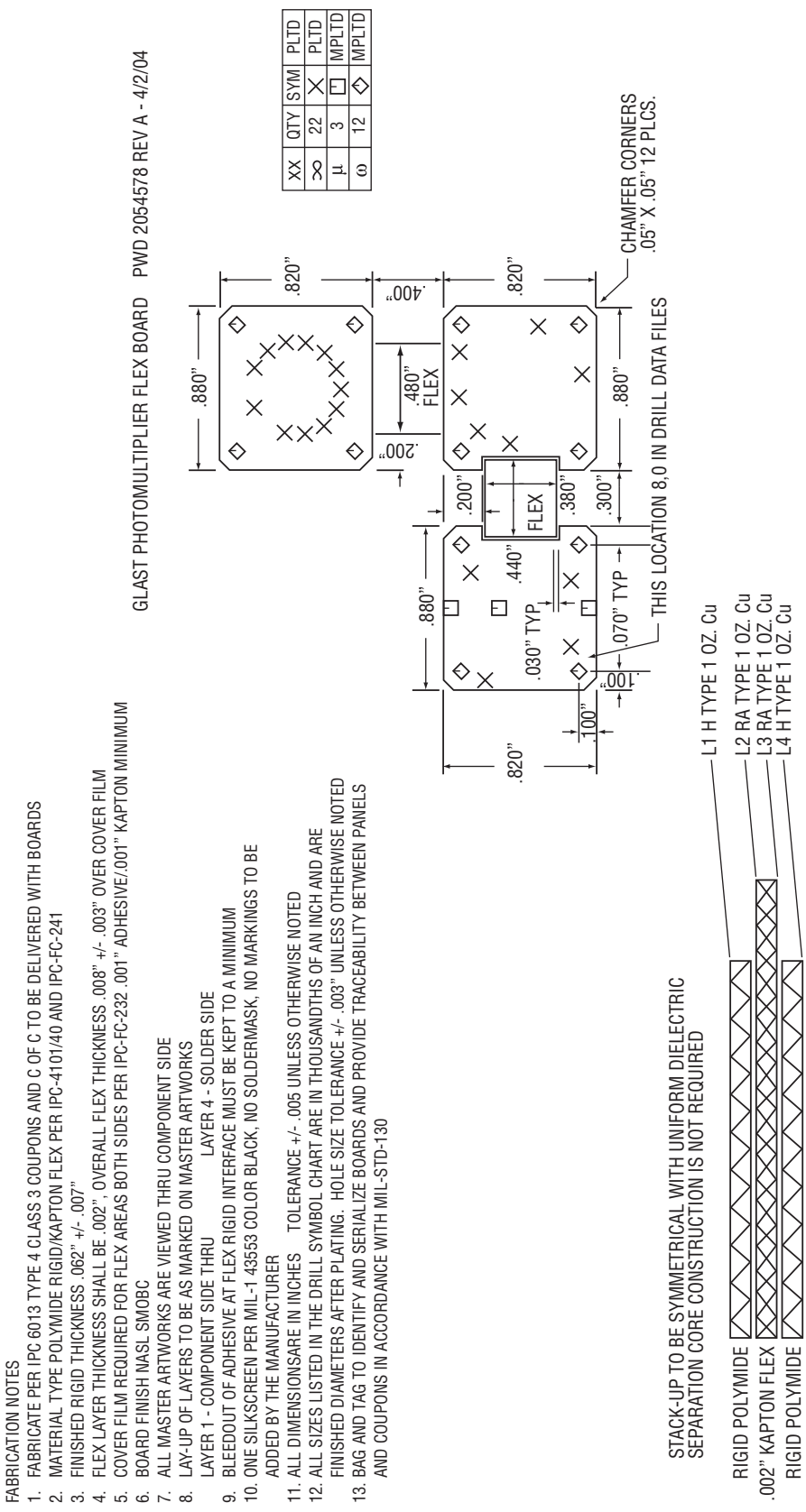
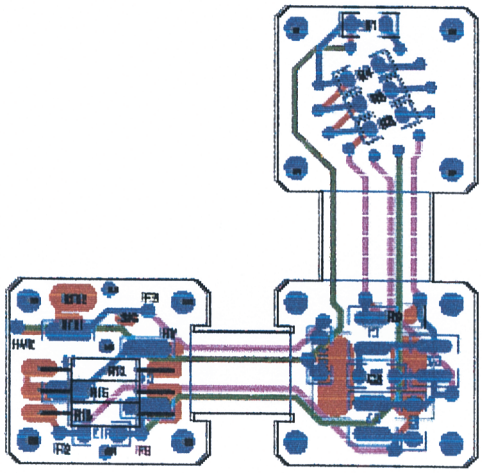

GLAST PHOTOMULTIPLIER FLEX BOARD PWD 2054578 REV A - 4/2/04
FABRICATION NOTES
1. FABRICATE PER IPC 6013 TYPE 4 CLASS 3 COUPONS AND C OF C TO BE DELIVERED WITH BOARDS
2. MATERIAL TYPE POLYMIDE RIGID/KAPTON FLEX PER IPC-4101/40 AND IPC-FC-241
3. FINISHED RIGID THICKNESS .062" +/- .007"
4. FLEX LAYER THICKNESS SHALL BE .002", OVERALL FLEX THICKNESS .008" +/- .003" OVER COVER FILM
5. COVER FILM REQUIRED FOR FLEX AREAS BOTH SIDES PER IPC-FC-232 .001" ADHESIVE/.001" KAPTON MINIMUM
6. BOARD FINISH NASL SMOBC
7. ALL MASTER ARTWORKS ARE VIEWED THRU COMPONENT SIDE
8. LAY-UP OF LAYERS TO BE AS MARKED ON MASTER ARTWORKS
LAYER 1 - COMPONENT SIDE THRU LAYER 4 - SOLDER SIDE
9. BLEEDOUT OF ADHESIVE AT FLEX RIGID INTERFACE MUST BE KEPT TO A MINIMUM
10. ONE SILKSCREEN PER MIL-1 43553 COLOR BLACK, NO SOLDERMASK, NO MARKINGS TO BE ADDED BY THE MANUFACTURER
11. ALL DIMENSIONSARE IN INCHES TOLERANCE +/- .005 UNLESS OTHERWISE NOTED
12. ALL SIZES LISTED IN THE DRILL SYMBOL CHART ARE IN THOUSANDTHS OF AN INCH AND ARE FINISHED DIAMETERS AFTER PLATING. HOLE SIZE TOLERANCE +/- .003" UNLESS OTHERWISE NOTED
13. BAG AND TAG TO IDENTIFY AND SERIALIZE BOARDS AND PROVIDE TRACEABILITY BETWEEN PANELS AND COUPONS IN ACCORDANCE WITH MIL-STD-130
XX QTY SYM PLTD
∞ 22 X PLTD
μ 3 □ MPLTD
ω 12 ◇ MPLTD
.820"
.880"
.400"
.480" FLEX
.200"
.200"
.380"
.300"
.880"
.820"
.880"
.440"
FLEX
.030" TYP
.070" TYP
.100"
.001"
CHAMFER CORNERS .05" X .05" 12 PLCS.
THIS LOCATION 8,0 IN DRILL DATA FILES
STACK-UP TO BE SYMMETRICAL WITH UNIFORM DIELECTRIC SEPARATION CORE CONSTRUCTION IS NOT REQUIRED
RIGID POLYMIDE
.002" KAPTON FLEX
RIGID POLYMIDE
L1 H TYPE 1 OZ. Cu
L2 RA TYPE 1 OZ. Cu
L3 RA TYPE 1 OZ. Cu
L4 H TYPE 1 OZ. Cu

Figure 7.I.1.

GLAST Photomultiplier Flex Board PWB 2054578 Rev - 02/9/04



Primary Component Side Layer 1 of 4 | Flex Layer 2 Layer 2 of 4 | Flex Layer 3 Layer 3 of 4 | Secondary Component Side Layer 4 of 4

Figure 7.I.2.

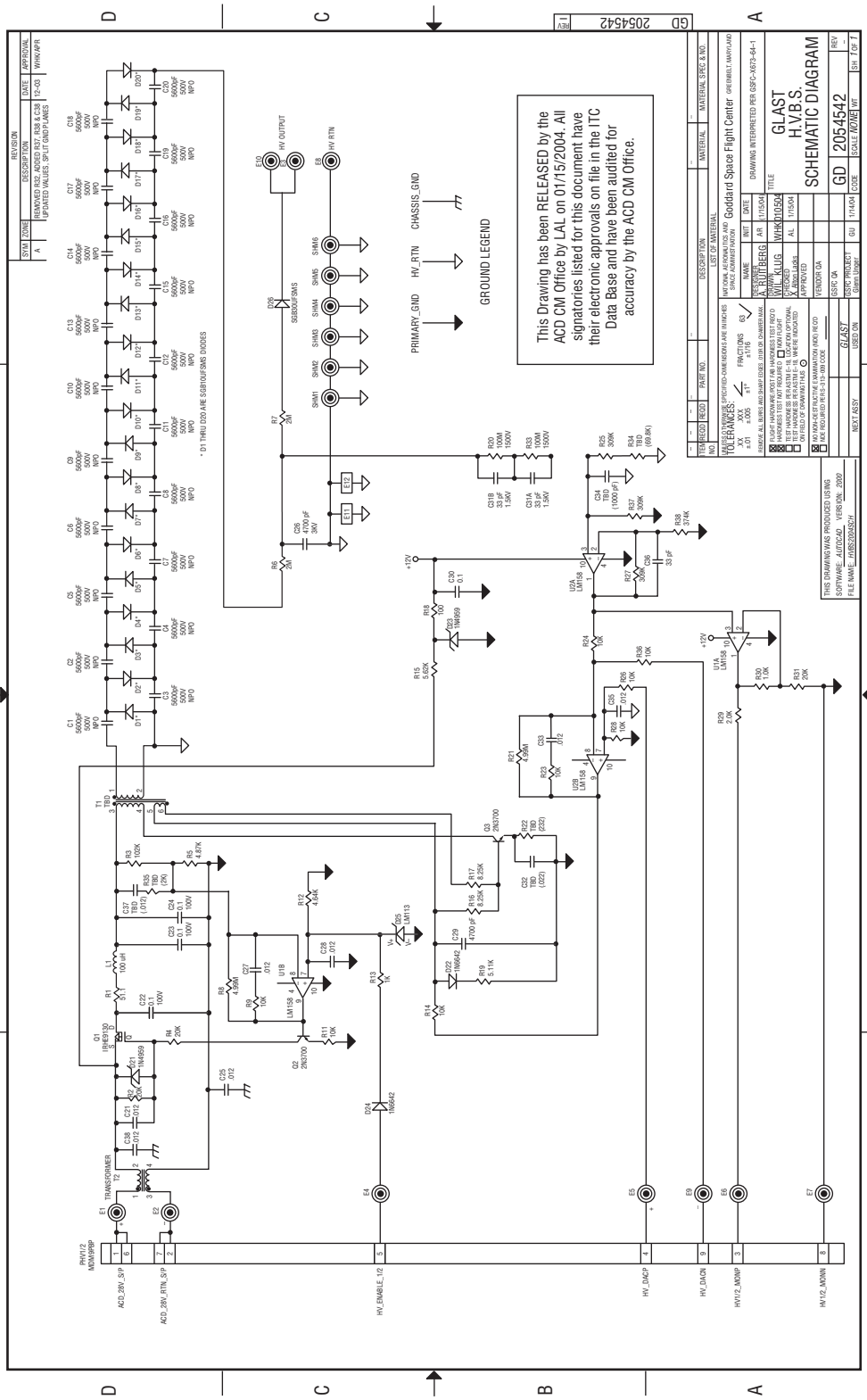


Figure 7.I.3. GLAST HVBS.

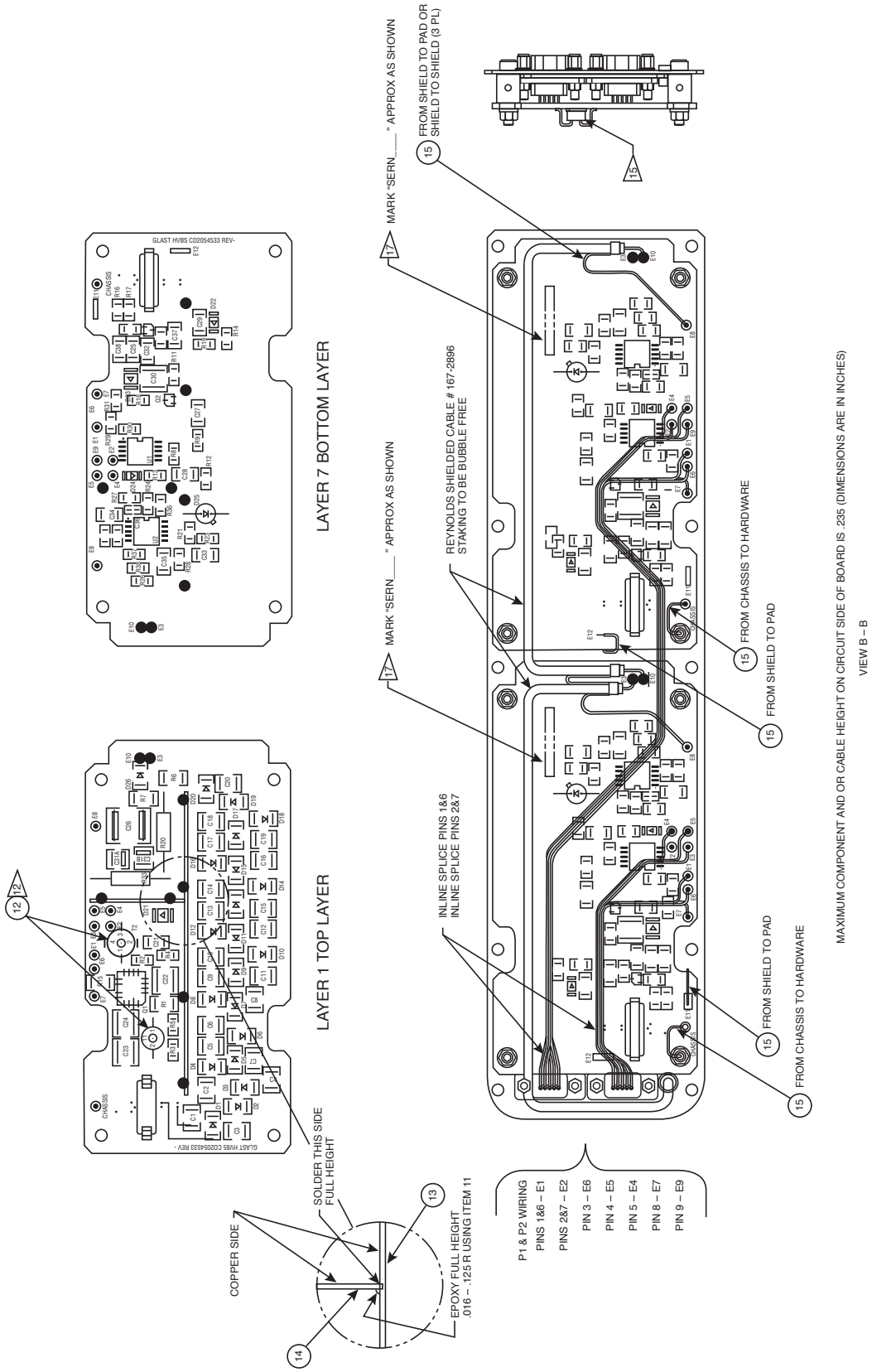


Figure 7.I.4. ASSEMBLY HVBS.

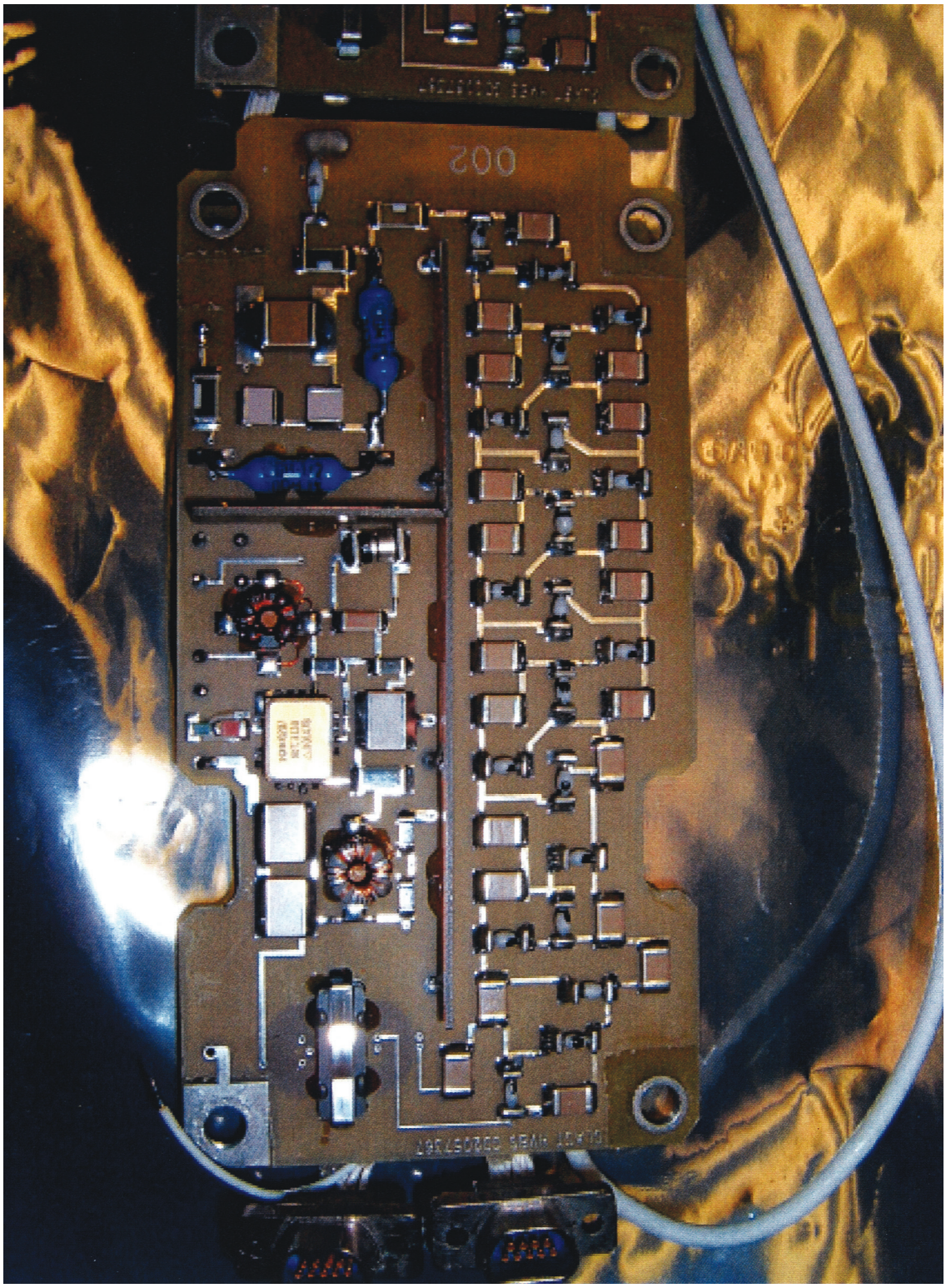


Figure 7.I.5. Photograph of HVBS.

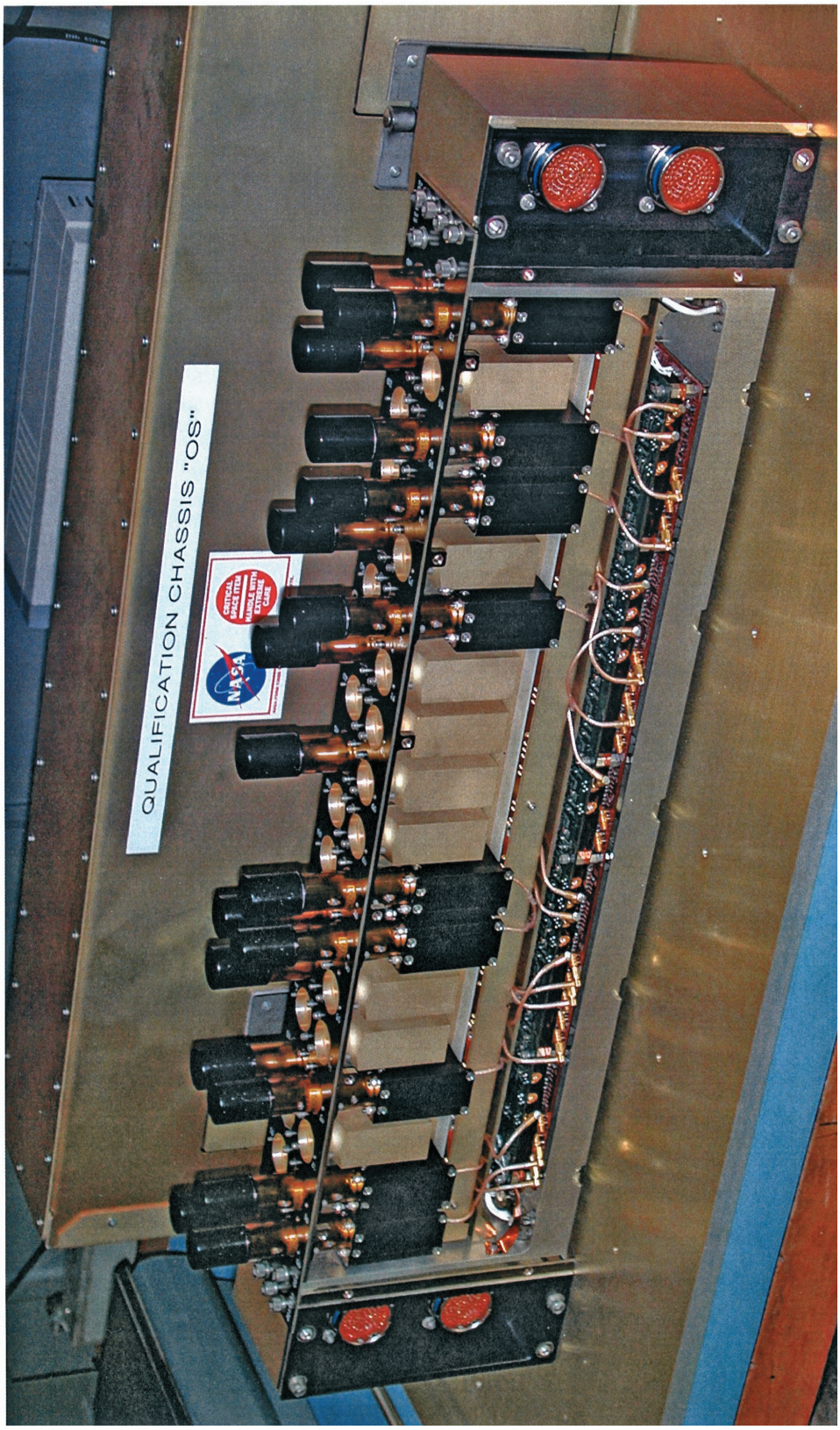


Figure 7.I.6. Photograph of some of the PMTs.

Appendix to Design Example I (HVBS)

Operational Guide for the GLAST ACD High Voltage Bias Supplies (HVBS)
DAS, 5/7/04

Purpose

It is possible that the intended operation of the ACD High Voltage Bias Supplies (HVBS) and their operational constraints, including the ways these work with the BEA electronics, is not immediately intuitive. This memo seeks to document some of the design intent and explain the expected operation functions, including *environmental pressure-related instrument safety issues.*

Table 7.I.1. Commands associated with the ACD HVBS.

Command	Function Code	Register Number	Data Field	Comment
HV_Level_Nominal	0	8	12 bits	This is a register in the GARC that contains the 12 bit value that will be sent to the DAC with the Use HV Nominal command.
SAA_HV_Level	0	9	12 bits	This is a register in the GARC that contains the 12 bit value that will be sent to the DAC with the Use HV SAA command.
Use_HV_Nominal	0	10	N/A	This command transfes the 12 bits in the HV_Level_Nominal register from the GARC to the MAX5121 DAC.
Use_HV-SAA	0	11	N/A	This command transfers the 12 bits in the SAA_HV_Level register from the GARC to the MAX5121 DAC.
GARC_Mode	2	8	12 bit register, [11:0] bits [3:1] are HV 1 Enables bits [6:4] are HV 2 Enables	These are the command bits for the Triple Modular Redundant command bits for the two supplies.
GARC_Status	2	9	N/A	This is a read-only register. Bit 1 is the HVBS 1 Enable status Bit 2 is the HVBS 2 Enable status

The block diagram below may assist operators in conceptualizing the HVBS control functions.

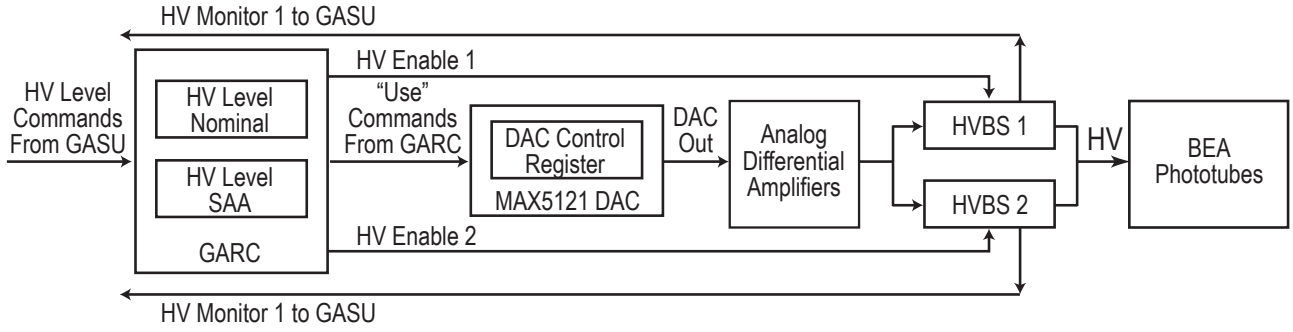


Figure 7.I.7. Simplified block diagram of ACD BEA high voltage control

Power

The ACD HVBS operate on +28 V power supplied to the BEA through the 79 pin circular connectors. The pin locations are identical for each of these connectors. There are two HVBS per chassis assembly. The BEA receives a nominal +28 V on pins 5 and 7 with the +28 V _RETURN on pins 33 and 34. The HVBS cannot supply a high voltage when this power supply is off (i.e., at 0 V). The FREE card uses a separate 3.3 V power supply and can operate independently from the HVBS. It is important that the +3.3 V FREE card power be ON when the HVBS +28 V power is ON. The GARC ASIC on the FREE card must be on to ensure proper control of the HVBS enables and DAC level commands.

HVBS Control

Once the +28 V power is applied to the HVBS, the FREE board controls the output level of the supplies by means of an analog level voltage and via a digital enable level. The digital enable level is active high, meaning that +3.3 V is considered ON and 0 V is considered OFF. The analog level voltage is sent to the bias supplies differentially. This is controlled on the FREE card via the output of the MAX5121 Digital-to-Analog converter (DAC). The FREE card has an amplifier circuit which converts the single-ended 0–1.249 V DAC output to a differential voltage of 0–2.5 V with a IAV pedestal offset. The full range of the differential voltage of 0–2.5 V with a 1.4 V pedestal offset. The full range of the differential voltage (i.e., 2.5 V differential) corresponds to a full-scale range on the bias supplies of approximately 1300 V.

Use of Triple Modular Redundancy in the High Voltage Enable Bits

The GARC_Mode command is used to enable and disable the two ACD HVBS in each chassis. Each HVBS is enabled/disabled independently. In the nominal operational mode, only one supply is enabled at a time.

It is considered important that the FREE electronics maintain control of the HVBS output voltages at all times. The use of Triple Modular Redundancy (TMR) in the logical constructs of the GARC seeks to alleviate the condition that a single-event upset (SEU) could alter the state of the HV Enable flip-flop. This is done by implementing a majority voting logic for these circuits. Therefore, proper use of the GARC_Mode command means that the ground command should set bit [3:1] all to the same value. This is also true for bits [6:4], (The one exception to this would be in Functional Tests where the operation of the TMR circuitry is being checked). These GARC_Mode bits are the inputs to the TMR voting logic. The outputs of the TMR logic are the physical level signals (HV _ENABLE_1 and HV _ENABLE_2) that are passed from the GARC to the HVBS 1 and 2. The status of these levels is monitored via the read-only GARC_Status command, bits 1 and 2, respectively.

It is important that during non-operational times (e.g., periods of instrument operation when the phototubes are desired to be OFF) that these levels are controlled to the "0" or OFF state. This is the only means to keep the HVBS outputs at a zero level. If the DAC is at a "zero volts" level, but the HVBS is enabled, the flight supplies may still output over 100 V DC.

During flight operations, the GARC_Mode register values may be periodically checked to ensure no upset has occurred or should be periodically reloaded with refreshed values. A rough estimate of the GARC upset rate would indicate that once a week or once a month would be more than adequate in flight.

Operations within the South Atlantic Anomaly (SAA)

The GARC has been designed to account for proper phototube operation during SAA transitions. The SAA is a region of charged particles pulled a bit closer to the Earth's surface by a local increase in the Earth's magnetic field. The implication for the ACD, which is by definition a charged particle detector, is a very substantial increase in the amount of light scintillating in the tiles in this region. Because of the radiation increase, no science observations will be possible for the LAT during SAA transitions, which will occur approximately every 100 min (but will vary based on the precession of the LAT orbit).

If the PMT high voltage is left at nominal levels during this time, there will be excess current flowing through the tubes, resulting in a decreased lifetime of the detector system. It is desirable to decrease the PMT high voltage (which is nominally about 1000 V for a gain of about 1×10^6) by several hundred volts to reduce the electron multiplication gain by several orders of magnitude. However, it is also not desirable to turn of the HVBS completely due to the mechanical stress associated with the cycling of high voltage capacitors. An intermediate approach is to maintain a level of bias on the PMTs that it represents a very low electron multiplication gain while not allowing a substantial electric field change within the high voltage capacitors. Therefore, it is more desirable to turn the PMT voltage down to a number such as 400 V or 500 V. This is accomplished by having two levels stored in the GARC—a "nominal" science operations level and a lower, protected level, which is designated as the "SAA level." These values are stored in registers in the GARC and sent to the DAC at the appropriate orbital times. \

One fact about the FREE electronics that is not necessarily intuitive is that the DAC output (which becomes the differential analog level control for the HVBS) is controlled by a register in the MAX5121 DAC, not the GARC. The values stored in the GARC are loaded into the MAX5121 register whenever one of the "Use Level" commands is sent. This allows the ACD BEA operator to verify that the correct values arc in the GARC registers prior to enabling transmission of the value from the GARC to the DAC.

One other advantage to this approach is refreshing the contents of the MAX5121 DAC control register. The MAX5121 is not a radiation-hardened part; it is a commercial device. A single-event upset (SEU) in the control register will be reflected in the DAC output. The process of sending the "Use Nominal" and "Use SAA" commands provides an automatic memory-scrubbing cycle on this register, which is designed to mitigate the effects of SEUs on the DAC logic. Additionally, operators should note that the value written into the MAX5121 DAC may be read back just one time; this part has the curious feature of a destructive read operation. This is the only GARC-addressable register which operates in this manner. This feature may be understood by doing a GARC Write command to one of the Use HV Level Function/Registers and then doing a GARC Read command to the same Function/Register. This will return the value from the MAX5121. Subsequent reads will produce a different data pattern; the read is destructive in nature. Reading the MAX5121 does not affect the value latched into the part, however. Only the verification aspect is destructive.

Consideration of the Pressure of the Environment in which the HVBS Operates

The ACD HVBS are sensitive to the gas pressure under which they are operated. This is an ACD instrument safety issue. Operators of the ACD must be conscious never to enable the high voltage bias supplies unless the pressure

is approximately 1 atm (i.e., 760 torr nominal) or the pressure is less than 5 x 10^{-6} torr in a vacuum environment. If operated in a vacuum environment, the electronics should have been at the < 5 x 10^{-6} torr limit for 12 hours or more to ensure proper venting. If the HVBS are operated in between these regions (i.e., in the region 5 x 10^{-6} torr < Pressure < Ambient) , there is a possibility of a corona discharge occurring in either the HVBS or the PMT assemblies. (We would expect arcing when the local pressure around a HV component is somewhere in the 10^{-1} to 10^{1} torr range). This form of plasma discharge could cause permanent damage to the electronics of the BEA. There are two expected environments where this is applicable: thermal vacuum testing and in-flight operations.

The responsibility for correct operation of the high voltage control must fall on the Test Conductor. It should not be assumed that test scripts can be relied on to autonomously protect the instrument. Additionally, the concerns with high voltage operations may not be obvious to those unfamiliar with the operation of the ACD.

Sample HVBS Power-Up Sequence

The following represents a strawman sequence of steps for correctly powering up a BEA HVBS. It is possible this might be used to form a template that could be used for an actual script.

1. Verify that the ACD +3.3 V power is on and currents are nominal.
2. Verify that the BEA chassis is in the proper pressure environment (as described above).
3. Send an ACD GARC_Mode Read command. Verify bits [6:1] are 0.
4. Send an ACD GARC_Status Read command. Verify bits [2:1] are 0.
5. Verify that the ACD +28 V power is on and currents are nominal.
6. Verify the GASU HVBS Monitors 1 and 2 are reading ≈0 V
7. Send an CD GARC_Mode write command with bits [3:1] at b´111.
8. Send an ACD GARC_Mode read command to verify this command.
9. Send an ACD GARC_Status Read command. Verify bits [2:1] are b´01, indicating HVBS 1 is enabled and HVBS 2 is disabled.
10. Send the GARC HVBS Level Write command with a data argument of 300. Verify with a GARC Read command.
11. Send the Use_HV _Normal write command. Verify the DAC register contents with the Use_HV _Normal read command.
12. Verify that the GASU HVBS Monitor 1 reads an equivalent of approximately 100 V and that HVBS Monitor 2 reads approximately 0 V. Verify that no phototube has a rate in excess of 1 kHz (if it does, stop at this point and inform the science team).
13. Verify that the +28 V current is at a nominal value.
14. Repeat steps 10–13 with data arguments of 600, 900, 1200, etc., up to 3000. At a DAC register content of 3000, the HVBS should be at about 1000 V. PMT rates should be less than 1 kHz.

Powering down the supply would be essentially the same sequence of steps, but in reverse (larger data argument steps could be used, for example steps of 1000). The DAC register would be ramped down to 0 and then the GARC_Mode enable bits would be zeroed out.

AUTHOR'S NOTE

The chapters in this document have evolved over a period of several years and from Knowledge Capture meetings where exchange of experience and knowledge took place between several personnel. It is hoped by the authors that engineers and technicians that are newly entering the field will find this book helpful to them.

As seen in the last chapter—Chapter 7—much work has been done at GSFC and elsewhere, on power supplies that produce high voltage biasing for scientific instruments, but put out minimal current. Designs for Traveling Wave Tube (TWT) supplies or laser power supplies, which must give considerable current as well as high voltage, are *not* included in Chapter 7.

Such high voltage– high current supplies are usually called Electronic Power Conditioners or EPCs. These have several outputs with two or even more outputs delivering tens of watts to the TWTs (or lasers). This means, for example, for a 60 W TWT, that 25 milliamperes (mA)—not microamperes (μA)—are delivered by the EPC at 2500 V, by just a single output.

Obviously for these supplies, the low voltage portions of the circuits are very different and the parts and the transformer windings are different, etc., than for any of the low current, high voltage supplies discussed in this book. More feedback loops must be added for over-current and over-power protection. Also, the mounting of parts and the encapsulating resin must be chosen to get the internally developed heat (usually several watts) out of the supply to avoid thermal run-away.

Generally speaking, NASA relies on private industry to design and build these EPCs. In today's world of company buy-outs, finding names of manufacturers can be difficult. The authors of this book, have supplied several names of such manufacturers in the United States—not to recommend one over others—but to help the reader know where to begin to look, if necessary.

For TWTs:

Electron Technologies, Inc. (ETI), Divsion of L-3 Communications, Torrance, CA
Dynamic Wave Telecom, Inc., Anaheim, CA
Quarterwave Corp., Rohnert Park, CA
MCL, Inc., Bollingbrook, IL

There are also companies in Europe and Japan.

Authors (Left to Right): Renate Bever, Arthur Ruitberg, and Carl Kellenbenz. (Sandra Irish was not available the day the picture was taken.)

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14. ABSTRACT

This book is written for newcomers to the topic of high voltage (HV) in space and is intended to replace an earlier (1970s) out-of-print document. It discusses the designs, problems, and their solutions for HV, mostly direct current, electric power, or bias supplies that are needed for space scientific instruments and devices, including stepping supplies. Output voltages up to 30 kV are considered, but only very low output currents, on the order of microamperes. The book gives a brief review of the basic physics of electrical insulation and breakdown problems, especially in gases. It recites details about embedment and coating of the supplies with polymeric resins. Suggestions on HV circuit parts follow. Corona or partial discharge testing on the HV parts and assemblies is discussed—both under AC and DC impressed test voltages. Electric field analysis by computer on an HV device is included in considerable detail. Finally, there are many examples given of HV power supplies, complete with some of the circuit diagrams and color photographs of the layouts.

15. SUBJECT TERMS

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