

Radiation Hardened Electronics for Extreme Environments

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Abstract: *The Radiation Hardened Electronics for Space Environments (RHESE) project consists of a series of tasks designed to develop and mature a broad spectrum of radiation hardened and low temperature electronics technologies. Three approaches are being taken to address radiation hardening: improved material hardness, design techniques to improve radiation tolerance, and software methods to improve radiation tolerance. Within these approaches various technology products are being addressed including Field Programmable Gate Arrays (FPGA), Field Programmable Analog Arrays (FPAA), MEMS, Serial Processors, Reconfigurable Processors, and Parallel Processors. In addition to radiation hardening, low temperature extremes are addressed with a focus on material and design approaches.*

Keywords: radiation hardened; extreme environments; low temperature; FPGA; MEMS; high performance processors; reconfigurable computers; SiGe electronics

Introduction

The Radiation Hardened Electronics for Space Environments (RHESE) project expands the current state-of-the-art in radiation hardened electronics to develop high performance devices robust enough to withstand the extreme radiation and temperature levels of the space environment. The primary customers of RHESE technologies will be the missions being developed under NASA's Constellation program, including the lunar and Mars missions that will serve to accomplish the goals of the Vision for Space Exploration¹. Secondary customers for RHESE technologies include NASA science missions, collaborative efforts with other agencies of the US Government, and commercial applications. NASA's Marshall Space Flight Center (MSFC) manages the RHESE project.

The RHESE project provides a full spectrum of approaches to harden space electronics, including new materials, design processes, reconfigurable hardware techniques, and software techniques. Initial work within RHESE focuses on hardening Field Programmable Gate Arrays (FPGA)s and Field Programmable Analog Arrays (FPAA)s for use in reconfigurable architectures. As these technologies mature, the project shifts focus to efforts encompassing total processor hardening techniques. This phased approach to distributing emphasis between technology developments provides hardened FPGA/FPAA's for early mission infusion, including the Constellation program's Lunar

Precursor and Robotic Program (LPRP), then migrates to hardened, high speed processors with associated memory elements and high density storage for the longer duration missions encountered for Lunar Outpost and Mars Exploration occurring later in the Constellation schedule.

In addition to electronic hardening against radiation environments, RHESE supports the development of electronics capable of operating in extreme low temperature environments. Research in SiGe materials and designs using Micro Electro-Mechanical System (MEMS) constitute the RHESE efforts in low temperature electronics.

Though the tasks within RHESE are broad-based and diverse, they collectively include the development of:

- Total dose radiation tolerant electronics,
- Single Event Upset (SEU)-tolerant electronics,
- Latch-up tolerant electronics,
- High performance processors,
- Low temperature electronics,
- Reconfigurable robust electronics, and
- Updated models capable of predicting the effects of radiation on electronics.

The RHESE tasks are organized into a work breakdown structure that divides the effort into the following major categories of research: radiation hardened materials, radiation hardened by design, radiation hardened by software, high performance processors, reconfigurable processors, high density storage, and low temperature electronics. These categories are arranged in the RHESE Work Breakdown Structure (WBS), as shown in Table 1, and are subsequently described in the following sections.

Radiation Hardened Materials

RHESE address the development of hardened materials for electronic application in the space environment and the ability to appropriately model these materials within various spacecraft configurations. RHESE supports three tasks that are scoped to address material design and usage concerns. These tasks are the Self-Reconfigurable Electronics for Extreme Environments, Radiation Effects Predictive Modeling, and Ferroelectric-Based Electronics.

Table 1. RHESE tasks, implementing organizations, and responsible NASA centers as mapped into the project WBS

WBS#	Task	Implementing Organization	Responsible Center
1.0	Radiation Hardened Electronics for Space Environments	MSFC	MSFC
1.1	Program Management	MSFC	MSFC
1.2	Radiation Hardened Electronics	MSFC	MSFC
1.2.1	Radiation Hardened Materials		
1.2.1.1	Self-Reconfigurable Electronics for Extreme Environments (SRE-EE)	JPL	JPL
1.2.1.2	Model of Radiation Effects on Electronics	MSFC	MSFC
1.2.1.3	Ferroelectric Based Electronics	MSFC	MSFC
1.2.2	Radiation Hardened by Design		MSFC
1.2.2.1	SEE-Immune Reconfigurable Field Programmable Gate Array	Sandia National Laboratory	GSFC
1.2.3	Radiation Hardened by Software	ARC	ARC
1.2.4	High Performance Processors	GSFC	GSFC
1.2.5	Reconfigurable Processors	MSFC	MSFC
1.3	Low Temperature Radiation Hardened Materials	MSFC	MSFC
1.3.1	SiGe Integrated Electronics for Extreme Environments	Georgia Institute of Technology	LaRC
1.3.2	Low Temperature MEMS by Design	ARC	ARC

Self-Reconfigurable Analog/ Mixed Signal Electronics for Extreme Environments (SRE-EE): The scope of the SRE-EE task is to develop analog and mixed signal field FPAA technology for operation in the extreme radiation and temperature environments of space. NASA's Jet Propulsion Laboratory (JPL) leads the effort and includes the participation of NASA's Langley Research Center (LaRC), University of Southern California, the Georgia Institute of Technology (Ga. Tech.), the United States Navy Space Warfare center, and BAE Systems.

The SRE-EE designs and algorithms detect degradation in circuit performance due to faults or partial drifts attributable to temperature and radiation, then compensate for these faults and drifts by autonomously changing to another configuration that is more appropriate for the encountered environment.

Specific products provided by the SRE-EE task will be:

- Reconfigurable Analog Array Integrated Circuit (RAA-IC) in flip-chip technology with radiation and temperature tolerant building blocks,
- Breadboard with RAA-IC and FPGA that controls RAA-IC compensation,
- Radiation and temperature tolerant RAA-IC with self-compensation of a connected sensor,
- Breadboard with sensor, RAA-IC and FPGA that controls RAA-IC and sensor,

- Radiation and temperature tolerant Self-Reconfigurable Analog Array Integrated Circuits (SRAA-ICs) combining in a single chip reconfiguration analog building blocks and digital controls tested to survive -180C to +125C, 300K rad total integrated dose (TID) with SEUs, and
- Environment validated library of reconfigurable analog building blocks.

Verification of SRE-EE components will consist of characterizing a large sample of the SRAA IC and the building blocks of the library as a function of temperature. It will also include radiation characterization up to a total dose to 300 kRad and life testing at the extremes of the specified temperature range for total of 1000 hours. Additional testing at -180C under radiation will be used to evaluate the combined effect of temperature/radiation.

Model of Radiation Effects on Electronics: An updated model of radiation effects on electronics is critical to the implementation of space systems operating in the radiation environment. Designers must use this updated model to predict the mean-time-between-failure (MTBF) of their circuit designs when they choose to use state-of-the-art parts like the new radiation-hardened electronics that are being development in this project and elsewhere. This task develops a tool for estimating the total radiation dose expected for specific sets of electronics, and the frequency of the various single event effects that could occur in the space environment. This tool will be developed jointly by MSFC and Vanderbilt University and is planned to be internet accessible as it will replace the current radiation modeling standard of CREME96².

Specific products provided by the modeling task will be:

- Updated models and tools for estimating total dose and single event rates for electronic devices and
- Publication of these models and tools on the internet.

Verification of the new radiation model will be by comparison of model output with data obtained through test within accelerator facilities and through exposure to the space environment.

Ferroelectric Based Electronics: MSFC leads this effort in an emerging technology material development area that offers a high degree of radiation hardness, non-volatility, and on-the-fly reconfigurability. Ferroelectric materials have several advantages such as an extremely low coercive field, a high remnant polarization, better mechanical strength and small deviation in composition.

The objectives of this task are to identify candidate technologies, characterize their performance, and work with the companies developing the technology to meet the needs of deep space NASA missions.

Specific products provided by the modeling task will be:

- Radiation hardened memory devices,
- Ferroelectric Field Effect Transistor (FeFET) logic devices, and
- FeFET analog devices.

These products will be tested, characterized, and verified within temperature ranges from -230 degrees Celsius to +85 degrees Celsius. Both TID and SEU characterization testing are planned.

Radiation Hardened by Design

This area focuses on design approaches to improve radiation hardness that can be applied to any material system.

SEE-Immune Reconfigurable Field (SIRF) Programmable Gate Array: This task is led by NASA's Goddard Space Flight Center (GSFC) and is jointly supported by the Air Force Research Laboratory (AFRL). NASA and Sandia National Laboratory in partnership with Xilinx and the University of Idaho Center for Advanced Microelectronics and Biomedical Research are collaboratively developing the technologies required to implement a radiation-tolerant version of the Xilinx Virtex-4 FPGA. SIRF-based FPGAs can be used to implement subsystems that incorporate radiation-tolerant reconfigurable interfaces and digital interconnects. Such subsystems can be field programmed and reprogrammed to implement multiple functions in diverse systems.

Specific products provided by the SIRF task are:

- Design techniques to produce radiation tolerant Virtex-4 FPGA technology.

The SIRF verification plan ensures the delivered products map to detailed project requirements that address several issues, including performance characteristics, environmental susceptibilities, physical characteristics, and compatibility with the Xilinx development environment.

Radiation Hardened by Software

NASA's Ames Research Center (ARC) leads the development of Radiation Hardening by Software (RHS) technology. This task explores the addition of radiation hardening during the circuit design phase so that the resulting circuits are resistant to radiation events. The general approach of RHS is to pre-process circuits to make them resilient to SEEs by using evolutionary algorithms and other optimization techniques to insert data redundancy, efficient consistency checks, or other fault-mitigating structures.

Specific products provided by the RHS task are:

- A library of rad-hardened digital circuitry sub-modules,
- An evolutionary design toolbox that hardens a class of circuits with the ability to recover from a single fault, and
- An evolutionary design toolbox that hardens a class of circuits with the ability to recover from multiple simultaneous faults.

The verification of the RHS tools and libraries will proceed in two phases. First, throughout technology development, the tools will be continuously verified using radiation effect simulators that have been calibrated against in-beam radiation test data. Additional test data, such as better characterization of Single Event Transients (SET) in FPGAs, will be generated in-beam if needed to provide reasonable assurance of simulator veracity. Second, as the technology approaches a mid-maturity level, in-beam testing will be performed on complete designs produced using RHS. The overall target for design hardness is 10^{-12} unrecovered SEU/SET errors per bit-day in a radiation environment comparable to that of mission scenarios.

High Performance Processors (HPP)

The objective of the HPP task will be to identify emerging developments of new processors and new applications of existing processors into devices suitable for use in space environments. This task seeks to advance the state of the art of two metrics (sustained throughput and processing efficiency) for high-performance radiation-hardened processors by at least one order of magnitude. The resultant goals are throughput greater than 2000 Million Instructions Per Second (MIPS) with efficiency better than 500 MIPS/Watt. The task will be lead by GSFC, with support from MSFC, LaRC, and JPL.

The specific product provided by the HPP task is:

- High-performance (2000 MIPS, 500 MIPS/W) radiation hardened processors for space application.

Processor verification plans will ensure the deliverables map to detailed requirements. These requirements will address several issues, including performance characteristics, environmental susceptibilities, physical characteristics, and compatibility with targeted software compilers, development systems and operating systems.

Reconfigurable Processors

Reconfigurable processors is a task managed by MSFC that offers a reduction in flight spare inventories for long-duration missions, adaptability to system failures, and flexibility in interfacing components through the reconfiguration of a single onboard processor that can conform to multiple configurations.

Specific products provided by Reconfigurable Processors are:

- Support for multiple architectures to enable single spares to fulfill multiple electronic functions,
- Support for redundancy by providing adaptable spares,
- Support for recovery from component damage by radiation strikes and other events, and
- Support for multiple interconnection options.

Verification of the capabilities produced will be accomplished by two means, both involving testing. First, since exposure to harsh environments will not necessarily guarantee errors, and even supposing errors do result, their nature and behavior cannot be rigorously controlled, it will be necessary to induce known errors. Various means for inducing these errors in a methodical manner will be devised. Second, testing in actual environmental chambers will be carried out to simply satisfy the validity of the schemes under harsh conditions representative of planned target flight environments.

Low Temperature Radiation Hardened Electronics

Two low temperature electronics tasks are being supported to develop capabilities for long duration planetary surface operations; including operations in night or partially/permanently shadowed conditions.

SiGe Integrated Electronics for Extreme Environments: This task is led by the Georgia Institute of Technology. The goal of this task is to develop and demonstrate extreme environment electronics components using low-cost, commercial SiGe Bi-Complementary Metal Oxide Semiconductor (BiCMOS) technology. SiGe BiCMOS offers unparalleled low temperature performance, wide temperature capability, and optimal mixed-signal design flexibility at the monolithic level by offering power efficient, high speed devices and high density Si CMOS.

Specific products provided by SiGe Integrated Electronics are:

- Low Temperature Analog Circuits,
- Low Temperature Data Converters,
- Low Temperature Digital Circuits,
- Low Temperature Power Electronics, and
- Low Temperature Circuit Packaging

The verification phase of this project will consist of characterization of a large sample (> 20 chips) including the various mixed-signal components of the library as a function of temperature from -180C to 120C. It will also include radiation characterization (to a total dose of at least 300 krad); life testing at the temperature extremes (-180C and 120C) for 1,000 hours; as well as over-temperature cycle testing for a total of 100 cycles.

Low Temperature Tolerant MEMS by Design: MEMS are micro-scale, mechanical systems with a number of advantages that make them particularly suitable for space applications, where weight, power and volume are at a premium. ARC will mature a suite of design-optimization technologies in support of exploration missions. Specifically, tasks will be conducted to develop and test advanced software technologies to automate the design of temperature-hardened MEMS devices that are capable of operating in very low temperature (-180C) environments.

Specific products provided by the Low Temperature MEMS Design are:

- Design rules and algorithms for computer-assisted design of low-temperature MEMS design.
- A tool for designing multiple classes of temperature-hardened MEMS devices
- Computer cluster modeling software for MEMS design and simulation.
- System for automatically evaluating instances of a class of MEMS designs
- Retooled MEMS design software to include low-temperature capabilities

Verification of the technology to produce low-temperature MEMS devices will be done by fabricating multiple copies of a computer-generated MEMS design and testing them at the temperatures ranging between -180C and +85C. The pass/fail criteria under which the devices will be evaluated depends on the particular class of device being tested. MEMS resonators must resonate at a frequency within 5% of the target frequency for which they will be designed.

References

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2. <https://creme96.nrl.navy.mil>