BAE Systems Radiation Hardened SpaceWire ASIC and Roadmap

Unclassified

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Abstract

An Application Specific Integrated Circuit (ASIC) that implements the SpaceWire protocol has been developed in a radiation hardened 0.25 micron CMOS technology. This effort began in March 2003 as a joint development between the NASA Goddard Space Flight Center (GSFC) and BAE Systems. The BAE Systems SpaceWire ASIC is comprised entirely of reusable core elements, many of which are already flight-proven. It incorporates a 4-port SpaceWire router with two local ports, dual PCI bus interfaces, a microcontroller, 32KB of internal memory, and a memory controller for additional external memory use. The SpaceWire ASIC is planned for use on both the Geostationary Operational Environmental Satellites (GOES)-R and the Lunar Reconnaissance Orbiter (LRO). Engineering parts have already been delivered to both programs.

This paper discusses the SpaceWire protocol and those elements of it that have been built into the current SpaceWire reusable core. There are features within the core that go beyond the current standard that can be enabled or disabled by the user and these will be described. The adaptation of SpaceWire to BAE Systems' On Chip Bus (OCB) for compatibility with the other reusable cores will be discussed. Optional configurations within user systems will be shown. The physical implementation of the design will be described and test results from the hardware will be discussed. Finally, the BAE Systems roadmap for SpaceWire developments will be discussed, including some products already in design as well as longer term plans.

Acknowledgement

The authors gratefully acknowledge the NASA Glenn Research Center and the GOES-R program for their support, as well as the team of engineers who developed the other logic cores reused for this design.

The SpaceWire Interface Protocol and Core Implementation

The SpaceWire link, defined in European Cooperation for Space Standardization (ECSS) document, ECSS-E-50-12A, defines scalable links with a full duplex physical layer that employs Low Voltage Differential Signaling (LVDS) serial interfaces with data strobe encoding. As implemented in this ASIC, the LVDS physical interfaces operate at a maximum rate of 265 MHz, clocked with a dedicated Phase Locked Loop (PLL).

As defined in the SpaceWire specification, the router is a non-blocking cross-bar switch that allows simultaneous connection from any input port to any other output port unless multiple input ports request the same output port. In that event, arbitration is employed that may result in stalling links. The routing approach is called "wormhole" routing. It reduces latency by passing the beginning of packets on to the next router in a network before the first router receives the entire packet. As a result, a packet may end up being strung across several different routers. However, this feature also introduces the possibility to blockage in the switch fabric, which can be mitigated by controlling the maximum packet size and matching the receiving First-in, First-out (FIFO) buffers to the packet size. The router in this core implementation includes a unique "crowbar" feature that is designed for use with sources that provide only a raw data stream without routing information. With this feature, a raw data stream that arrives on a given port can be hard wired to connect to another pre-defined port even though the routing information is not contained within it.

The SpaceWire protocol supports two addressing modes: path addressing that uses addresses 1-30 and logical addressing that supports addresses from 32 to 254. When a data packet is required to transverse multiple SpaceWire routers, additional path addresses are concatenated within the header. As each hop is completed, the matching path address is removed, exposing the next path address. Alternatively, logical address information is maintained across all the hops until the SpaceWire data arrives at its intended destination. As such, logical addressing requires lower overhead than path addressing.

As implemented in the SpaceWire ASIC, the link portion of the core includes sections of logic operating at one quarter the serial link rate and the router (switch) runs at one eighth the serial link rate of the LVDS interface. The core is connected to the remainder of the design through an asynchronous interface. A block diagram of the SpaceWire core is shown in Figure 1. The SpaceWire Link core VHDL design was first implemented in the NASA Swift program, subsequently upgraded for the James Webb Space Telescope (JWST) program, and became the baseline for this SpaceWire ASIC [1, 2].

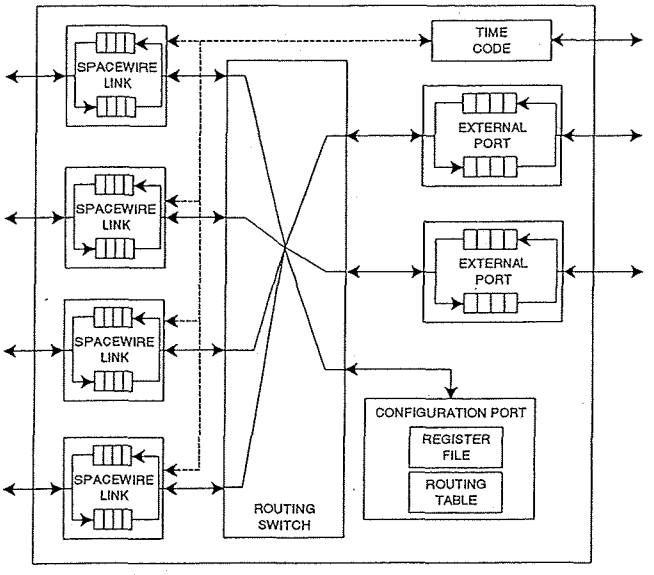

Figure 1: SpaceWire Core Block Diagram

The SpaceWire protocol defines two types of characters: control characters, which are 4 bits in length, and data characters, which are 10 bits. All characters include both an odd parity bit for error detection and a bit identifying the character as control vs. data. The packet size in the SpaceWire protocol is completely variable, bounded by a destination header on the front end and an "end of packet" marker character at its conclusion.

System level synchronization information is provided through a time code, which is a special control code that is broadcast over the network with low latency. The SpaceWire standard provides for one master to broadcast time code information across the network. One feature of this core implementation that is beyond the base SpaceWire specification is the ability for up to 4 masters to broadcast simultaneous time codes (up to 4), based on the use of two reserved bits that are the most significant bits of the data character. In addition, the router in this core design includes a "zero time-code jitter" feature that matches time code pulses to the same clock edge. Features of the core that go beyond the standard can be disabled for backward compatibility to other SpaceWire interface implementations as required.

A transport layer developed for the GOES-R mission, implements acknowledgement and retry functions that are required for reliable transport. Originally defined for the JWST mission [2] that did not complete implementation of it, the reliable delivery protocol was enhanced, streamlined, and validated with the GOES-R program using the Protocol Identifier (ID), which will be documented in a new standard ECSS-E-50-11 [6]. An application header byte was implemented in this core as part of the transport layer that allows the user to know if a logical address is present on the received data and which port the data came in on. Also an 8 bit CRC was implemented in hardware for the transport layer.

Adaptation of the Router to the On Chip Bus

A Router Interface (RIF) core is employed to adapt the SpaceWire router to the On Chip Bus (OCB) that acts as the ASIC common internal connection medium [3]. The RIF incorporates both transmit and receive Direct Memory Access (DMA) engines and FIFO buffers with a capacity of four 32 byte cache lines on both transmit and receive sides of the full duplex router. Linked descriptor lists stored in the OCB memory space control the DMA engines. They handle alignment between the 64 bit OCB and 32 bit SpaceWire router ports, with alignment supports on 32 bit boundaries. The interfaces to the DMA engines act as master interfaces on the OCB, while configuration and status information are provided via a separate OCB slave port. For fault tolerance, the RIF implements parity on the OCB and it uses "one hot" state machines for control. The RIF core also implements a Cyclic Redundancy Code (CRC) byte in hardware employing the polynomial used for the ATM standard as the last byte in the packet.

The SpaceWire router provides two bi-directional interfaces to the ASIC, each with 64 by 36 bit transmit and receive FIFOs (the extra bits are used for end of packet indication). Because the RIF core was designed to connect to this interface, two RIF cores are included in the ASIC. The RIF core and the SpaceWire router and links are coded at the RTL level in synthesizable VHDL, to allow easy porting to other technologies.

Reusable Cores Complete the Design

The balance of the SpaceWire ASIC consists of reused core designs already proven in the Enhanced Power PCI bridge ASIC. These include dual 32 bit Peripheral Component Interconnect (PCI) bus interfaces, compatible to level 2.2 of the standard. Each PCI interface has an independent clock domain, allowing them to run at different rates. This is particularly useful if one PCI interface is used for higher speed local connections while the second interface supports a multi-drop backplane bus. The PCI bus typically runs at 33 MHz when connected to a PCI backplane or 66 MHz or higher when used within a single card in a point-to-point connection. Both PCI interfaces contain a target, master, and arbiter functions to allow maximum flexibility options for interconnection.

The PCI buses can be used to connect multiple SpaceWire ASICs to be used as a larger router. If both buses are used, the ASICs can be connected in a point-to-point configuration that minimizes contention and arbitration on the PCI bus. In this configuration, daisy-chaining is employed if necessary to move through multiple ASICs. Logical addressing must be employed with the header maintained as the data crosses over the PCI bus to support the multiple routing tables. An additional application-specific header is added as data crosses from a SpaceWire link through the RIF to the OCB that identifies where the packet came from and defines whether the logical address is present. This unique header is removed prior to transfer of data across the PCI bus. This multiple ASIC configuration is shown in Figure 2.

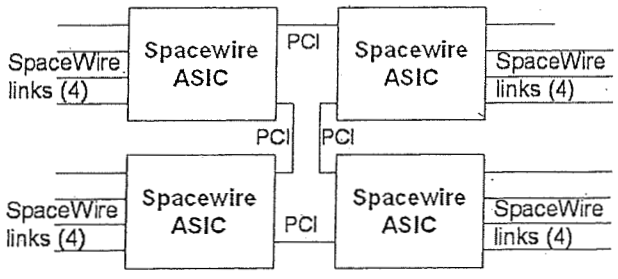

Figure 2: 16 Port SpaceWire Router Using Four SpaceWire ASICs

The Embedded Microcontroller (EMC) core provides support for the SpaceWire transport layer in this design.. It may also be employed to support the use of multiple ASICs operating as a larger router. The EMC controls the startup and configuration of the ASIC and manages the data traffic flow with the ASIC. The EMC is a 32-bit fixed point RISC processor with a 2KB instruction cache and its own complier developed by BAE Systems.

Test and debug are supported through use of a JTAG core, and a pair of 16 KB SRAM memories provide for scratchpad buffer space. Additional external memory (SDRAM, SRAM, EEPROM, etc.) can be accessed through the memory controller core. The DMA controller core provides the ability to transfer data to memory or any of the cores on the OCB from the PCI buses.

All of the cores connect to the common medium known as the On Chip Bus (OCB). The OCB consists of a high performance bus implemented as a non-blocking cross-bar switch with 64 bit data and word level odd parity and a lower performance 32 bit bus that supports 32 bit, 16 bit, and 8 bit data with word, half-word, and byte parity respectively. The OCB address bus is 32 bits. To support the throughput required with the SpaceWire transport layer, the high performance bus element of the OCB and all the interfaces to it can operate at speeds up to 75 MHz in this ASIC.

A block diagram of the SpaceWire ASIC is shown in Figure 3.

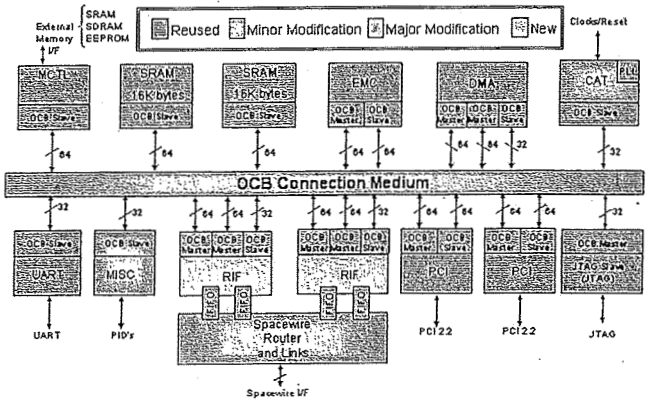

Figure 3: SpaceWire ASIC Block Diagram

Physical Implementation

The SpaceWire ASIC is implemented in a 0.25 micron bulk CMOS technology using the BAE Systems "R25" standard cell library specifically designed for radiation hardened applications [4]. The die is 12.7 mm by 12.7 mm. The design employs six layers of aluminum wiring and is connected to its ceramic column grid array (CGA) package via "flip-chip" mounting with collapsible solder balls. The 32.5 mm package supports 504 signal pins, of which the SpaceWire ASIC requires 423. The core voltage of the design is 2.5V with I/O at 3.3V. A screen shot of the SpaceWire ASIC that shows relative placement of the core functions is shown in Figure 4. The reusable cores (with exception of the RIF), the R25 library and process technology, and the CGA package are all at Technology Readiness Level 9 (TRL-9). The SpaceWire switch and link updates are considered to be at approximately TRL-7.

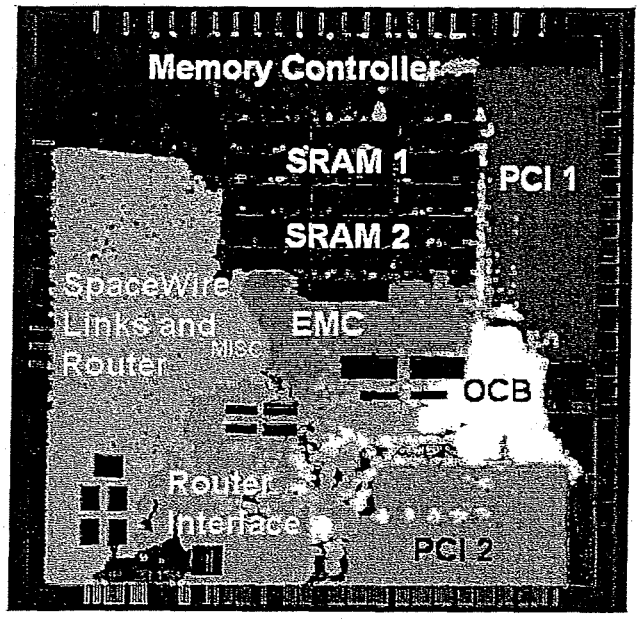

Figure 4: SpaceWire ASIC Layout Screen Shot

At the board level, the GOES-R and LRO programs are using the ASIC differently. For the GOES-R program, a CompactPCI (cPCI) board with the SpaceWire ASIC and additional memory chips has been developed that interfaces with a standard RAD750 processor board across the PCI backplane. For the LRO program, a unique processor board has been designed to NASA specifications, which locates the SpaceWire interface on the processor board itself. This configuration results in a board with multiple PCI loads on the backplane that is not consistent with the PCI standard but that meets NASA's requirements.

SpaceWire ASIC Functional Test Results

The first pass SpaceWire ASIC hardware is currently in functional testing and is working as designed. Early testing has been performed at room temperature. The GOES-R customer successfully tested all functional threads of the SpaceWire ASIC on their cPCI memory board against a pair of SpaceWire testers developed for the James Webb Space Telescope (JWST) mission as a first step and has moved on to testing the chip using two of the cPCI memory boards. Note the SpaceWire core has undergone basic compatibility testing with the leading commercial SpaceWire vendors. The ASIC has been tested up to 132 MHz, only because that meets the test program requirements for the projects using the chip. Testing the links at the full rate will be performed to complete the verification of the chip. An ambient temperature lab version of the LRO processor board with the SpaceWire ASIC has also recently been delivered to the LRO program for software development and demonstration purposes.

The BAE Systems "R25" 0.25 micron CMOS standard cell circuit library has already been fully validated across the military spec temperature range and has been characterized for resistance to all radiation characteristics. In addition, ASICs based on this circuit library and package are already successfully flying space missions. At this time, explicit radiation testing of the SpaceWire ASIC is not required to validate it for flight. The R25 technology, which is utilized for the RAD750 and Power PCI bridge ASICs as well as the Millennium SRAM, provides for 200 Krad (Si) Total Ionizing Dose and an SEU rate of <1E-9 upsets/bit-day. Qualification testing of the SpaceWire ASIC is in progress with flight qualified modules available in the 4th quarter of 2006.

BAE Systems SpaceWire Roadmap

BAE Systems is committed to long-term use of the SpaceWire protocol. There are already two additional ASIC designs in progress that will incorporate the SpaceWire interface, as shown in Figure 5. The next generation of the Power PCI bridge chip, the companion chip to the RAD750® microprocessor, adds the SpaceWire core with the 4-port router in addition to other new functions. All of the existing and newly added functions are created from fully synthesizable reusable cores. This ASIC will be manufactured in the RH15 150nm radiation hardened technology on the BAE Systems CMOS process line in Manassas. The integration of the SpaceWire router into this ASIC enables fully cPCI compatible RAD750 flight and payload processor boards that support the

SpaceWire protocol while also saving board area and decreasing power dissipation.

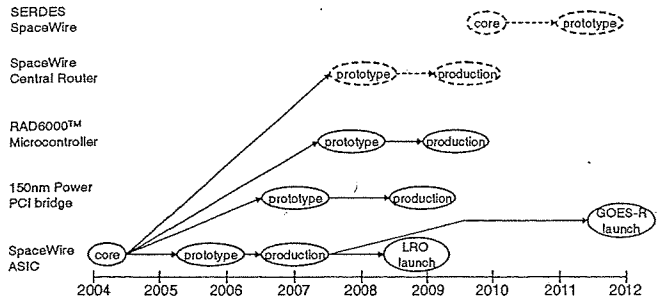

Figure 5: BAE Systems SpaceWire Roadmap

The second ASIC currently in design that employs the SpaceWire protocol is the RAD6000™ microcontroller. This ASIC is also to be built in RH15 technology based on existing and new reusable logic, analog, and memory cores. The original plans for this ASIC accounted only for a pair of SpaceWire link ports, but this will probably be upgraded to support either 2 links or a 4 port router based on the required vs. available die area. This ASIC will provide SpaceWire support to instruments, robotic appendages, and other subsystems that require direct interface to sensors and actuators.

building blocks. One option is the development of either a 16 or 24 port central router chip that would provide for extensive SpaceWire networks without the need to "daisy-chain" from chip to chip. As shown in Figure 6, this comprehensive set of building blocks will allow development of a fully SpaceWire enabled spacecraft.

Another future possibility is the extension of the SpaceWire interfaces to multi-Gigabit performance high speed serial links commonly referred to as SERDES links in a standard that is expected to be formalized as "SpaceFibre" during 2006. The new Gigabit interfaces will be able to bridge between original SpaceWire ports via the switch (router), which can incorporate both kinds of interfaces. One last addition that may be incorporated, is the primary/redundant physical layer interface logic developed by JWST [5], which allows a switch-over from a failed link to a alternate link similar to MIL-STD-1553. This mechanism is transparent to the user and may be disabled to be fully complaint with the SpaceWire standard.

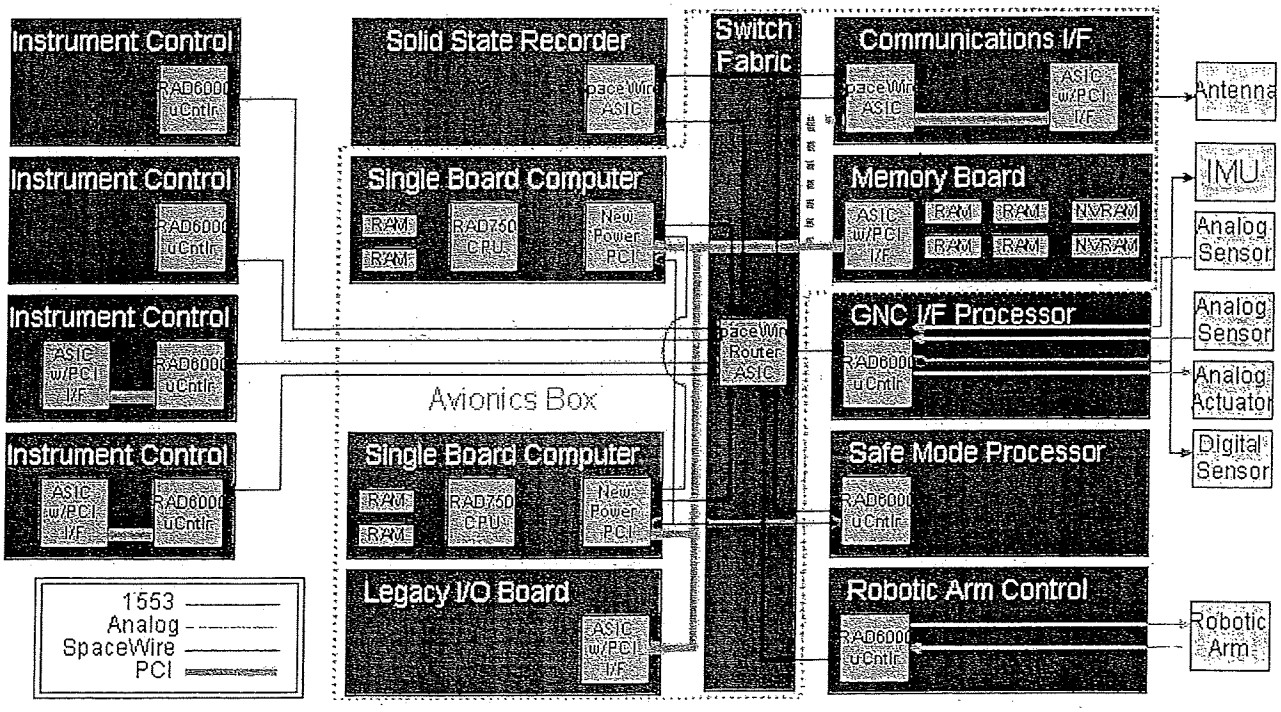

Figure 6: Example SpaceWire Enabled Spacecraft System

In the longer term, BAE Systems and GSFC have discussed the possibility of additional SpaceWire

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