A Technical and Cost Perspective on Radiation Testing Challenges

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To be presented by Kenneth LaBel at the Microelectronics Reliability and Qualification Workshop (MRQW), Los Angeles, CA, 12/4/06-12/7/06

Outline of Presentation

- **Introduction – a Changing Microelectronics World**
- **Sample Technology Changes and Related Impacts on Radiation Testing**
  - **Silicon, Circuit/Process, Packaging**
- **Perspective on the "New" Cost of Doing Business**
- **Considerations**

Latent damage sites: device did not fail during ground irradiation, but at some time afterward

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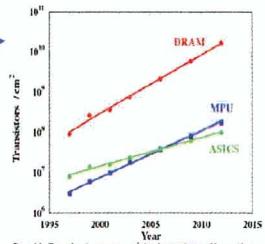
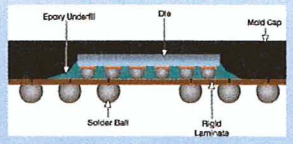
Microelectronics Technology Trends

- Scaling trends (smaller feature size) resulting in:
  - Increased gate/cell density per unit area (as well as power and thermal densities)
  - Lower supply and logic voltages (≤1V)
    - Reduced electrical margins in a single IC
  - Changes in materials
    - Use of anti-fuse structures, phase-change materials, alternative K dielectrics, Cu interconnects (previous – Al), insulating substrates, ultra-thin oxides, etc…
    - New material leading to unknowns in radiation response and physics of failure



- Increased device complexity
  - More functions per chip: >1 billion gates in a single device
  - Increased number of levels of metal
  - Heterogeneous integration
- Increased operating speeds to >> GHz (CMOS, SiGe, InP, ABCS)
- Increased package complexity
  - Use of flip-chip, area array packages, etc
- Increased importance of application specific usage to reliability/radiation performance



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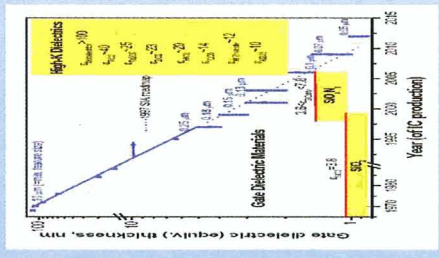
3

Technology Engendered Challenges for Radiation Effects

- Reduced feature size and Increased integration density
  - Lower upset thresholds due to reduced operating voltages and nodal capacitance
  - Increased probability of multiple bit upsets due to increased packing density & charge sharing
  - New materials resulting in unknowns concerning radiation response (dose enhancement) and FIT projection (materials physics of failure)
- Increased circuit complexity
  - Increased number of failure modes, e.g. SEFI
  - Increased difficulty in test and evaluation of all operating modes, e.g. time for complete node coverage approaching infinity
  - Unobservable and uncontrollable states
  - Radiation sensitivity as a function of operation
  - Added probability of nuclear reactions with metal layers, e.g. low LET particles causing upset through secondary production
- Increased circuit operating speed
  - Need for higher speed test equipment and/or approaches
  - Test facility arrangements
  - Device temperature control
- Packaging complexity
  - Issues with respect to test ions package penetration, e.g. higher beam energy test facilities required
  - Shadowing of critical nodes/ Critical nodes covered by metal layers
- Modeling and simulation
  - 3-D and mixed-mode models required
  - Over-layer and substrate interaction must be included
  - Simulation time



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4

Microelectronics Technology Roadmap

- **Sample Issue: the scaling of feature size and closeness of cells**
- **Technology complications**
  - **Multiple node hits with a single heavy ion track**
    - **Due to transistor proximity and thinness of the substrate material.**

Litho International Tech Roadmap

Lithography Technology Requirements – ITRS 2001 Update

Start Production	2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
Logic Half Pitch (nm)	150nm	130nm	107nm	90nm	80nm	70nm	65nm	45nm	32nm	22nm
Logic Gate in Resist (nm)	90nm	70nm	65nm	53nm	45nm	40nm	35nm	25nm	18nm	13nm
DRAM Half Pitch (nm)	130nm	115nm	100nm	90nm	80nm	70nm	65nm	45nm	32nm	22nm
Contact in Resist (nm)	165nm	140nm	130nm	110nm	100nm	90nm	80nm	55nm	40nm	30nm
Overlay	45nm	40nm	35nm	32nm	28nm	25nm	23nm	18nm	13nm	9nm

Source: ITRS

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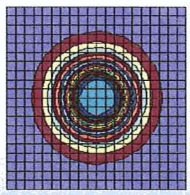
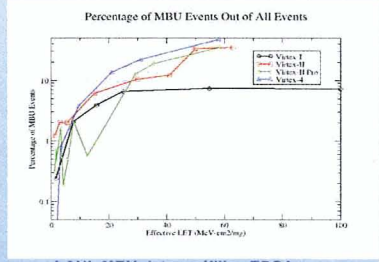
5

Feature Size and Density Implications

- **Multiple node hits**
  - **Charge sharing from critical node strikes**
    - **A single particle strike can spread charge to multiple cells. If the cells are logically as well as physically located**
      - **Standard memory scrub techniques such as Hamming Code can be defeated**
    - **This is not new, simply exacerbated by scaling. Traditional SEU modeling considers particle strikes directly on a transistor**
  - **Charge spreading for strikes near but not on the transistor can generate errors**
    - **Measured error cross-sections may exceed physical cross-sections**
    - **More targets and the spread of non-target hits implied potentially increased error rates per device**
  - **The role of particle directionality and of secondaries becomes critical**
    - **Modeling requires use of physics-based particle interaction codes coupled with circuit tools.**
    - **GEANT4, MCNPX, etc. are the type of codes required**
      - **Efforts begun to turn these into tools and not just science codes**
    - **Impact of metalization**



Charge spreading from a single particle in an active pixel sensor (APS) array impacts multiple pixels



LANL MBU data on Xilinx FPGAs

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6

Integration Density Issue Impacting Test and Evaluation

Example: State-of-the-art Commercial Memory

32k x 8 SRAM circa early 1990's
Feature size is 0.8 to 1.25 um

1 Gb SDRAM circa 2006
Feature size is 90nm

When the current "accepted" SEE test methods were written, large memory devices were on the order of 256 kb (say ~1E5 cells), current state of the art memories exceed 1 Gb (1E9 cells). These existing test methods typically use 1E7 ions/cm² as test run particle fluences. With the old devices, probabilities favored that every cell was hit (ie., an overtest of 100x). In the new devices, something on the order of 1% of the cells are hit during a test run. This lack of conservativeness provides issues for statistics, small probability events, etc…

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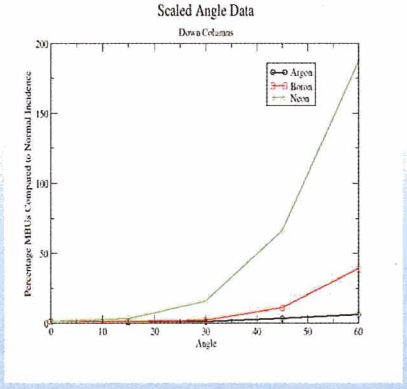
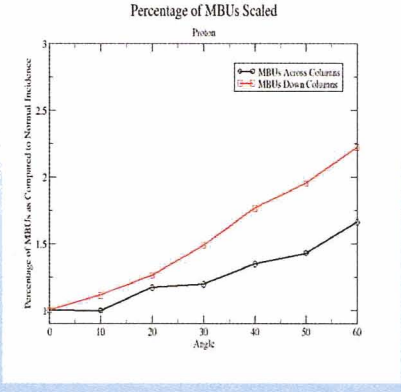
7

Importance of Angular Effects

Example: State-of-the-art FPGA





As seen here in a 90nm FPGA, the relative number of multiple bit upsets (MBUs) for both heavy ion and proton SEE varies significantly with particle interarrival angle.
Coupling the omnidirectional event with this angular effect and adding in the effects caused by secondary reactions from materials with the IC/package complicates interpretation of test data, beam requirements, and rate prediction techniques.

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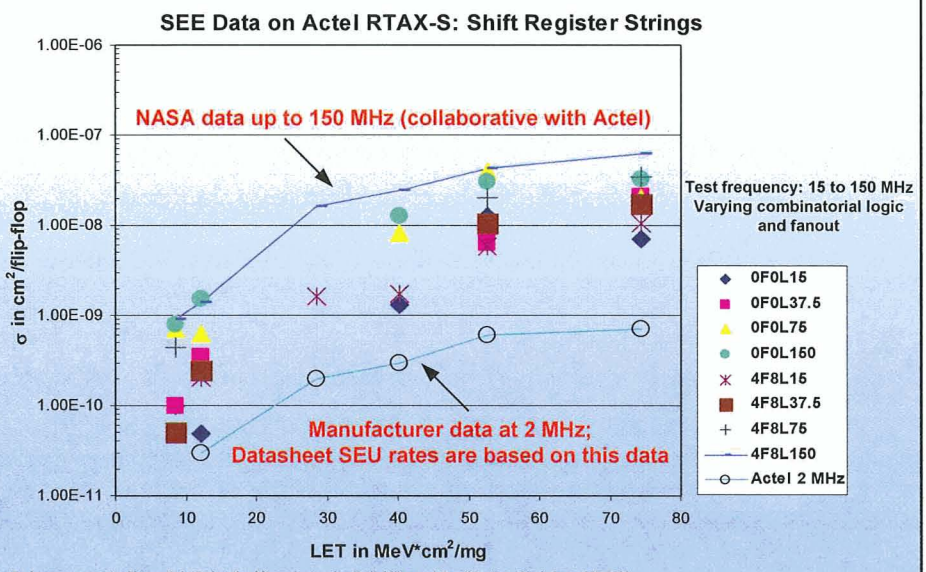
8

Importance of Operating Frequency-Specific Results

***Example:** First at speed SEE data on Actel RTAX-S FPGA*



Operating Speed Implications

Testing at a remote facility requires highly portable test equipment capable of high-speed measurements

- **Tester needs to be near the device or utilize high-speed drivers**
  - **Cable runs between the device under test (DUT) and the tester can be up to 75 feet**
- **Simple devices like a shift register chain can be tested using bit error rate testers (BERTs)**
  - **BERTs can run to ~$1M and tend to be very sensitive to problems from shipping**
    - **At proton test facilities secondaries are generated (neutrons) that can cause failures in the expensive test equipment if they are located near the DUT**
  - **Self-test techniques for testing devices being developed for shift-register structures**
- **Modern reconfigurable FPGA-based test boards being developed to test more generic devices**
  - **Daughtercard or embedded DUTs**

Beware of stray neutrons impinging on your test equipment. Here, Borax is shown on top of a power supply to absorb neutrons.

Operating Speed Implications

- **Testing in a vacuum chamber implies mechanical, power/thermal, and hardware mounting constraints**
  - **High-speed devices often mean high power consumption**
    - **Issue is mounting of DUT in vacuum chamber and removal of thermal heat**
      - **Can also be a challenge NOT in a vacuum**
      - **DUT may need to be custom packaged to allow for thermal issues**
    - **Active system required for removal of heat**
- **Open air facilities help, but have often have other considerations**
  - **Cost**
  - **Accessibility**

Brookhaven National Laboratories' Single Event Upset Test Facility (SEUTF)

Vacuum Chamber

User equipment area

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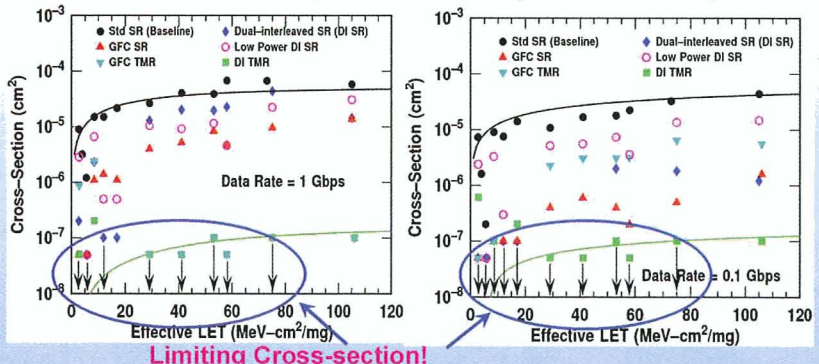
11

SiGe Radiation Evaluation and Modeling –

Working collaboratively with technology development programs



Limiting Cross-section!

Evaluating SEE Rad Hard by Design (RHBD) Approaches:

Dramatic SEE improvements in SEE sensitivity on 8HP HBT

Data Rates can run to >>10 GHz!

MAYO CLINIC

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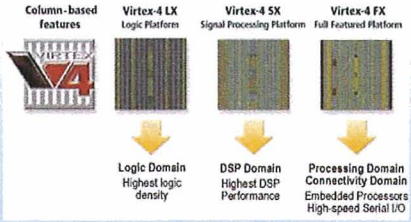
BOEING

Complexity Implication

- **Example: SRAM-based reprogrammable FPGA-measuring sensitivity of user-defined circuit**
  - **SEE in configuration area corrupts user circuitry function**
    - **Can cause halt, continuous mal-operation, increased power consumption (bus conflicts), etc.**
  - **Often the sensitivity of the configuration latches overwhelm user circuitry sensitivity**
    - **Must have correct configuration to measure user circuit performance**
- **Increased number of control structures in a device drives an increasing rate of single event functional interrupts (SEFIs)**

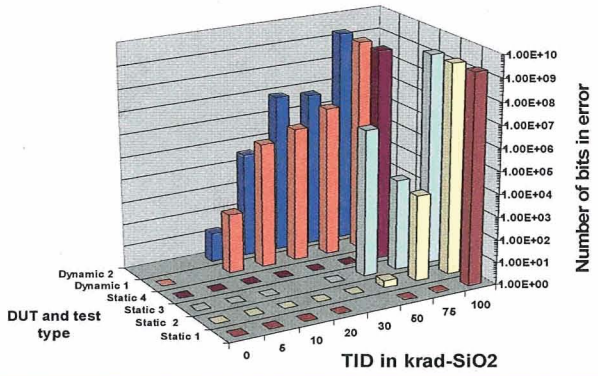


Complex new FPGA architectures include hard-cores: processing, high-speed I/O, DSPs, programmable logic, and configuration latches

Importance of Mode-Specific Results

Example: State-of-the-art Flash Memory Evaluation

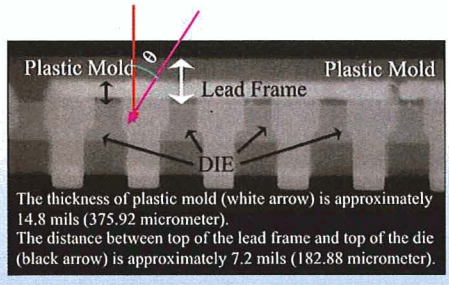
Micron 2Gb NAND Flash - Number of Bad Bits
90 nm CMOS



Failures noted in dynamic mode at << cumulative dose levels than static mode. Some devices like an SDRAM may have >>50 operational modes.

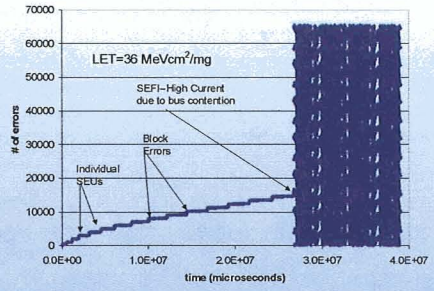
State-of-the-art SDRAM Memory Evaluation

Challenges for test preparation and data collection/analysis



X-Ray Photo of a DUT

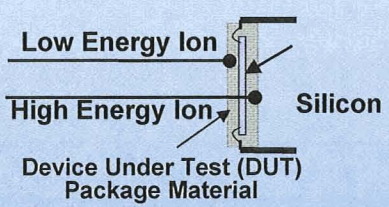
Determining effective LET as a function of angle requires correcting for the energy lost by the ion as it traverses overburden to the sensitive volume, as well the usual 1/cosθ dependence.



Real-time error counts during a test run:
Different types of errors have different signatures, Complicating data collection, test decision making, and analysis

Complexity Implications

- Macro-beam structure: implies probabilistic chance of hitting a single node that may be sensitive
  - If test is run for SEE, typical heavy ion test run is to 1x 10^7 particles/cm².
    - Ex., SDRAM – 512 Mb (5x10^8 bits plus control areas)
      - If all memory cells are the same, no issue. BUT if there are weak cells how do you ensure identifying them?
      - Control logic may be a very small area of the chip. If you fly 1000 devices, area is no longer "small"
  - Difficult to evaluate clock edge sensitivity of a node
- Die access (required for most single event testing)
  - Typical heavy ion single event macro-beam simulators have limited energy range
    - Implies limited penetration through packaged device
    - Access to die typically required
      - Overlayers, metalization, etc must be taken into account



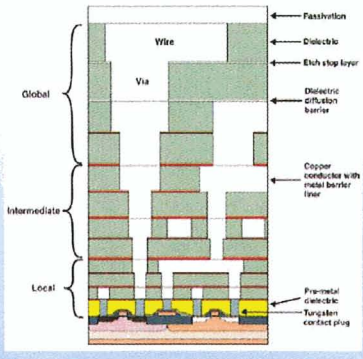
Facility	Ion (Energy)	LET (Si)	Range in Si (μm)	Peak LET
NSCL	Xe (3.2 GeV)	40	272	69
TAMU	Ar (2 GeV)	5.9	390	18

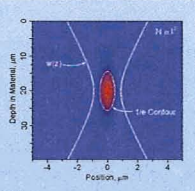
Table assumes ion traverses 1.5 mm plastic LET given in MeV-cm²/mg

Complexity Implications

- **Standard microbeam and laser test facilities have similar limitations for range of particle**
  - **On older technologies, these facilities are used to determine what structure within a device is causing fault/failure**
  - **New technique (two-photon absorption - TPA) with the laser is being developed, but is still in research phase**
  - **New test structures built specifically for test may be required**
    - **Reduced metalization, special packaging, etc.**

Typical Chip Cross Section



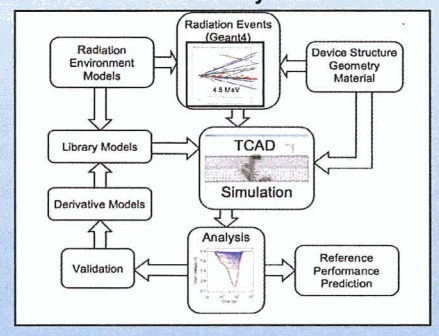


TPA is a new technique to overcome some of the test limitations from packaged device and metalization issues.
Courtesy Dale McMorrow, NRL

Modeling and Simulation Implications

- **While not the focus of this talk, related issues existing for modeling and simulation**
- **Reference programs include**
  - **VU RADSAFE Simulation System**
  - **TCAD model development**

RADSAFE System



SET Mixed-Mode Model

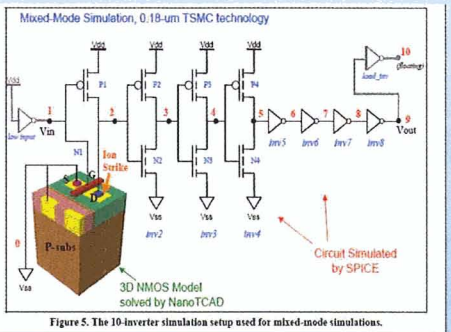


Figure 5. The 10-inverter simulation setup used for mixed-mode simulations.

The Increasing Cost of Doing Business -

Example: Radiation Single Event Effect Test Costs
Qualification Testing of a Commercial Memory – 1996 to 2006 (1 of 2)

- **Device under test (DUTs): Commercial Memory**
  - For use in solid state recorder (SSR) applications
- **1996**
  - SRAM memory
    - 4 Mbits per device
    - <50 MHz bus speed
    - Ceramic packaged DIP or LCC or QFP
- **2006**
  - DUT: DDR2 SDRAM
    - 1 Gbit per device
    - >500 MHz bus speed
    - Plastic FBGA or TSOP
    - Hidden registers and modes
    - Built-in microcontroller

- **Issues**
  - Size of memory
    - Drives complexity on tester side for amount of storage, real time processing, and length of test runs
  - Speed
    - Difficult to test at high-speeds reliably
      - Need low-noise and high-speed test fixture
    - Classic bit flips (memory cell) extended to include transient propagation (used to be too slow a device to respond)
    - Thermal and mechanical issues (testing in air/vacuum)
  - Packaging
    - Modern devices present problems for reliable test board fixture, die access (heavy ion tests) requiring expensive facility usage or device repackaging/thinning
    - Difficulty in high-temp testing (worst-case)
  - Hidden registers and modes
    - Functional interrupts driving "anomalous data"
      - Not just errors to memory cells!
  - Microcontroller
    - Not just a memory

Example: Radiation Single Event Effect Test Costs

Qualification Testing of Commercial Memories - 1996 to 2006 (2 of 2)

1996 SEE Test of a 4M SRAM

Description	Man-weeks or units	Cost in $	Total	Note
Heavy Ion at BNL SEUTF				Includes eng, rad, other to define what needs to go into test set with project.
Test plan	0.20	$4,000.00	$800.00	
Device procurements	10.00	$50.00	$500.00	
Misc parts	1.00	$250.00	$250.00	Sockets, connectors, etc...
Device delidding	0.05	$3,500.00	$175.00	
Test board design - electrical and layout	0.40	$4,000.00	$1,600.00	
Board fab and population	1.00	$3,500.00	$3,500.00	In-house board build
Board/tester debug	0.50	$4,000.00	$2,000.00	
Rad expert (test oversight and plan)	0.40	$5,000.00	$2,000.00	
Heavy ion test performance - contractor	2.00	$1,500.00	$3,000.00	
BNL Beam	6.00	$700.00	$4,200.00	Simple data: bit flips, latchup
Data analysis	1.00	$3,500.00	$3,500.00	
Test report (eng, rad expert, rad lead)	0.50	$4,000.00	$2,000.00	
		Total:	$23,525.00	

2006 SEE Test of SDRAM

Description	Man-weeks or units	Cost in $	Total	Note
Heavy Ion at TAMU				Includes eng, rad, other to define what needs to go into test set with project.
Test plan	1.00	$4,000.00	$4,000.00	
Device procurements	10.00	$75.00	$750.00	
Misc parts	1.00	$1,000.00	$1,000.00	Higher speed drives cost
Device thinning and package processing	10.00	$350.00	$3,500.00	Assumes FBGA package; if this does not work, more expensive test facility like NSCL needed: >$100K delta
Daughterboard Board design - electrical	0.40	$4,000.00	$1,600.00	
Daughterboard Board design - PCB	0.50	$3,500.00	$1,750.00	
Test Boards	10.00	$500.00	$5,000.00	
Board population	0.40	$3,500.00	$1,400.00	
Board/tester debug	0.50	$4,000.00	$2,000.00	
Tester VHDL development	3.00	$4,000.00	$12,000.00	
Technician	1.00	$3,500.00	$3,500.00	
Rad expert (test oversight and plan)	0.60	$5,000.00	$3,000.00	
Heavy ion test performance - contractor	2.00	$2,000.00	$4,000.00	
TAMU	16.00	$750.00	$12,000.00	2X time required: more data, more error types, more complex results
Data analysis	3.00	$3,500.00	$10,500.00	
Test report (eng, rad expert, rad lead)	1.00	$4,000.00	$4,000.00	
			Total in	$70,000.00

1996 vs 2006 a 3X Cost Delta

Other test costs (radiation and reliability) have increased commensurately!

Hypothetical New Technology Part Qualification Cost

Item	Cost	Note
Parts Procurement (500-1000 devices for testing only)	$25-1000K	Individual device costs can run from cents to tens of thousands
Standard Qualification Tests	$300K	
Radiation Tests and Modeling	$400K	Assumes total dose and single event (heavy ion) only
Failure Modes Analysis	$300K	Out-of-the-box look at the "hows and whats" for non-standard research required for qualification
Additional Tests, Modeling, and Analysis based on Failure Modes	$500K	
Total cost for one device type	$1.5-3M	Not all new technologies will meet standard qualification levels: technology limitations document

Assumption: 12-24 months to develop sufficient data for technology confidence

Summary

- **Challenges include**
  - **Impact of new materials and manufacturing methods on long term radiation response**
  - **SEFI in deep-submicron microprocessors, microcontrollers, SDRAM and other complex**
  - **Testing at operating speed for SET characterization and SER prediction.**
  - **Test fidelity issues resulting from facility beam energy limitations**
    - **SEE strike angle dependence**
    - **SEU and SEL caused by very high energy proton interaction with high-Z metal layers**
  - **Modeling and simulation fidelity; 3-D models required for deep-submicron devices**
- **Programs exist to address these issues but the level of investment is not keeping pace with the complexity and number and problems identified**
  - **Evaluations often being undertaken AFTER insertion into program designs**
    - ***RISK!***