SEU and Test Considerations for FPGA Devices

Melanie Berg
Muniz Technologies Incorporated
NASA/GSFC Radiation Effects an
Analysis Group

Outline

- Field Programmable Gate Array (FPGA) Background
  - Definition
  - Implementations in space missions
  - Available Technologies
- Single Event Upsets (SEUs) and Single Event Transients (SETs)
  - Definition
  - How they Effect FPGAs
- Testing
  - Goals
  - Considerations
  - Data Analysis
- Summary

What's the Issue?

Faulty Chips Delay Launch of Japanese Imaging Satellite

PAUL KALLENDER-UMEZU, TOKYO
MISSY FREDERICK, WASHINGTON

The Japanese government has decided to postpone the launch of the nation's next reconnaissance satellite by six months or more following the discovery of potentially defective integrate-circuits in the satellite, a government official said August 26.

The Prime Minister's Cabinet Office, which is in charge of the nation's Information Gathering Satellite (IGS) program, decided Aug. 25 to postpone the launch of what would be the nation's third reconnaissance satellite in orbit after deciding it was necessary to replace a number of field programmable gate array (FPGA) chips made by Actel Corp. of Mountain View, Calif., according to Yasuhiro Itakura, research officer at Japan's Cabinet Satellite Intelligence Center, which is part of the Cabinet Office.

The satellite, which carries an optical sensor, was to have been launched by a Japanese H-2A rocket from the Tanegashima Launch Center before the end of March 2006, but it will take about six months to replace the potentially faulty chips and test the satellite to prepare it for flight, Itakura said in an August 26 telephone interview.

Some 10 chips need to be replaced, he said. Details about when the problem was discovered were not available at the time of the interview.

Problems with Actel's earlier version of its FPGA were discovered in autumn 2003, after more than 1 million of the devices were shipped to various vendors.

Ken O'Neill, director of military and aerospace product marketing for Actel, said after news of the defect became known, Actel supplied the Japanese government with the latest version of the company's FPGA, which the company has the option to install in place of the old version. Since then, the government has been doing reliability testing of both the old and new product, though Actel had not received official [redacted] extensively, and clearly show a very high level of reliability," O'Neill said. "We have confidence that the reliability of the earlier version is high, but the latest version of the software does offer a higher level of reliability," he said.

FPGAs contain hundreds of thousands of programmable elements, according to O'Neill, and the defect found in the old version of the chips affected one antifuse within the design, causing it to fail. O'Neill said the chips that do fail usually do so early in the lifetime of the part.

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The IGS program was developed in response to an August [redacted] failed.

Comments: mfrederick@space.com

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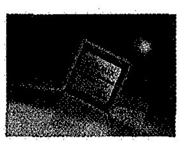
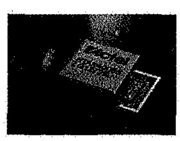
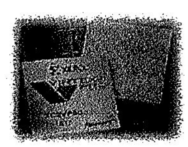
Field Programmable Gate Arrays (FPGA)







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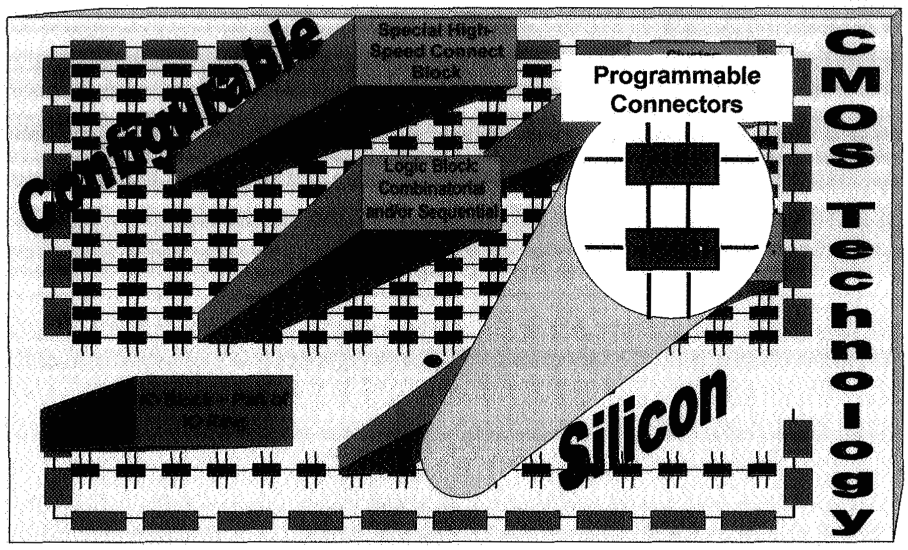
General FPGA Architecture



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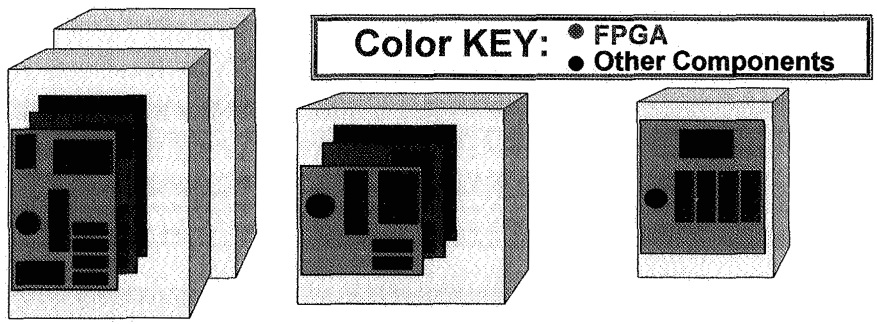
Role of FPGA/ASIC Devices within Space Missions



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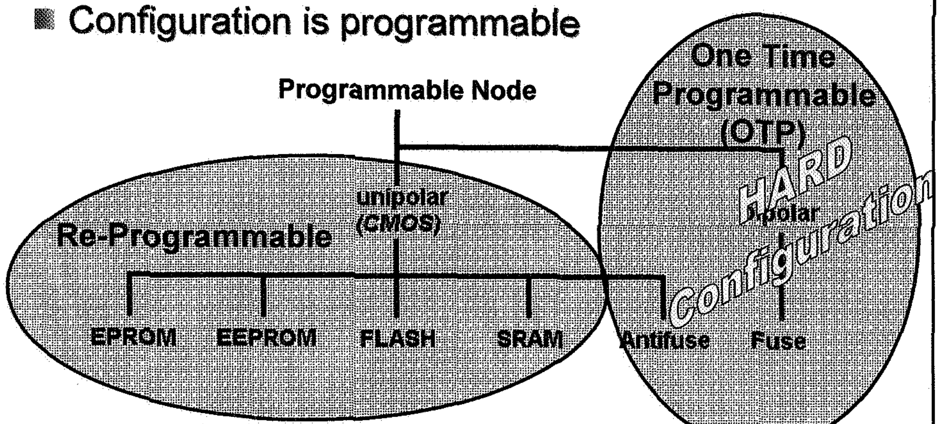
Configuration: Key Difference in FPGA Technologies

- Configuration defines: Functionality and Connectivity
- Configuration is programmable



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Single Event Upsets (SEUs) and Single Event Transients (SETs)

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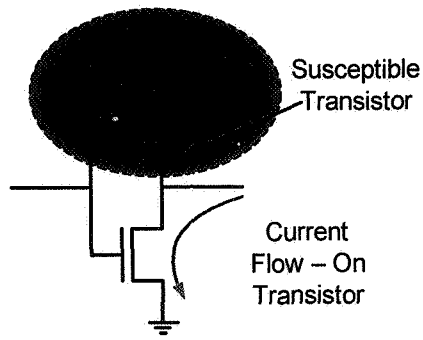
Single Event Upsets (SEU) and Single Event Transients (SET)

- CMOS transistors have become more susceptible to incurring faults.
- Why?
  - reduction in core voltage
  - decrease in transistor geometry
  - increase in switching speeds,
- A Fault Occurs when a transistor that is turned off:
  - Collects Charge at the drain
  - turns on with enough charge to change the state of the output



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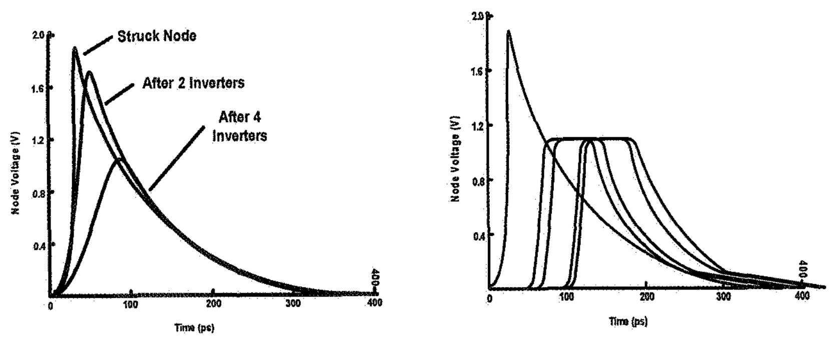
Transient Generation and Propagation



Add something about set capture in dff

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How do SEUs and SETs Effect FPGAs?

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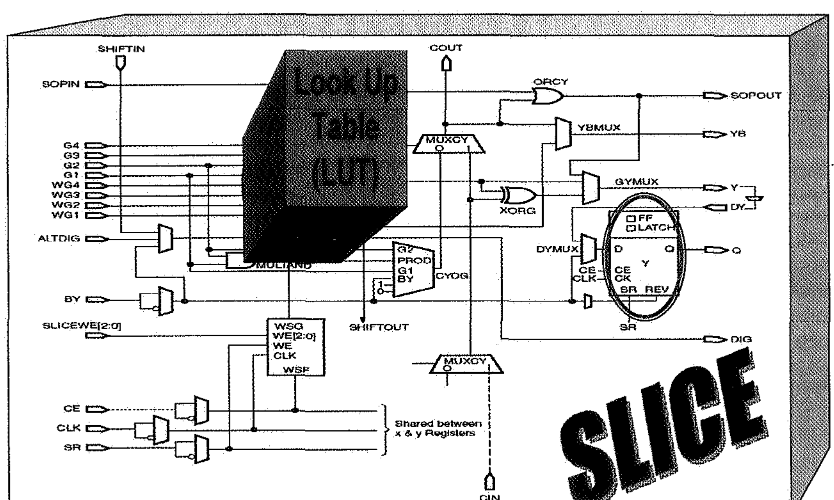
Example 1: Xilinx and the Complexity of a Configuration Logic Block (CLB)



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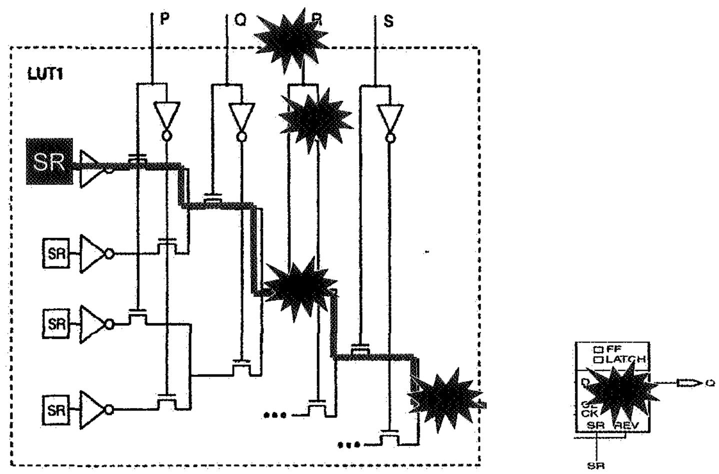
Example: Susceptibility in a Xilinx 4-Input Look Up Table (LUT)



Example 1: Summary....How Do SET's/SEU's Effect Xilinx FPGAs?

- Configuration Memory hit:
  - Largest area of concern for the Device
  - The entire FPGA can become un-configured.
- Logic/Connector Hit
  - *Frequency dependency*: SETs can be caught by Flip-Flops
  - *Frequency independent*: SEU can occur in Flip-Flop
- Single Event Functional Interrupt (SEFI): Hits to
  - Power On Reset
  - Configuration Control logic
- **What considerations must be taken to test for these conditions?**

Testing Complex FPGA Implementations Targeted for Critical Missions

Choosing the Most Cost Effective FPGA for a Project with Critical Requirements

- Define realistic Requirements
- Trade-offs:
  - Reliability
  - Performance
  - Schedule
  - Total Cost
- Define a methodology for trade-off analysis
- Radiation Testing is key and can be broken into 2 major categories:
  - Characterization:
    - General device study
    - Simple Test structures
  - Qualification
    - Project specifics
    - Test structures may be more complex

We'll Focus on Device Characterization

Goals for Device Characterization

- How radiation-tolerant (in general) is the Device Under Test (DUT)?
- Test for:
  - Clock Tree Susceptibility
  - Rest Tree Susceptibility
  - Sequential logic Hardness
  - Combinatorial Error Cross-Section Contribution
  - I/O Susceptibility
  - Single Event Functional Interrupts (SEFI)
  - Configuration Memory Susceptibility **(SRAM –Based Only)**

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DUT Radiation Test Strategies

- Push the limits of the DUT.
  - Timing variations (very slow to fastest clock rates)
  - Types of logic cells (check device technology library)
  - Fill Device with logic
  - Safe I/O strategies
- Designs should be simple so that faults are not masked and undecipherable.
- Designs should represent realistic implementations
  - Proper reset structures
  - Synchronous design techniques
  - Various levels of combinatorial logic between DFF structures
  - Fanout variation

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Common DUT Characterization Test Structures

- Shift Register Strings (sequential logic)
- Combinatorial Clouds of logic between (sequential cells)
- Large quantities of I/O to accommodate data variation, system clock rate variation, design interfacing, and I/O susceptibility testing

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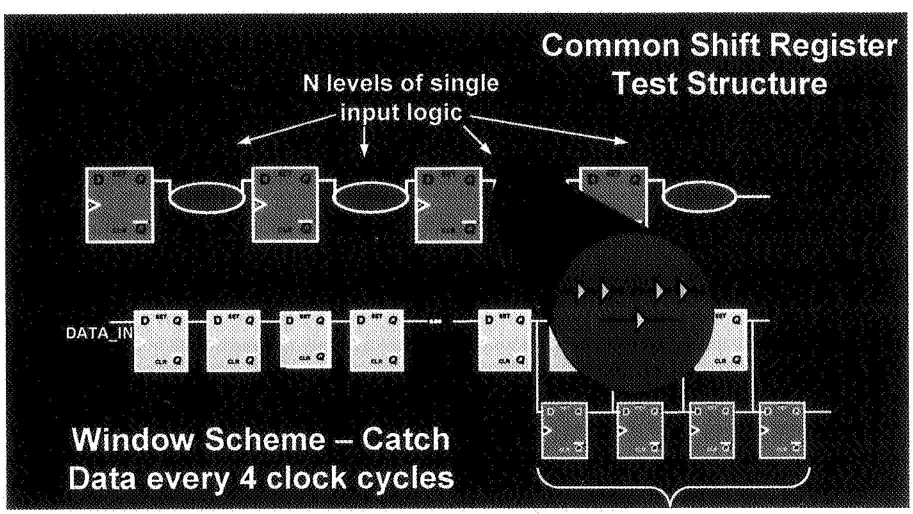
Testing Sequential and Combinatorial logic



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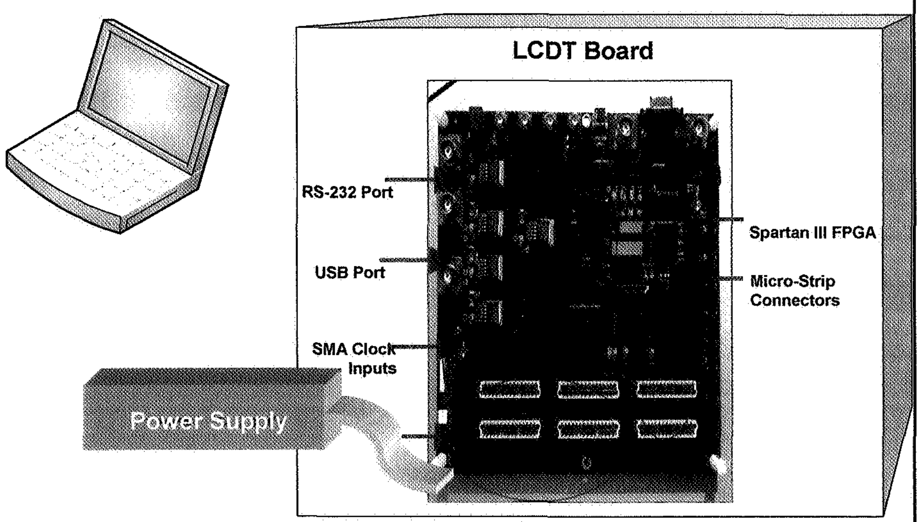
Tester Radiation Test Strategies

- Attention to Timing Characteristics of the DUT
- Application of corner case input variations (stress the part)
- Deterministic DUT Data Capture
- Tester to DUT Interface Limitations
  - Number of I/O
  - Simultaneously Switching Outputs (SSO)
  - Interface connector speed

NASA GSFC Low Cost Digital Tester



Analyzing Test Data – Asking the Right Questions

- Does the device stay configured?
- Is the DUT schematic supplied?
- Is the DUT implementation a reliable design?
  - Synchronous design techniques
  - "Single Integrity" solution applied
- How reliable is the supplied inputs and data capture scheme of the tester?
- What are the maximum and minimum frequencies supplied to the DUT during test and how do they relate to the timing specifications of the device?
- What are the data rates? (May be difficult to determine for complex designs)
- Are there SEFIs
- Is there speed degradation?

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Data Analysis Example

- Actel Corporation and NASA-GSFC collaborated in supplying SEU RTAX-S device specific data
- Data was supplied at 2MHz testing frequency
- Simple shift register test structures were implemented
- Question: Was the supplied data an Efficient characterization of the devices?

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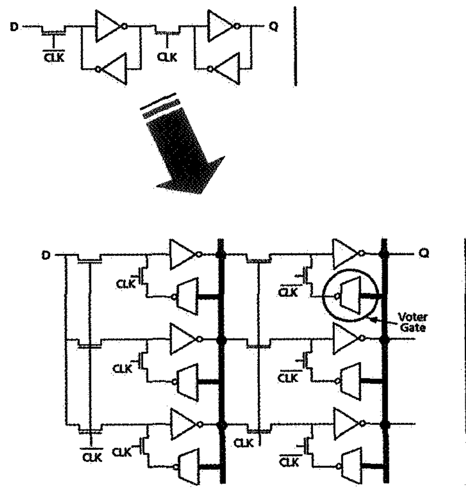
Actel Logic Blocks: Sequential and Combinatorial

- RCELL (Sequential):
  - Triple Mode Redundant (TMR) Mitigation
  - Inputs are shared (single points of failure)
  - contains more logic (not shown)
    - 2 MUXs one for logic and one for clocking)
    - Adds more sources of failure
- CCELL (Combinatorial):
  - Logic Block is generally a MUX structure
  - Addition of block should increase error cross section as frequency increases



Actel Expectations: SET Frequency Response

- In general ...Combinatorial.....
- RCELL contains some
- CCELL should make a considerable contribution due to frequ dep

Data Analysis Example (Continued)

- Another effort between Actel and NASA-GSFC was undertaken
- Clock Rates were supplied to the DUT from 15MHz to 150MHz
- DUT Input Data:
  - Alternating data was supplied at half the clock rate
  - Static "0"
  - Static "1"
- Several Designs were implemented to analyze the potential increased susceptibility to transients when utilizing C-CELLS
- Synchronous Design Approach was implemented in the DUT and in the tester.

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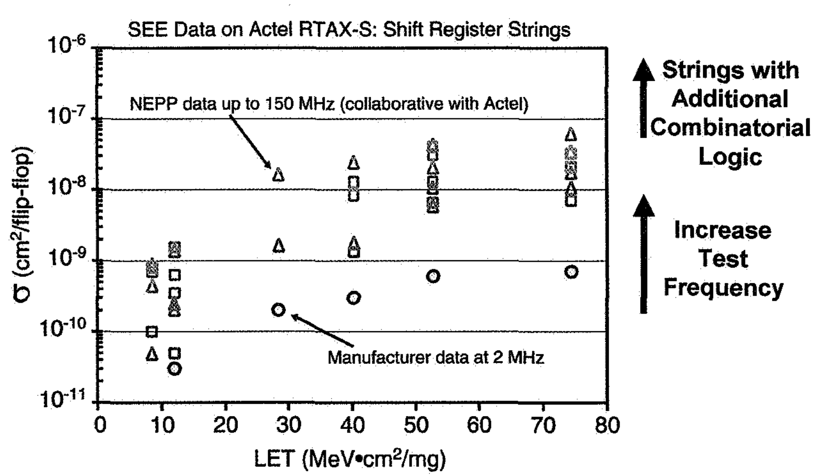
RTAX-S Data: Earlier and Current Test Data



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Survey – Why Was the Original 2MHz Data Acceptable?

- Asked Engineers and Physicists.
- Here's the Best of:

Engineers:

- Told Frequency dependency does not exist
- Was not aware of transients and their effects in circuitry

Physicists:

- Based on the new 150MHz, the original assumption that the data is scalable holds true – (2Mhz to 150Mhz testing should result in about 2 orders of magnitude between data sets

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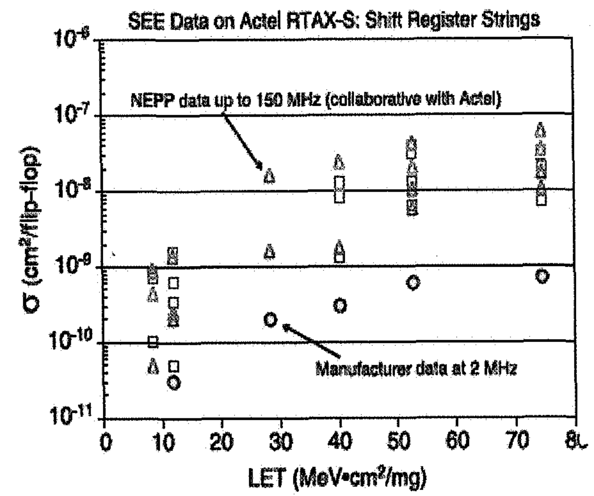
2 Orders of Magnitude is True in this Case



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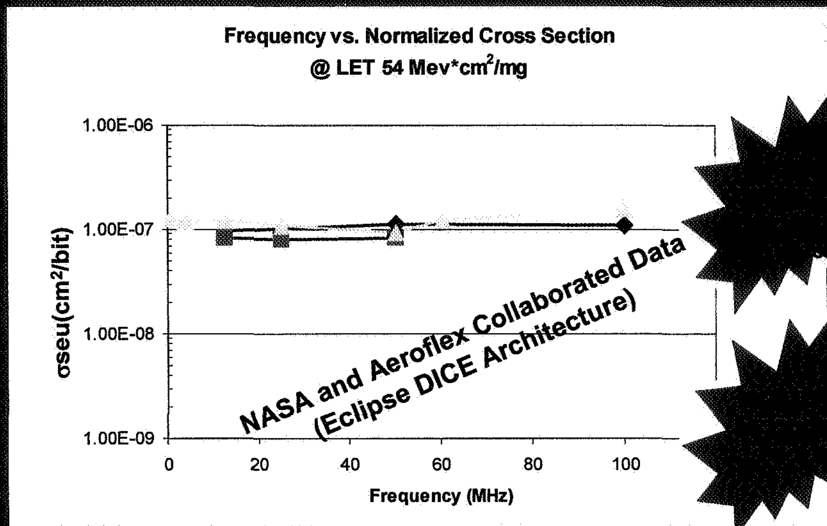
However…



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Comparision of FPGA Radiation Test Data (Dynamic Shift Register Tests Only)

	Actel	Aeroflex	Xilinx
Mitigation	TMR: embedded in device	DICE: embedded in device	Scrubbing: (overwriting Configuration Memory) Can not test without
Frequency	150 MHz	120 MHz	50 MHz
Frequency Dependent	Yes	No	?
Data Dependant	Yes	Yes	?
Lowest Cross Sections	✔		
Stay configured	Yes	Yes	No
SEFI	No	No	Yes
Speed Degradation	No	Yes – Too much exposure to high LET	No

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Data Analysis Conclusion

- We are aware of possible faults within circuitry
- When analyzing data, the proper precautions must be taken and the correct questions must be asked?

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Summary

- FPGAs have proven to be cost effective solutions to large, complex systems
- Configuration and logic structures vary among manufacturers
- When considering potential SEUs and deciding which device is best suited for a project, special attention must be taken concerning
  - Configuration Hardness
  - Logic Level Hardness
  - Ease of system level implementation
  - Function necessities (speed, data manipulation, ...)
  - Mitigation schemes (if necessary

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Summary (Continued...)

- Radiation Testing is necessary to characterize device level SEU data.
- Care must be taken to implement appropriate tests in order to push the DUT to its limits
  - Speed
  - Reliable data supply and capture
  - Realistic DUT design implementation
  - Simplistic structures – avoid fault masking
- While analyzing data the proper questions should be asked to ensure the data efficiently characterizes the device.

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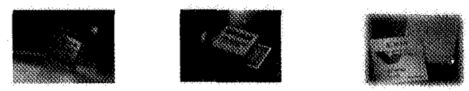
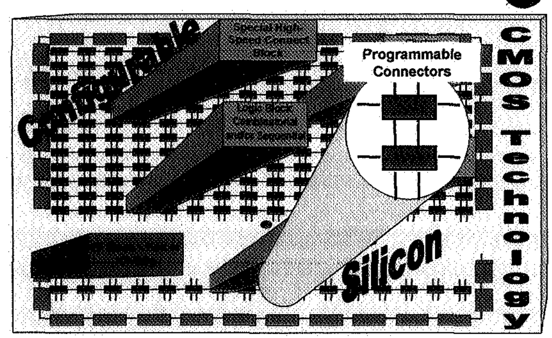
The IGS program was developed in response to an August [redacted] incident when North Korea [redacted] a missile that overflew [redacted] ritory and landed in [redacted] Two more satellites [redacted] join the first pair in [redacted] vember 2003, but [redacted] lites were destroyed [redacted] H-2A rocket carrying [redacted] failed.

Field Programmable Gate Arrays (FPGA)



General FPGA Architecture



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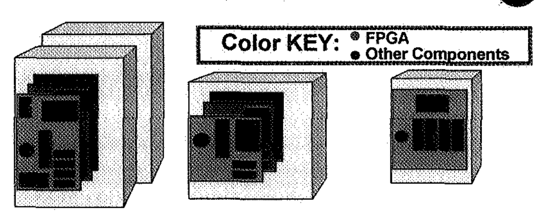

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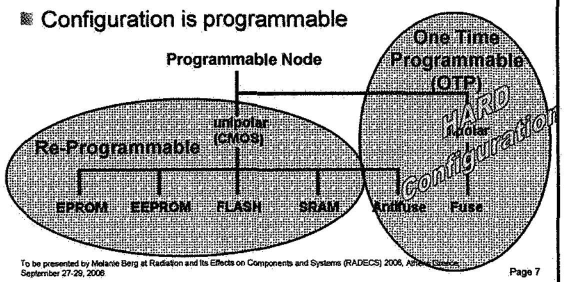
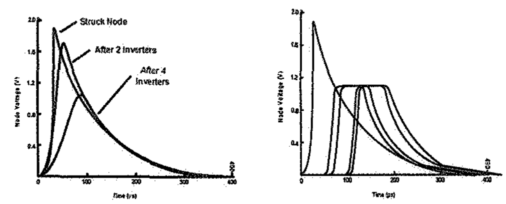


Transient Generation and Propagation



Add something about set capture in dff

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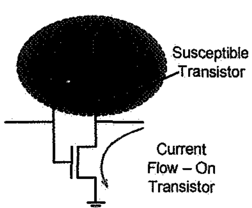
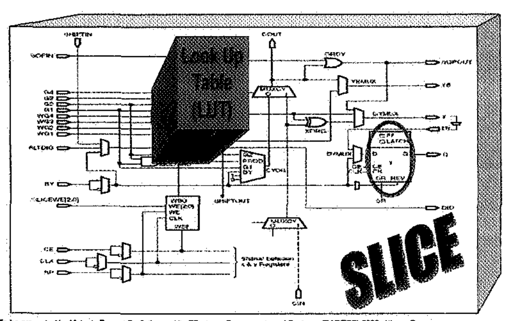
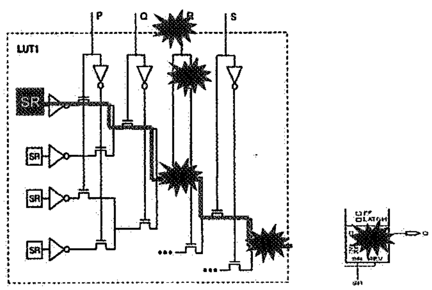


Example 1: Xilinx and the Complexity of a Configuration Logic Block (CLB)



Example: Susceptibility in a Xilinx 4-Input Look Up Table (LUT)



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- Test for:
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  - Single Event Functional Interrupts (SEFI)
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DUT Radiation Test Strategies

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  - Types of logic cells (check device technology library)
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Common DUT Characterization Test Structures

- Shift Register Strings (sequential logic)
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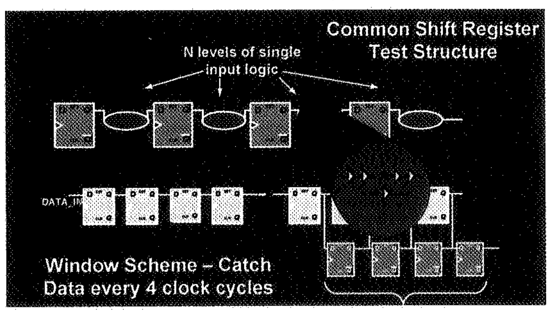
Testing Sequential and Combinatorial logic



Tester Radiation Test Strategies

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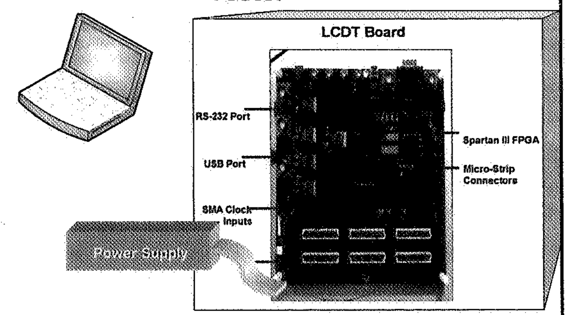
- Tester to DUT Interface Limitations
  - Number of I/O
  - Simultaneously Switching Outputs (SSO)
  - Interface connector speed

NASA GSFC Low Cost Digital Tester



Analyzing Test Data – Asking the Right Questions

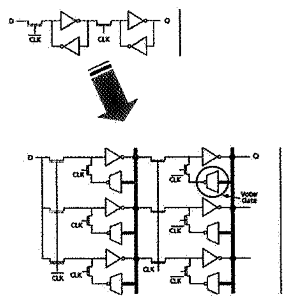
- Does the device stay configured?
- Is the DUT schematic supplied?
- Is the DUT implementation a reliable design?
  - Synchronous design techniques
  - "Single Integrity" solution applied
- How reliable is the supplied inputs and data capture scheme of the tester?
- What are the maximum and minimum frequencies supplied to the DUT during test and how do they relate to the timing specifications of the device?
- What are the data rates? (May be difficult to determine for complex designs)
- Are there SEFIs
- Is there speed degradation?

Data Analysis Example

- Actel Corporation and NASA-GSFC collaborated in supplying SEU RTAX-S device specific data
- Data was supplied at 2MHz testing frequency
- Simple shift register test structures were implemented
- **Question: Was the supplied data an Efficient characterization of the devices?**

Actel Logic Blocks: Sequential and Combinatorial

- RCELL (Sequential):
  - Triple Mode Redundant (TMR) Mitigation
  - Inputs are shared (single points of failure)
  - contains more logic (not shown)
    - 2 MUXs one for logic and one for clocking)
    - Adds more sources of failure
- CCELL (Combinatorial):
  - Logic Block is generally a MUX structure
  - Addition of block should increase error cross section as frequency increases



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Actel Expectations: SET Frequency Response

- In general …Combinatorial…..
- RCELL contains some
- CCELL should make a considerable contribution due to frequ dep

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Data Analysis Example (Continued)

- Another effort between Actel and NASA-GSFC was undertaken
- Clock Rates were supplied to the DUT from 15MHz to 150MHz
- DUT Input Data:
  - Alternating data was supplied at half the clock rate
  - Static "0"
  - Static "1"
- Several Designs were implemented to analyze the potential increased susceptibility to transients when utilizing C-CELLS
- Synchronous Design Approach was implemented in the DUT and in the tester.

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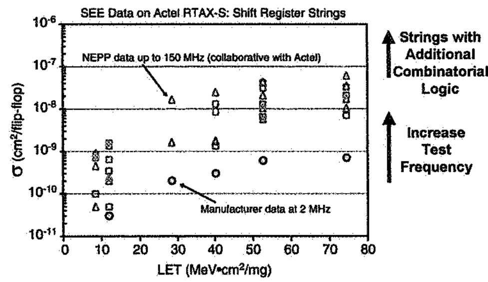
RTAX-S Data: Earlier and Current Test Data



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Survey – Why Was the Original 2MHz Data Acceptable?

- Asked Engineers and Physicists.
- Here's the Best of:

Engineers:

- Told Frequency dependency does not exist
- Was not aware of transients and their effects in circuitry

Physicists:

- Based on the new 150MHz, the original assumption that the data is scalable holds true – (2Mhz to 150Mhz testing should result in about 2 orders of magnitude between data sets

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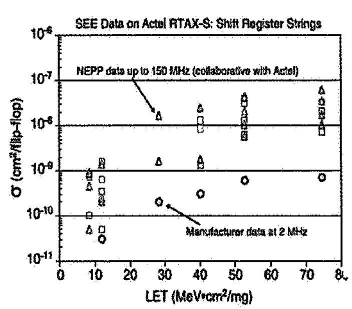
2 Orders of Magnitude is True in this Case



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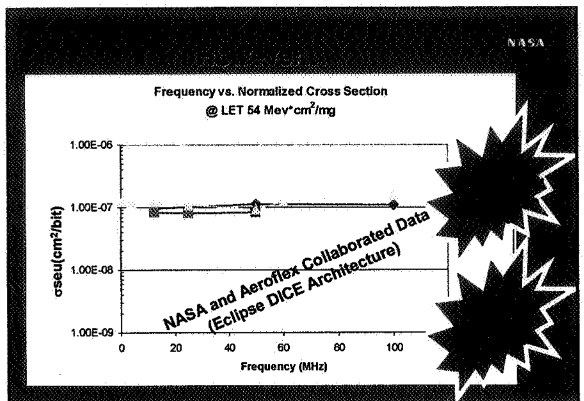

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Comparision of FPGA Radiation Test Data (Dynamic Shift Register Tests Only)

	Actel	Aeroflex	Xilinx
Mitigation	TMR: embedded in device	DICE: embedded in device	Scrubbing: (overwriting Configuration Memory) Can not test without
Frequency	150 MHz.	120 MHz	50 MHz
Frequency Dependent	Yes	No	?
Data Dependant	Yes	Yes	?
Lowest Cross Sections	✓		
Stay configured	Yes	Yes	No
SEFI	No	No	Yes
Speed Degradation	No	Yes – Too much exposure to high LET	No

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Data Analysis Conclusion

- We are aware of possible faults within circuitry
- When analyzing data, the proper precautions must be taken and the correct questions must be asked?

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Summary

- FPGAs have proven to be cost effective solutions to large, complex systems
- Configuration and logic structures vary among manufacturers
- When considering potential SEUs and deciding which device is best suited for a project, special attention must be taken concerning
  - Configuration Hardness
  - Logic Level Hardness
  - Ease of system level implementation
  - Function necessities (speed, data manipulation, ...)
  - Mitigation schemes (if necessary

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Summary (Continued...)

- Radiation Testing is necessary to characterize device level SEU data.
- Care must be taken to implement appropriate tests in order to push the DUT to its limits
  - Speed
  - Reliable data supply and capture
  - Realistic DUT design implementation
  - Simplistic structures – avoid fault masking
- While analyzing data the proper questions should be asked to ensure the data efficiently characterizes the device.

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