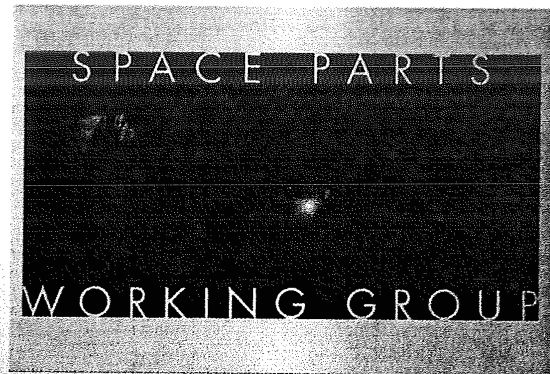

Kenneth A. LaBel, Michael J. Sampson

NASA/GSFC

THE AEROSPACE CORPORATION

To be presented by Kenneth A. LaBel and Mike Sampson at the Space Parts Working Group (SPWG) meeting, Torrance, CA, May 1-2, 2007. 1

The NASA Electronic Parts and Packaging (NEPP) Program – *Insertion of New Electronics Technologies*

Kenneth A. LaBel, Michael J. Sampson
Co- Managers, NEPP Program
NASA/GSFC
ken.label@nasa.gov michael.j.sampson@nasa,gov
301-286-9936
http://nepp.nasa.gov

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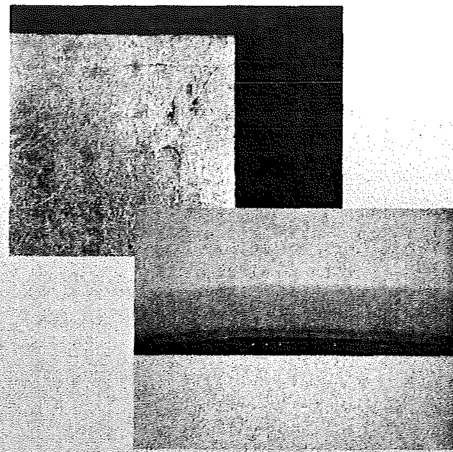
Outline of Presentation

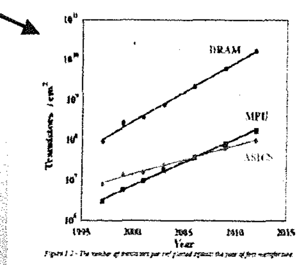
- A Changing Electronics World
- Cost of Doing Business
- Sample Shortcomings
  - Radiation Test Methods
- A Poster-child for New Technologies: Field Programmable Gate Arrays (FPGAs)
  - NEPP Efforts in FPGAs
- New Technology Insertion Meeting
  - Review
  - Directions



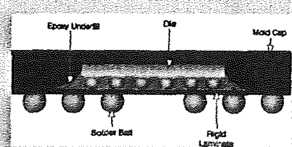
Two examples of deprocessing yield failures
-Cracks (top) and Waffling (bottom)
-Photos courtesy of Radiation Assured Devices

CMOS Electronics Technology Trends

- Scaling trends (smaller feature size) resulting in:
  - Increased gate/cell density per unit area (as well as power and thermal densities)
  - Lower supply and logic voltages ($\leq$1V)
    - Reduced electrical margins in a single IC
  - Changes in materials
    - Use of anti-fuse structures, phase-change materials, alternative K dielectrics, Cu interconnects (previous – Al), insulating substrates, ultra-thin oxides, etc...
    - New material leading to unknowns in radiation response and physics of failure



- Increased device complexity
  - More functions per chip: >1 billion gates in a single device
  - Increased number of levels of metal
  - Heterogeneous integration
- Increased operating speeds to >> GHz (CMOS, SiGe, InP, ABCS)
- Increased package complexity
  - Use of flip-chip, area array packages, etc
- Increased importance of application specific usage to reliability/radiation performance



The Changing World of Radiation Testing of Memories -

Comparing SEE Testing of Commercial Memories – 1996 to 2006

- Device under test (DUTs): Commercial Memory
  - For use in solid state recorder (SSR) applications
- 1996
  - SRAM memory
    - 1 um feature size
    - 4 Mbits per device
    - <50 MHz bus speed
    - Ceramic packaged DIP or LCC or QFP
- 2006
  - DUT: DDR2 SDRAM
    - 90 nm feature size
    - 1 Gbit per device
    - >500 MHz bus speed
    - Plastic FcBGA or TSOP
    - Hidden registers and modes
    - Built-in microcontroller

- Sample Issues for SEE Testing
  - Size of memory
    - Drives complexity on tester side for amount of storage, real time processing, and length of test runs
  - Speed
    - Difficult to test at high-speeds reliably
      - Need low-noise and high-speed test fixture
    - Classic bit flips (memory cell) extended to include transient propagation (used to be too slow a device to respond)
    - Thermal and mechanical issues (testing in air/vacuum)
  - Packaging
    - Modern devices present problems for reliable test board fixture, die access (heavy ion tests) requiring expensive facility usage or device repackaging/thinning
    - Difficulty in high-temp testing (worst-case)
  - Hidden registers and modes
    - Functional interrupts driving "anomalous data"
      - Not just errors to memory cells!
  - Microcontroller
    - Not just a memory

Commercial memory testing is a lot more complex than in the old days!

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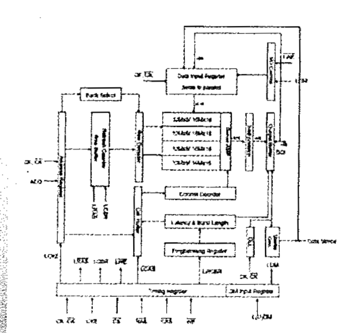
Can we test anything completely?



Commercial 1 Gb SDRAM
68 operating modes
operates to >500 MHz
Vdd 1.8V external, 1.25V internal

Sample Single Event Effect Test Matrix

full generic testing

Amount	*Item*
3	Number of Samples
68	Modes of Operation
4	Test Patterns
3	Frequencies of Operation
3	Power Supply Voltages
3	Ions
3	Hours per Ion per Test Matrix Point

66096	**Hours**
2754	**Days**
7.54	**Years**

and this didn't include temperature variations!!!

Test planning requires much more thought in the modern age as does understanding of data collected (be wary of databases). Only so much can be done in a 12 hour beam run – application-oriented

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Even Application-Specific Tests are Costly!

1996 SEE Test of a 4M SRAM

Description	Man-weeks or units	Cost in $	Total	Note
Heavy Ion at BNL SEUTF				
Test plan	0.20	$4,000.00	$800.00	Includes eng, rad, other to define what needs to go into test set with project.
Device procurements	10.00	$50.00	$500.00	
Misc parts	1.00	$250.00	$250.00	Sockets, connectors, etc...
Device delidding	0.05	$3,500.00	$175.00	
Test board design - electrical and layout	0.40	$4,000.00	$1,600.00	
Board fab and population	1.00	$3,500.00	$3,500.00	In-house board build
Board/tester debug	0.50	$4,000.00	$2,000.00	
Rad expert (test oversight and plan)	0.40	$5,000.00	$2,000.00	
Heavy ion test performance - contractor	2.00	$1,500.00	$3,000.00	
BNL Beam	6.00	$700.00	$4,200.00	Simple data: bit flips, latchup
Data analysis	1.00	$3,500.00	$3,500.00	
Test report (eng, rad expert, rad lead)	0.50	$4,000.00	$2,000.00	
		Total:	$23,525.00	

2006 SEE Test of SDRAM

Description	Man-weeks or units	Cost in $	Total	Note
Heavy Ion at TAMU				
Test plan	1.00	$4,000.00	$4,000.00	Includes eng, rad, other to define what needs to go into test set with project.
Device procurements	10.00	$75.00	$750.00	
Misc parts	1.00	$1,000.00	$1,000.00	Higher speed drives cost
Device thinning and package processing	10.00	$500.00	$5,000.00	Assumes FBGA package; if this does not work, more expensive test facility like NSCL needed: >$100K delta
Daughterboard Board design - electrical	0.80	$4,000.00	$3,200.00	
Daughterboard Board design - PCB	0.80	$3,500.00	$2,800.00	
Test Boards	10.00	$500.00	$5,000.00	
Board population	0.40	$3,500.00	$1,400.00	
Board/tester debug	0.50	$4,000.00	$2,000.00	
Tester VHDL development	4.00	$4,000.00	$16,000.00	
Technician	1.00	$3,500.00	$3,500.00	
Rad expert (test oversight and plan)	0.60	$5,000.00	$3,000.00	
Heavy ion test performance - contractor	3.00	$2,000.00	$6,000.00	
TAMU	16.00	$750.00	$12,000.00	2X time required: more data, more error types, more complex results; partial test
Data analysis	3.00	$3,500.00	$10,500.00	
Test report (eng, rad expert, rad lead)	1.00	$4,000.00	$4,000.00	
		Total in $	$80,150.00	

1996 vs 2006 a >3X Cost Delta

Other test costs and schedules (radiation and reliability) have increased commensurately! Quote here is optimistic, can be 3 or 4X more.

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Hypothetical New Technology Part Qualification Cost

Item	*Cost*	*Note*
Parts Procurement (500-1000 devices for testing only)	$25-1000K	Individual device costs can run from cents to tens of thousands
Standard Qualification Tests	$300K	
Radiation Tests and Modeling	$400K	Assumes total dose and single event (heavy ion) only
Failure Modes Analysis	$300K	Out-of-the-box look at the "hows and whats" for non-standard research required for qualification
Additional Tests, Modeling, and Analysis based on Failure Modes	$500K	
Total cost for one device type	$1.5-3M	Not all new technologies will meet standard qualification levels: technology limitations document

Assumption: it takes 12-24 months to develop sufficient data for technology confidence

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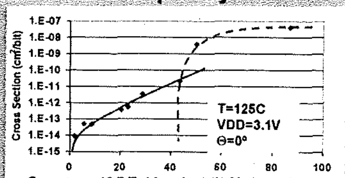
Where we are –

Radiation test methods and what has changed in the world

- Existing test methods
  - SEE
    - JEDEC JSD 57
    - ASTM, F1192-00
  - TID
    - MIL-STD-883B, Test Method 1019.7
    - ASTM, F1892-06
- All had prime development in the mid-90s with some updates since, however, many new issues have been discovered that may not be covered adequately



Courtesy ISDE, Vanderbilt University

- Examples: Recent SEE Phenomena
  - Angular effects in SOI technologies
  - Role of single event transients (SETs) and commensurate speed-related issues in both analog and digital circuits
  - Ion penetration and range issues in power and packaged components
  - Approaches to die access
  - Impact of application and reconfigurable approaches to SEE performance
  - Role of nuclear reactions from heavy ion particle interactions
  - Role of charge-sharing

NEPP and FPGAs- A Sampling of Challenges

Can we "qualify" without breaking the bank?

New Connectors
-higher-speed, lower noise
-serial/parallel

New Silicon
-90nm CMOS
-new materials

New Board Material
-thermal coefficients
-material interfaces

New Architectures
-new interconnects
-new power distribution
-new frequencies

New Workmanship
-inspection, lead free
-stacking, double-sided
-signal integrity

New Design Flows/Tools
-programming algorithms, application
-design rules, tools, simulation, layout
-hard/soft IP instantiation

New Package
-Inspection
-Lead free

Approaching FPGAs as a More Than a "Part" for Reliability

NEPP FPGA Task

Device Physics	Hardware	Software	Qualification
Understand possible failure modes	Develop platforms capable of adequately testing FPGAs	Develop designs that are custom tailored for specific failure modes	Develop an analysis methodology that correctly integrates results w/ new & current requirements
Do device level simulations to tie failures to operation	Leverage off vendor demo & engineering PCBs	Design test vectors that produce/induce failures	Provide de-rating & screening methodologies to ensure margin & success

NEPP POC for this effort: Doug Sheldon, JPL

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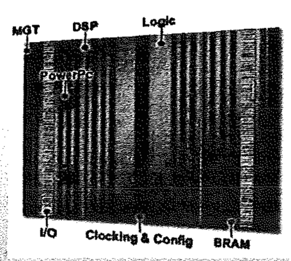
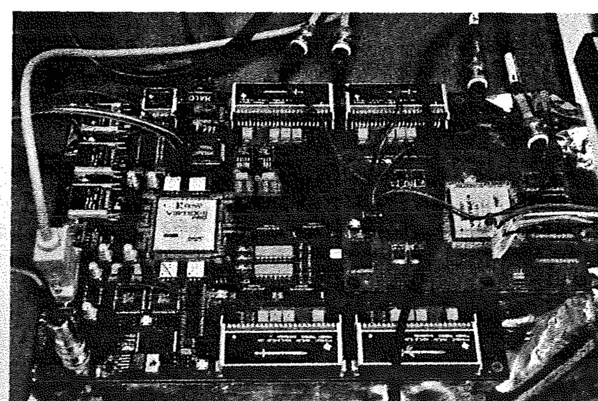
FPGAs Beget Novel Radiation Test Setups



Xilinx Virtex-IV Architecture



High-speed digital test motherboard w/Xilinx Virtex-II Pro FPGA as DUT controller and DUT daughtercard w/Xilinx Virtex-IV FX60

NEPP POC for FPGA Test Techniques:
Melanie Berg, MEI/GSFC
Gary Swift, JPL

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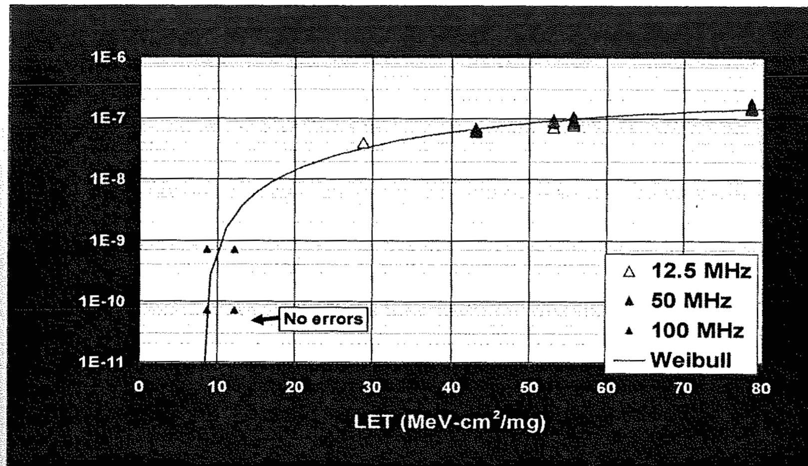
Understanding the Complex Radiation Data –

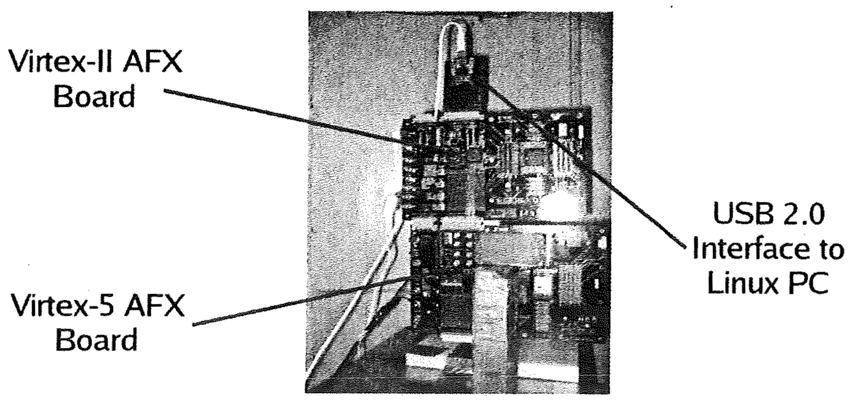
Aeroflex FPGA showing no Single Event Transient (SET) (operating frequency) sensitivity



But was the test design inside the device adequate to see SETs?

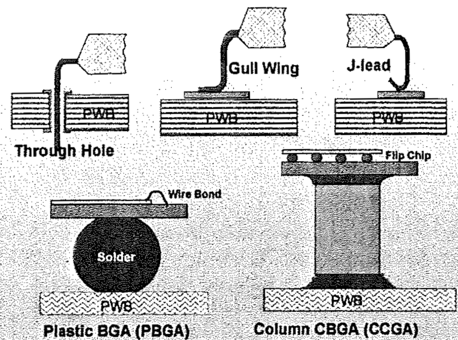
NEPP POC: Melanie Berg, MEI/GSFC

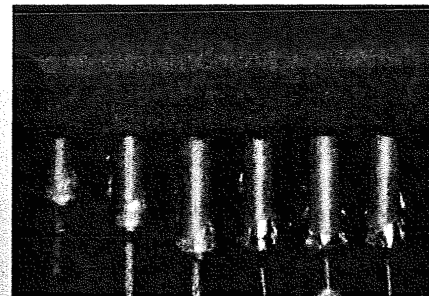
NEPP Collaborates between NASA Centers, Other Agencies, Industry, and University on FPGA



LANL Virtex-5 SEE Test Fixture: A Collaborative Test with NEPP!

Tracking Packaging Complexity and Reliability for FPGAs

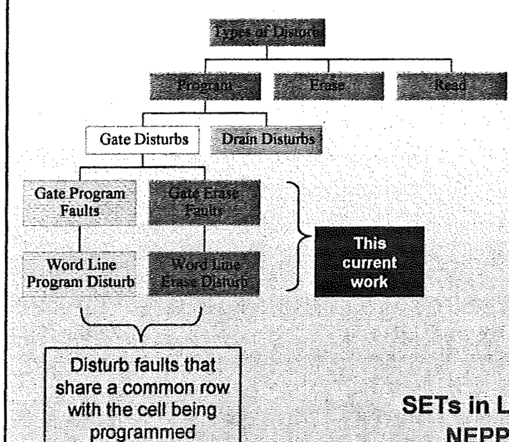


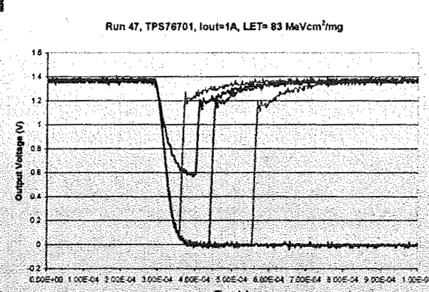


CCGA Package~1100 I/O Pins
245 Thermal Cycles (-55/+100 C) –
No Failures

NEPP POC for this effort: Reza Ghaffarian, JPL

Devices Supporting the FPGA Need to be Considered





SETs in Low-Voltage Power Conversion Devices
NEPP POC: Christian Poivey, MEI/GSFC

Gate Disturb Effects in FLASH NVMs
NEPP POC: Doug Sheldon, JPL

Summary of the New Electronic Technologies and Insertion into Flight Programs Workshop

- Workshop logistics
  - Held at NASA/GSFC on Jan 31 – Feb 2
  - Over 100 attendees from NASA, DoD, DOE, Industry, and University
    - No international participation due to government installation limitations
- Over 30 presentations and one panel session
  - Two days on general new electronics technology
  - One day with an FPGA focus
  - Expertise ranging from systems to packaging to parts to radiation and everything in-between
  - >80% or presentation are now available at ***http://nepp.nasa.gov***
- Goals of the workshop
  - 1. The Definition of New Technology Needs to Identify ALL Major Risks Without Creating an Unsupportable Burden and be Spaceflight Oriented
  - 2. A Path to a Risk-Acceptable Technology Insertion Methodology for Spaceflight

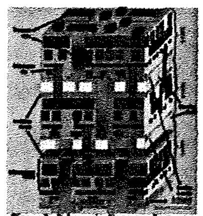


Figure 3. Schematic diagram of a prototypical 3-D integrated circuit with a high density of vertical interconnects between layers and carefully placed thermal vias.

The growing convergence of part, package,and workmanship issues

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Challenge to the panel - So What Now?

- Do we
  - *Put our heads in the sand and hide?*
  - *Run screaming and try working in another field?*
  - *Accept unknown risk?*
- OR do we
  - ***Work together to develop a way forward?***
  - ***Critically look at "qualification" versus risk reduction/acceptance?***
  - ***Determine how to work in an interdisciplinary manner?***
  - ***Develop a group/sub-groups to recommend approaches?***
  - ***Develop a white paper on how to get our arms around this growing challenge?***
  - *???*

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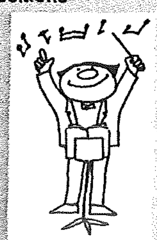
Highlights of Panel Notes and Comments

- Common recognition that we need to collaborate to move forward
  - Cross-organizational and cross-industry
- Need to define terms clearly
  - New, Qualification, Technology, Heritage, Reliabiltiy
    - Characterization vs. qualification
  - "Out of environment" usage
- Agreed Insertion Approach: form "consortia"
  - Government with industry review
  - Bandleader needed to "conduct" facilitate all the players for a 360 degree view
    - Systems engineering approach critical
  - Regular communication of progress required
- Rule/criticality based approach
  - Allows tailoring and application-specific review
  - Risk analysis required based on probability of occurrence
- Next step: White Paper
  - Objective: Organizational buy-in

Summary and Comments

- Suggested NEPP Augmentation Areas
  - Sample technical effort shortfalls were highlighted in FY07 plans
    - Example: Entire NEPP planned FY07 budget could be used for FPGA efforts!
  - New training modules are required for new technology insertion
    - More than just a parts, packaging, and radiation issue
    - Currently collaborating with CNES, ESA and others on radiation training class (SERESSA)
  - Increased university presence
    - Shortfall of qualified parts, packaging, and radiation specialists
      - Example: Difficulty in finding US citizens for radiation positions
    - Scholarships, post-doc opportunities, etc needed
- New Technology: The Direction Forward
  - Identify the players
  - Need to find a bandleader and get started
  - Develop executive summary
  - Increase education of these issues to the community



Any volunteers?