Semi-Automated Diagnosis, Repair, and Rework of Spacecraft Electronics

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NASA's Constellation Program for Exploration of the Moon and Mars places human crews in extreme isolation in resource scarce environments. Near Earth, the discontinuation of Space Shuttle flights after 2010 will alter the up- and down-mass capacity for the International Space Station (ISS). NASA is considering new options for logistics support strategies for future missions. Aerospace systems are often composed of replaceable modular blocks that minimize the need for complex service operations in the field. Such a strategy however, implies a robust and responsive logistics infrastructure with relatively low transportation costs. The modular Orbital Replacement Units (ORU) used for ISS requires relatively large blocks of replacement hardware even though the actual failed component may really be three orders of magnitude smaller.

The ability to perform in-situ repair of electronics circuits at the component level can dramatically reduce the scale of spares and related logistics cost. This ability also reduces mission risk, increases crew independence and improves the overall "supportability" of the program. The Component-Level Electronics Assembly Repair (CLEAR) task under the NASA Supportability program was established to demonstrate the practicality of repair by first investigating widely used soldering "materials and processes" (M&P) performed by modest manual means. The work will result in program guidelines for performing manual repairs along with design guidance for circuit reparability.

The next phase of CLEAR recognizes that manual repair has its limitations and some highly integrated devices are extremely difficult to handle and demand semi-automated equipment. Further, electronics repairs require a broad range of diagnostic capability to isolate the faulty components. Finally repairs must pass functional tests to determine that the repairs are successful and the circuit can be returned to service. To prevent equipment demands from exceeding spacecraft volume capacity and skill demands from exceeding crew time and training limits, the CLEAR project is examining options provided by non-real time tele-operations, robotics, and a new generation of diagnostic equipment. This paper outlines a strategy to create an effective repair environment where, with the support of ground based engineers, crewmembers can diagnose, repair and test flight electronics in-situ. This paper also discusses the implications of successful tele-robotic repairs when expanded to rework and reconfiguration of used flight assets for building Constellation infrastructure elements.

I. Introduction

NASA's plans for long duration missions to the Moon and, especially, to Mars require a much greater degree of self sufficiency on the part of the crew than ever before. Such missions will have greatly reduced logistic support from Earth, compared to International Space Station (ISS) operations. Returning to Earth in the event of an emergency may not be an option either, as a lunar return flight could require two to three days, and a Martian return flight will require much longer.

One area of mission support that NASA must plan for is electronic repairs. Despite the rigorous testing required by NASA, electronics faults have already occurred in both Space Shuttle and ISS operations, leading to the use of backup systems or loss of capability to some degree[1,2]. While the electronics and other systems used in a long duration space mission will undergo rigorous testing, the crew of such missions will most likely encounter an

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electronics failure at some point in the mission. With the design of the Crew Exploration Vehicle (CEV) already beginning and likely influencing the design of future spacecraft and hardware, it is not too early for NASA to begin exploring and designing techniques and tools for crew members conducting electronics repair during long duration space mission. These considerations include system design (for accessibility, parts type and sizes, and board complexity), repair infrastructure (including diagnostic capabilities, tools, and other needed equipment), and logistics constraints. The decisions on how to approach each of these considerations depends on the overall repair strategy chosen.

The historical approach to electronics repair on manned spaceflight missions (particularly those aboard the International Space Station, or ISS) has been to replace modular subassemblies called Orbital Replacement Units (ORU's). The astronaut simply replaces the malfunctioning ORU with a spare, and then returns the faulty ORU to Earth, where it is diagnosed and repaired, then returned to a pool of spares awaiting re-use in space. This approach allows for simplicity in the diagnosis of the problem, as the fault only has to be isolated to a given ORU, rather than determining the fault down to the component level. Crew training and experience in performing repairs are minimized. Also there is a high degree of confidence in the repair, as the ORU can be tested extensively on the ground prior to being re-launched to the ISS.

Conversely, this approach carries with it a severe penalty in terms of the logistics support required (and overall cost to the program). Conceptually, it is easy to imagine the penalty in mass and volume that is levied when an entire ORU (which may weigh ~25 lbs or more on Earth) is launched to remedy a failure of a single, small component such as a resistor, transistor, or other electrical component. While this approach is expensive, it may be acceptable for low Earth orbit (LEO) missions if they are re-supplied regularly since large quantities of spares would not need to be stored on orbit.

Alternatives to the ORU are lower-level repairs which can include shop-replaceable units (SRU) such as circuit board-level swap-outs and / or a component-level repair strategy. This could serve to greatly reduce the planned-spare ORU requirements, while providing a capability to handle unforeseen repair contingencies. The need to handle such unexpected events has been illustrated by several events in NASA flight history. The successful conclusion of the Apollo 13 mission, after an explosion severely damaged the service module, highlights the benefits of having the capability to implement on-the-spot repairs. The consequence of failing to allow for off-nominal repairs was demonstrated in the tragic loss of the shuttle Columbia; even if the crew had been aware of the problems with the leading edge tiles, they were not equipped to make repairs in-flight. Since that incident, NASA has made considerable efforts to allow for contingency repairs of problems of that nature[3].

The Component-Level Electronics-Assembly Repair (CLEAR) project under the NASA Supportability program was established to develop and demonstrate the technology necessary to allow crew-member to effectively perform electronic repair down to the component level. CLEAR involves collaborative efforts between NASA's Glenn Research Center, Langley Research Center, Johnson Space Center, the National Center for Space Exploration Research, and the U.S. Navy. The overall processes involved with repair which are the objectives of the CLEAR task are composed of four primary elements:

1. Capability to diagnose an electronics assembly and identify the faulty component(s) with equipment that fits within the mass-volume and power constraints of spacecraft.
2. Capability to repair electronics down to the component-level on-orbit with processes and materials that are safe and compatible with the space environment which allows the crew to make the necessary repair.
3. Capability to evaluate and determine that the repaired circuit is safe to return to service.
4. Capability to augment the flight crew with knowledge and skills to diagnose faults and perform repairs without expanding crew size.

This multi-faceted program utilizes a cross-disciplinary approach to examine pre- and post-repair diagnostics and functional test; material and process for repair such as component soldering, conformal coatings removal and replacement; and electronics design for supportability. These areas are investigated by a combination of trade studies, analysis, ground based testing, reduced gravity aircraft testing, and actual spaceflight testing aboard the ISS in multiple experiments. This paper provides an update to this task since previously reported at this meeting in the previous year.[4-5]

II. CLEAR Task Overview

A. Manual Electronics Repair

All repair scenarios for the Constellation Program (CxP) will include some manual repair capability in which the crew can make electronic repairs. Currently, the ISS has a soldering kit aboard which offers a very basic capability and is a logical baseline for future capabilities. The soldering kit and tools available on-orbit are capable of basic

repairs (e.g. wire splicing and some limited component-level repair). However, component-level repair has not been actually demonstrated using this equipment aboard ISS. The experience of the US Space Program with repairs is limited to a very few cases (e.g. ARCTIC-1 repair discussed below) and some basic experiments[6]. Before mission planners can expect to have a repair capability, it must be demonstrated in the field (i.e. to raise the technology readiness level, or TRL, to a level six[7]).

In a series of 2 flight experiments, the CLEAR project will demonstrate manual component-level repair using an augmented version of the soldering capability currently on ISS. The first experiment, called SoRGE, uses the soldering kit to investigate the basic materials and processes (M&P) involved with soldering in a microgravity environment using a through-hole configuration. The second experiment, called Component Repair Exp-1, intends to demonstrate all of the physical processes of end-to-end component-level repair of a circuit board. These experiments, which are discussed further below, utilize the Space-station Development Test Objective (SDTO) process to get aboard ISS (ref).

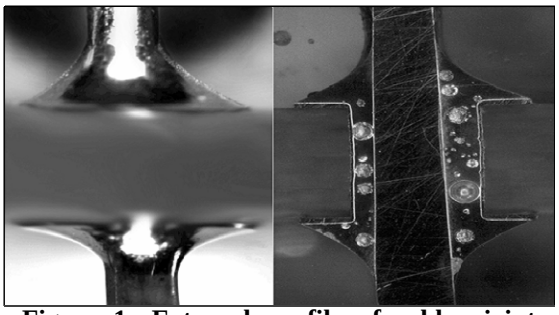

Figure 1: External profile of solder joint (left), and cross section of joint (right) showing internal voids.

1. Soldering in Reduced Gravity Experiment (SoRGE)

SoRGE is an experiment which is investigating the formation of solder joints in a microgravity environment (Figure 1). Results from earlier aircraft testing showed that void defects (bubbles /voids trapped within the solder) increased in joints formed in reduced gravity as those formed in normal gravity[8-12]. Joints were formed in various reduced-gravity environments including (nominally) Martian, Lunar, and zero gravity levels[*]. In these tests, the void fraction increased as gravity level was decreased. For joints formed in a nominally zero-gravity environment, the void fraction was 3-times higher than those joints formed in normal gravity. Changes in joint geometry were also observed, with the reduced-gravity joints being more symmetric.

The ISS experiment SoRGE is examining several techniques which may serve to mitigate the formation of voids in the solder joints. This experiment is comprised of a series of small circuit cards, with small electrical components (resistors) attached to the surface (Figure 2). The experiment has several kits, each of which is looking at various solder and flux combinations, to quantify and minimize the amount of void formation in solder joints. Also, this experiment will yield valuable information regarding the physical process of soldering in low-g with a crew-member who received only limited training.

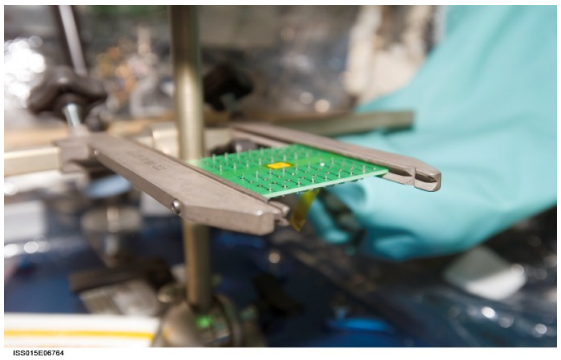

Figure 2: An image of the test card used during the SoRGE experiment.

This experiment was brought to the ISS by the Shuttle Atlantis during STS-115 and soldering was accomplished by Astronaut Sunita Williams (Figure 3) during February and May of 2007. Half of the available 12 test kits were completed and returned to Earth aboard STS-118 in August 2007. The samples were returned to GRC in October 2007 and are currently undergoing analysis. The planned analysis consists of a visual examination for solder process quality as well as non-destructive analysis to look at solder joint voiding. The results of this research will help specify the soldering process used in future in-space repairs.

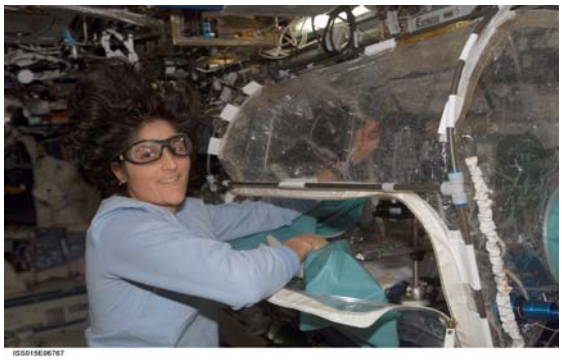

Figure 3: Astronaut Sunita Williams conducting the SoRGE experiment during Expedition 14 aboard the ISS.

[*] Brief periods (~25 seconds) of reduced-gravity are experienced aboard these aircraft as they fly parabolic trajectories which are calculated to provide the desired relative acceleration levels.

2. SDTO2: Component Repair Exp-1 (CRE-1)

CRE-1 will demonstrate the physical processes of an end-to-end manual electronics repair in a microgravity environment. The physical processes include:

- Conformal coating removal
- Component removal
- Board cleaning
- Soldering a new component in place
- Reapplying conformal coating

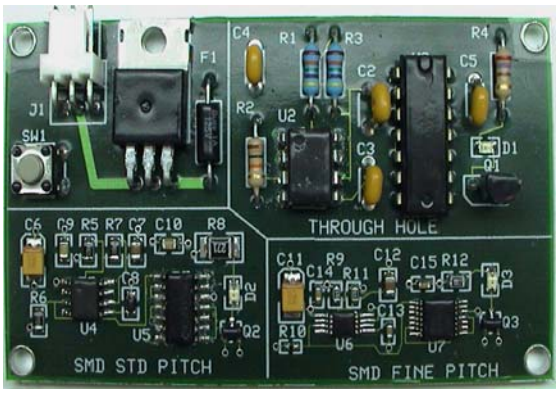

Figure 4: Image of CRE-1 circuit board

Crew members will work on functional circuit boards designed to mimic those already in use. These board designs use standard circuit components and component spacing. These standard circuit components include through-hole parts, standard-pitch surface mount devices (SMD), and fine pitch SMDs with typical component spacing (Figure 4). The circuit boards also have three thicknesses of silicone room-temperature vulcanizing (RTV) conformal coating: a primed, 4-mil coating; an unprimed 15-mil coating; and no coating, allowing for continued operation should the crew encounter difficulties removing conformal coating. The repairs will be conducted within the Maintenance Work Area (MWA) aboard the ISS (Figure 5). The experiment will utilize the soldering kit available aboard the ISS as well as an augment tool set provided by the CRE-1 experiment. The goal of the tests is to evaluate the feasibility of performing component level repair and evaluate processes so recommendations to procedures, tool selection, crew training, as well as board design may be made. CRE-1 is currently at Kennedy Space Center awaiting a manifest opportunity to fly to the ISS.

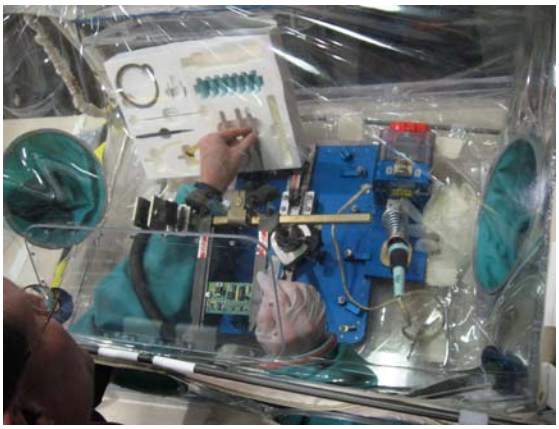

Figure 5: Testing of the CRE-1 experiment in the MWA mock-up at Johnson Space Center. Shown in the image are the auxiliary tools used to conduct manual repair of electronics.

3. Manual Repair Process Recommendation

The primary goal of the manual repair efforts is to develop a series of recommendations to the NASA CxP for processes, materials, tools, and training for crew members to perform manual electronics repairs during space missions. These recommendations will be built from the results of the on-orbit testing, ground based testing on the C-9 reduced gravity aircraft, and work in consultation with the U.S. Navy at the Naval Surface Warfare Center in Crane, IN. Additional work expected to begin in 2008 includes examination of possible conformal coating selection, both in manufacture and after a repair, that would help enable manual repair. It is anticipated that this recommendation will include future development areas needed to refine manual repair.

Analysis of Arctic Freezer Samples

Studying the results of electronics repairs actually performed on orbit will provide an insight into the actual, current capabilities and constraints of crew members performing these repairs. During Expedition-6, Astronaut Don Pettit attempted the repair of ARCTIC-1 (or the Arctic Freezer), a module used for the cold storage of experiment samples. This work included some aspects of electronics repair, including joining wires and connecting wires to component tabs (Figure 6), with the use of the soldering kit on the ISS. Nondestructive analysis and visual inspection of these joints, as well as, similar joints formed in normal gravity for comparison, is on-going and will aid in

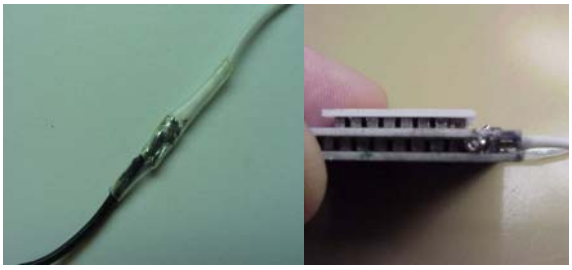

Figure 6: Typical solder joints examined from the repair of ARCTIC-1 freezer aboard the ISS.

evaluating the effectiveness of soldering in reduced gravity, especially in the mitigation of voids within solder joints.

C-9 Test Analysis

In February 2007, a series of solder tests were conducted on the C-9 reduced gravity aircraft which included the examination of various solder and flux combinations, most focusing on the use of no-clean or water-clean fluxes with eutectic solders. This work builds on previous aircraft tests[8-12], and will provide insight into general soldering and void mitigation techniques for reduced gravity operations. The analysis includes discriminating between samples based on the quality of the given in-flight performance (the aircraft parabola) as well as acceptance by a NASA flight qualified technician, based on NASA standards. Acceptable samples are nondestructively analyzed for void formation. Results from this analysis of a subset of these tests are presented in a complimentary paper at this conference[13]. These results will help develop criteria for selecting solder, flux, and techniques to be used for in-flight repair of electronics.

Crew Training Requirements (with U.S. Navy)

Crew training prior to a mission is vital for electronics repair. Crew members are presumed to have little or no prior experience in performing repairs, so training materials must prepare and reinforce the repair process. The team, working with a group at the Naval Surface Warfare Center in Crane, IN, responsible for preparing training materials for the U.S. Navy, will prepare and test crew training courses of 4, 8, and 16 hours, allowing NASA to tailor and choose a course suitable for electronics repairs. These materials are also planned to be available during flight as a refresher course and to prepare a crew member immediately prior to performing a repair. The team, together the U.S. Navy, will propose a tool set tailored to the level of crew training to allow crew members to effectively conduct the repairs they have been trained to perform.

B. Semi-Automated Repair

The previous section discussed hand or manually operated repairs used in the soldering and desoldering process. Manual repair will always provide an important repair capability, but it requires training and periodic practice to maintain proficiency. Manual repair also requires direct crew involvement throughout the repair process. A fully automated process such as in manufacturing requires special fixtures and equipment, along with a great deal of experimenting or system "tuning." For single unit repairs a mix of manual and automated operations is more practical and is most likely to achieve successful repairs within the spacecraft weight and volume constraints. Certain operations, such as wiping away process residues, are simple if performed manually but can be very difficult to accomplish by robotic means. Heating devices to narrow temperature bands and then quickly and precisely placing them demand automated operations. Semi-Automated repairs reduce the demand for high skill while increasing productivity.

Rework Stations (Figure 7) that melt or "reflow" solder with Hot Gas or Infrared heat evolved to handle complex devices. Such systems are semi-automated where manual operations involve alignment with optical aids but employ automated heating systems and mechanically guided placement. In this way, Semi-Automated rework stations extend repair capabilities to circuits not amenable to manual repair.

Figure 7: An ATCO AT-707 is typical of a commercial rework station capable of replacing high density integrated circuits. Photo from http://atco-us.com/.

Figure 8 is a qualitative representation of how semi-automated technology can extend a repair capability. The vertical axis of Figure 8 qualitative represents how increased PCB layering increases board thermal conductivity. The increased conductivity increases heat transfer away from the solder joint(s) and may exceed the manual soldering iron's capacity. More advanced manual techniques (more advanced soldering tools than available on ISS) may include custom tips and board heaters to preheat the entire board to temperatures just below the reflow solder temperature. However, the high heat loads and long heating cycles require to solder the conductively cooled circuit boards, common in spacecraft, are more likely to be successfully repaired by semi-automatic systems.

The horizontal axis of Figure 8 shows increasing complexity in device packaging and lead count. At the extreme right is the Ball Grid Array (BGA) where lead counts may exceed 1000 and are impossible to solder by hand. Large integrated circuits like BGAs require simultaneous solder or desolder of many pins or solder balls and are best handled by semi-

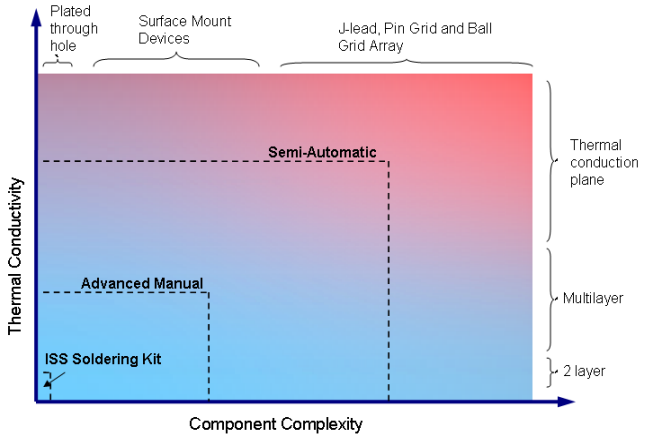

Figure 8: Graphic showing the increased repair capability offered by semi-automated repair technology.

automatic equipment to provide precise parameter control, such as, placement, coordinated motion, temperature ramp and soak profiles, and critical timing.

It is likely that the first operational need for repair capabilities is during long-duration outpost stays on the Moon and especially Mars. However, the ISS is a prime location to evaluate such technology and, because of the retirement of the space-shuttle in 2010, may benefit from a repair capability to help sustain systems with reduced logistical support. While the ISS and outposts share many similarities in terms of the environment, the prime difference is that there is significant gravitational force for the outpost whereas for ISS there is not. The semi-automated system is expected to employ or accommodate a variety of functions that include machine set-up, optical examination, process monitoring, a variety of mechanical repair operations (including soldering and de-soldering), handling and application of a variety of process fluids, and containment of solid debris and volatile products within the tight confines of a spacecraft or habitat. Before investing in specialized equipment, studies need to determine if the processes have any significant reduced gravity dependence, outgas, or other space environment sensitivity. The CLEAR task is in an early evaluation phase examining the general operation and capability of these stations, as well as the benefits and challenges for adapting them for use in space flight.

C. Diagnostics and Functional Test

While the physical repair of electronics in spacecraft and habitats is challenging, diagnosing faults down to the component level represent a bigger challenge. Furthermore, confidence of a successful repair must be accomplished via a functional test of the repaired board and/or subsystem. On the ground, NASA, the military, and industry all have practices, technicians, and equipment in place to perform diagnostics and repairs of electronics. Each group has adapted standard test equipment as well as customized equipment to perform the diagnostics particular to their requirements. None of these cases, though, have the volume, mass, power, and user experience level limitations imposed on them as for a long duration space mission.

Currently, ISS diagnostic and test equipment is limited to a portable Fluke Scope Meter®, a laptop logic analyzer and a limited output power supply and a special test set up to specifically test on-orbit multiplexer/de-multiplexer units. Such hardware is far from a complete diagnostic instrument set suited to test the array of systems including: electrical power, command & data handling, communications & tracking, guidance & navigation, and controls & display systems throughout spacecraft. Even if provided detailed information, it is beyond the most capable crews to fully understand diagnostic measurements of every spacecraft component. The next sections describe the strategy and technology that CLEAR is evaluating for diagnostics and test capability in future manned space missions.

Figure 9: A representative National Instruments PXI chassis populated with a variety of instruments from different manufacturers. Photo from http://www.pxisa.org/.

Diagnostics

Repairs of circuit board assembles requires isolating faults to the component level. There is no single technology solution but success lies in focusing on the fundamentals of measurements rather than stacks of instruments. The challenge is selecting equipment and/or developing hardware that can cover the majority of diagnostic needs (as well as functional test discussed below) within the allowable mass and volume constraints of a spacecraft or habitat. The PXI (PCI eXtensions for Instrumentation) based suite of instruments (Figure 9) may be one potential solution. The advantage of such devices is the space saved by combining many PXI-based instruments into one bus. The drawbacks include requirements for instruments to be

redesign into card format which is compatible with the bus architecture. Further, bus architecture often becomes obsolete. For example, the PXI architecture is currently being displaced by the new PXI Express.

Another approach would be to use Local Area Network (LAN) technology such as LXI (LAN Extension for Instrumentation). LXI instruments can be used in a coordinated suite of instruments or broken out as independent and portable instruments. High speed LAN based instruments are expected to resist obsolescence much longer. LXI instruments however, are not as compact as PXI. Recent industry trends indicate that a mixed system of LAN and Bus based instruments provide the best solution.

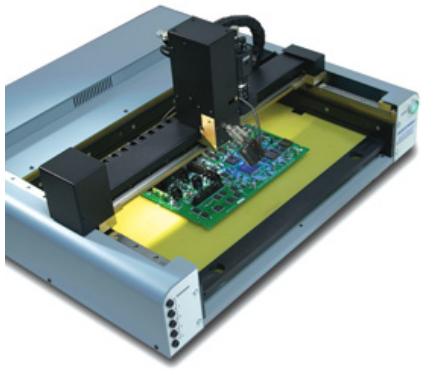

Figure 10: Huntron® ACCESS unit is an automated diagnostic system that employs circuit computer aided design (CAD) data and imaging to help guide the probing process. Photo courtesy of Huntron. Inc.

Diagnostics are often comprised of instruments that are used manually or programmed to automatically make measurements in a prescribed sequence. The instruments usually send stimulus signals and capture responses from the target circuit. For automated diagnosis, the same motion control capability used in repair can provide probing for diagnostics. One promising technology is the Analog Signal Analysis (ASA) technique used by the Huntron® ACCESS instrument to probe circuit nodes with a very low power signal that will not harm the circuit (Figure 10). This signal energizes single nets on the card to determine a characteristic waveform. A net is a common connection where multiple components are connected. This waveform is then compared with a known good board signature. If there is significant difference between the measured waveform and the known good waveform, one or more of the components attached to the net are defective. This approach reduces the number of components required to be replaced and minimizes the operator's skill requirements. However, ASA may not always isolate a fault to individual components, particularly, if they are not directly accessible. Complex Signature Analysis (CSA), being developed by CLEAR, is an alternative approach that relies on characterizing a circuit's self resonant and network resonant behaviors. CSA is expected to detect faulty devices that are inaccessible to ASA techniques. ASA and CSA both provide the ability to diagnose a circuit in a "power OFF" condition. Should ASA/CSA fail to isolate faults using a "known good board" technique, ASA/CSA can still capture measurements that could be further examined by knowledgeable ground based engineering. ASA/CSA operates on circuits in a "Power Off" condition which affords extra safety. However, it is often necessary to run tests on a circuit in a "Power On" condition to isolate functional problems such as software faults.

Functional Test Equipment

Functional testing is used to determine if a circuit is capable of performing its intended function before it is integrated into a system. It is often used to verify software functions that cannot be measured by fundamental diagnostic measurements. The actual functions of an ORU electronic circuit may be simple and repetitive. Most ORUs are part of a larger system and thus functionality may require interaction through multiple external interfaces. Functional test equipment often emulates the external system and operational conditions and includes additional "breakout" instrumentation to monitor interactions. Automatic Test Equipment (ATE) is employed when the number of channels and execution speed exceeds the capability of human operators. Typically, ATE systems are a combination of custom and off-the-shelf test equipment and software, with a software executive that governs the test process.

It is not uncommon for a single avionics box to require multiple racks of test equipment. In their terrestrial form, the weight and volume required for functional testers prohibits their use aboard spacecraft. However, functional test is an important part of any repair process and must be available. The ability to perform functional testing at the board level enables the generation of engineering data during the debug process. It also allows for the functional testing at the board level to minimize the risk of a circuit card damaging the system. Therefore, strategies for functional testing in spacecraft or habitat volumes require significant reduction of both mass and volume of terrestrial systems or newer technology. One such technology is offered by synthetic instruments.

Synthetic Instruments

Synthetic Instruments (SI) refers to an approach that exploits software and reconfigurable hardware to maximize the flexibility of test systems. Synthetic Instruments are implemented on generic hardware, typically, Field

Programmable Gate Arrays, (FPGAs). FPGAs are designed to provide a vast array of logic gates that can be configured to provide distinct data and control functions. Unlike software executed by microprocessors, the "Synthetic Instrument" programmed into the FPGA executes at extremely high speeds and with high levels of parallel processing. The FPGA can be reconfigured, on demand, as a completely new Synthetic Instrument. The latest generation of FPGAs can provide real-time signal processing which was once the domain of Digital Signal Processors. The main advantage of SI is that it allows us synthesize high performance instruments on an "as needed" basis.

The Department of Defense regards SI as a major advance in reducing (a) life cycle costs (b) time to develop and field new or upgraded test equipment, (c) test system logistics footprint, and (d) test systems physical footprint[14]. The strategy behind SI is to allocate any digitized functions to software. Innately analog functions, such as sensors, analog signal devices, and power sources are handled by modules that can be reconfigured electronically to provide wide operating ranges. In addition, to handle the vast variety of connector configurations, SI provides an upfront analog switching matrix that routes signals from a target test circuit to a selected analog instrument module. The CLEAR project is evaluating SI as part of a strategy to provide both diagnostic and functional test capability for a wide range of spacecraft electronics using only a small amount of physical hardware.

Both repair and diagnostics require significant skill and knowledge related to the circuit under test. Therefore, it is anticipated that the crewmember will require significant ground based support to debug issues. Furthermore, many of the process described above can be automatically controlled from the ground in a non-real time fashion. To keep the crew workload to a minimum, the semi-automated diagnostic and repair system should be amenable to tele-operations. Such operations also will allow data from the circuit under test to be available to ground personnel.

D. Tele-Operations: Linking the Crew to Knowledgeable and Skilled Support

In light of limitations on available technician-level skill and designer knowledge of the electronic systems, the key to success is to link the process to knowledgeable and skilled engineering staff though tele-operations. Other tele-robotic experiments focus on real-time control and real-time feed back while other robotic efforts focus on achieving total robot autonomy. Although crew autonomy is the desired goal, a likely strategy for a semi-automated diagnostic and rework station in spacecraft and habitats is to provide timely but not real-time interaction. The preferred mode is to avoid real-time "joystick" interaction with the hardware because the current infrastructure is prone to interruptions and signal delays.

For Lunar operations, the 4 second round trip transmission and system delays make real-time control awkward and even dangerous. The vast range of delay times for Mars makes real-time control impossible. Even the ISS has delays but also frequent "loss of signal" events which makes real-time control unreliable. Avoiding real-time interaction simplifies the communications and interaction and also provides an opportunity to "validate" commands prior to sending them to prevent costly and possible hazardous mistakes. Pre-scripted repair routines for anticipated needs will be developed. A potential solution to avoid the cost of a of support staff on standby, repair depots and manufacturers could support repairs on an "as needed" basis. The use of such a tele-operations capability is best captured by a Semi-Automated Diagnostic and Repair Operations scenario we describe below. This scenario is intended to illustrate how a diagnostic and repair tele-operation might proceed with a repair capability as shown in Figure 11.

Semi-Automated Diagnostic and Repair Operational Scenario

A vehicle health monitoring system reports a fault in a system ORU package. The faulty ORU is removed and replaced with a spare ORU which restores functionality to the system. Subsequently (as crew time permits and criticality requires), the faulty ORU is further diagnosed with a computer connected via an ORU test port. An internal Built-In-Tests (BIT) checks the diagnostic codes on all circuit boards. Ground support observes the diagnostics data via tele-operations. One circuit board fails to respond to BIT initiation. The subject board is removed from the ORU and interconnections were found to be good. Ground support asks the crew to move the board to the Semi-Automated Diagnostic and Repair Station and set up for further diagnostics and possible repair.

The board's failure to execute the BIT implies that the main processor is non-functional due to internal fault or failed supporting component. The ground support engineers examine high-resolution camera images down-linked from workstation but no visible damage is found. The circuit is equipped with a JTAG port and supports "boundary scan techniques[5]". The JTAG Boundary Scan Analyzer finds no problems at the I/O ports but reveals that several

[5] Boundary scan, also known as JTAG 1149, was developed by the Joint Test Action Group to allow board makers to check individual devices while isolating them from the external circuit[15].

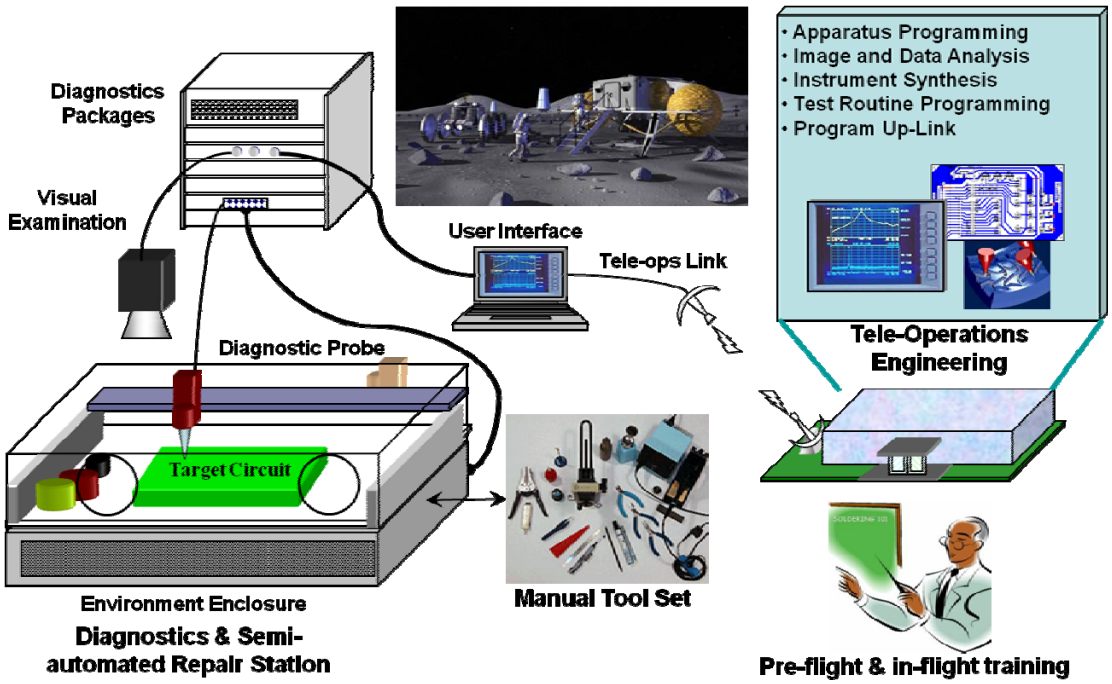

Figure 11. Diagnostic and Repair concept (including both manual and semi-automated processes) being evaluated by the CLEAR team.

registers are irreparably damaged, possibly due to radiation. Having isolated the component, the repair workstation is set up to remove and replace the device.

The ground crew determines that no prior repair routine exists so they go "offline" to create a repair program while the crewmember resumes other activity. Assisted with information from the vendor, the ground crew loads the circuit's Computer Aided Design (CAD) data into a Repair Process Modeling Tool that aids in programming robotic operations of the rework station. The circuit's registration points and exclusion zones are defined to prevent collisions with clamps and some taller board components. The Repair Process Modeling Tool defines motion paths, tool change points, including the component pick & place operations. Reflow heater position, heating profile are calculated using a reflow thermal simulation tool developed as part of the rework station. When the control code script is complete, it is run through a verification tool that simulates the process and shows a 3D animation of the process. Tool collisions discovered in the simulation are corrected and the code is determined to be error free.

On-orbit a "touch-off" of circuit registration points assures the machine motion is calibrated. The ground crew has determined that the conformal coating around the component should be removed manually because jumper wires interfered with mechanical methods. The workstation enclosure circulation filters capture any stray debris as the crewmember strips away the coating.

The control is then switched to automatic mode and the process is initiated. After the reflow heat cycle, a robotic pick & place tool removes the component. A quick manual wipe of the site removes any residue and a solder paste dispenser applies new solder. Another reflow cycle melts the paste while a component pre-heater prepares the new device. The robotic suction tools picks up and positions the new device and holds it until the last reflow heat cycle is complete.

An imaging camera scans the board for completeness and looks for debris. The tool is changed to an Analog Signature Analysis Probe and the preprogrammed probing sequence reveals that the board's signatures are normal. Subsequent JTAG boundary scan and register checks are normal. Power up BIT tests also return normal results. Finally, the ground team has come up with code to program the SI system available on orbit to do a function test on the card. The board is connected via a cable assembly and the instruments go through a functional checkout of the circuit board with normal results. The board is then re-integrated into the ORU and BIT tests indicate functionality. The final assembly is complete and any configuration information is noted. Since the original ORU was replaced with a spare, this unit now becomes the next serviceable spare until needed. The ground updates any lessons learned and refines the repair program. After further simulations, the repair script is "canned" as a ready-to-run routine for future use.

Impact on the Future of Constellation

Extrapolating a future capability based on Earth based practices is not enough. On Earth, the economy of mass markets, low cost labor, low cost transportation, and very high production rates results in circuits that have short service life and are un-repairable "throw-away" electronics. Further, the design, materials, and processing choices are based on meeting economical production needs and often involve waste, aggressive chemistry and materials that are unsuited for space.

Understanding the behavior of basic materials in low-g and high vacuum and making the effort to fully exploit processes that are innately suited for space will lead to in-situ repairable electronic circuits. The extremely high cost of launching replacement hardware drives us toward electronic designs that provide long service life, but are also repairable, and can be reworked and reconfigured to serve alternate uses.

The spacecraft constraints imposed on the addition of new equipment are formidable. The development of several key capabilities will enable us to repair and rework spacecraft electronics without relying on Earth launched logistics. The CLEAR task is considering the strategy of compressing large test systems to small scale because of the huge cost of redesigning every known instrument into a small form factor. We are seeking alternate ways of diagnosing circuits by exploiting built in features where possible such as the JTAG Boundary Scan, and by looking at potential technology solutions such as Synthetic Instruments. Such concepts can be the first steps for a fabrication capability to help build infrastructure to support future missions.

The tele-operations developed for robotic repair can evolve into a fabrication capability as well. The experience learned from conducting repairs as well as the underlying materials and processes directly translates to operations for manufacturing with in-situ resources. Another possibility is to build additional infrastructure by reworking spent flight hardware for different functional use. This strategy need not wait for Mars – it can be employed and perfected in the Lunar Outpost phase. The near term need not be overlooked as the impact on logistics is already being felt as Space Shuttle support for ISS begins to draw to a close. By delivering capabilities starting with the ISS and then the Lunar Outpost, we can benefit from cost savings and early return on our development investments as well as gain confidence in their capability by the time we send humans to Mars.

Summary

NASA's historical solution to the problem of in-flight electronics repair has been the replacement of sub-units called Orbital Replacement Units. This approach requires significant logistical support through regular re-supply flights. For long-duration space missions, resupply flights are limited. Therefore, NASA is investigating component-level repair of electronics as a potential way to reduce the logistical footprint required to support future missions.

The Component-Level Electronics-Assembly Repair (CLEAR) project under the NASA Supportability program was established to develop and demonstrate the technology necessary to allow crew-member to effectively perform electronic repair down to the component level. CLEAR is looking at ways future exploration crew can, within the constraints of a spacecraft or habitat, (a) diagnose electronic assemblies and identify the faulty components, (b) repair electronics down to the component-level, (c) evaluate the circuit post repair via a functional test, and (d) augment the flight crew with knowledge and skills to diagnose faults and perform repairs without expanding crew size. These areas are investigated by a combination of trade studies, analysis, ground based testing, reduced gravity aircraft testing, and actual spaceflight testing aboard the ISS in multiple experiments. This paper provides an update to this task since previously reported at this meeting in the previous year.

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Certain commercial entities, equipment, or materials may be identified in this document in order to describe an experimental procedure or concept adequately. Such identification is not intended to imply recommendation or endorsement by the National Aeronautics and Space Administration, nor is it intended to imply that the entities, materials, or equipment are necessarily the best available for the purpose.

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