High-Performance, Radiation-Hardened Electronics for Space and Lunar Environments

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Abstract. The Radiation Hardened Electronics for Space Environments (RHESE) project develops advanced technologies needed for high performance electronic devices that will be capable of operating within the demanding radiation and thermal extremes of the space, lunar, and Martian environment. The technologies developed under this project enhance and enable avionics within multiple mission elements of NASA's Vision for Space Exploration, including the Constellation program's Orion Crew Exploration Vehicle, the Lunar Lander project, Lunar Outpost elements, and Extra Vehicular Activity (EVA) elements. This paper provides an overview of the RHESE project and its multiple task tasks, their technical approaches, and their targeted benefits as applied to NASA missions.

INTRODUCTION

The RHESE project is one of many technology development efforts within NASA's Exploration Technology Development Program (ETDP). This program exists to ensure the technology needs of NASA's current and future missions have available the appropriate enabling and enhancing technologies when needed. The RHESE project provides a full spectrum of approaches to harden space electronics against the radiation and thermal extremes of the space environment. Hardening approaches include new materials, design processes, reconfigurable hardware techniques, and software modeling tools. The primary customers of RHESE technologies will be the missions being developed under NASA's Constellation program within the Exploration Mission Systems Directorate (ESMD), including the lunar and Mars missions that will serve to accomplish the goals of the Vision for Space Exploration (NASA, 2004). Applicable Constellation program missions include the Orion Crew Exploration Vehicle's (CEV's) lunar capability, the Lunar Lander project, Lunar Outpost elements, and Extra Vehicular Activity (EVA) elements. Secondary customers for RHESE technologies include NASA science missions, collaborative efforts with other agencies of the US Government, and commercial applications. NASA's Marshall Space Flight Center (MSFC) manages the RHESE project.

Three broad-based approaches are being taken to address radiation hardening within the RHESE: improved electronic material hardness against radiation, design and configuration techniques to improve radiation hardness and tolerance, and software methods to model, predict, and improve radiation hardness and tolerance of devices. Within these approaches various technology products are being developed. The specific approaches to developing environmentally-hardened electronics within RHESE are accomplished through focused technology tasks. The specific verification and validation approach varies with each technology and is addressed more specifically in each technology description. In general, a ground-based demonstration in a relevant environment validates a technology product. Products are then ready for customer missions to flight test and qualify as part of their specific application of these technology products.

TECHNICAL TASKS WITHIN RHESE

Of the tasks developed within the RHESE project, the Modeling of Radiation Effects on Electronics (MREE) task aims to update the industry standard electronic modeling product, CREME96 (Tylka, 1997), such that it can continue to be employed in the design and assessment of state-of-the-art radiation hardened electronic devices. The Single Event Effects (SEE)-Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF) task focuses on design methods to be used in hardening reconfigurable FPGAs to radiation events. With respect to critical flight processor needs, the High Performance Processor (HPP) task pursues design methods and techniques that may result in a robust, low power, high performance, radiation hardened processor. The Reconfigurable Computing (RC) task addressed techniques to support long-duration mission needs for adaptable spares and fault tolerance functions. To address materials that are proving to be capable of enabling electronic operations in to extreme temperature ranges, the Silicon-Germanium (SiGe) Electronics task aims to deliver prototype subsystems capable of operating within environments that span a wide temperature range, specified for the Exploration missions as being -180 °C to 125 °C.

Described below are the active tasks within the RHESE project for fiscal year 2008. The previous fiscal year's RHESE project was described at the Government Microcircuit Applications and Critical Technology Conference of 2007 (Keys, 2007). Each task description includes task objectives, technology approach, and a summary of planned products and applications available for utilization by the technology customer.

Modeling of Radiation Effects on Electronics

The MREE task is developing a predictive model of radiation effects and how they affect modern advanced electronic architectures. This model will be employed to guide the selection of modern radiation hardened components for use in space systems. Designers may also use this model to predict the mean-time-between-failure (MTBF) of their circuit designs when selecting state-of-the-art commercial or radiation-hardened electronics for use in their flight avionics. This task will develop a tool to estimate and predict the frequency of the various single event effects such as logic upsets and circuit latch-up as well as the total radiation dose effects within these microelectronic devices as operated in the space environment.

The Monte Carlo method will be used within the simulation tool - allowing the shielding effect of the vehicle's exact structure to be considered when assessing the susceptibility of a particular microelectronic circuit to high energy particle radiation. This approach also allows the exact physical structure of the microelectronic circuit and the exact pattern of hole-electron creation within that circuit structure to be taken into account such that the resulting charges and currents within the circuit can be determined accurately. The tool will be developed jointly by NASA's MSFC and Vanderbilt University. The resulting model code will be used to propagate a large sample of particles from the external environment though the vehicle and the device. This allows accurate estimates to be made of total dose and the single event rates for the chip under investigation in its location within the space vehicle under any external environment model and in any orbit that is chosen. This model will be made available over the internet so that engineers can obtain total dose and single event effect rate estimates on line as is now possible with the industry standard CREME96 simulation models.

Technical Approach

MSFC will provide the models for the radiation environments to be used for the estimation of single event effects and total dose under various space weather conditions. MSFC will also provide Monte Carlo computer code to propagate the external radiation environment through the actual design of the spacecraft structure to the microelectronic chip that is being investigated. These codes will propagate individual particles, selected at random from the external particle environment striking the spacecraft, to and through the chip. During propagation the effects of nuclear interactions and energy loss by ionization will be taken into account. The result will be a list of individual particle descriptions and coordinates at the chip which are fed into the code generated by Vanderbilt University. These particle lists will also be used to predict the total radiation dose to the electronics.

Vanderbilt University will model the physical structure of the microelectronic circuit within the semiconductor material of the chip and propagate the individual particles from the list prepared by MSFC into the device structure. The Vanderbilt code will account for nuclear reactions, energy loss and hole-electron pair creation within and nearby the microelectronic circuit components. Vanderbilt will also develop classes to track the collection of charge

onto the nodes of the microcircuit from the distribution of hole-electron pairs created by the ionizing particle. There will also be code that examines how the circuit responds both to the charges collected on various nodes and to the currents resulting from the rates of charge collection at various points in the circuit. In particular, there will be code that predicts whether the passage of the charged particle through the chip leads to any single event effects. Table 1 outlines the primary objectives of the delivered radiation predictive modeling tool as used for the identified potential NASA customers.

TABLE 1. Pertinent objectives of the Modeling of Radiation Effects on Electronics task.

Objective	Performance Category	Key Performance Parameter	Units	State of the Art	Performance Target (Full Success)	Performance Target (Min Success)	Validation Method
Radiation Effects Predictive Models	Performance	Radiation Model Accuracy	Number of Technologies Included	Out of date	4 Technologies	2 Technologies	Test

Products and Application

Products from this task include: updated models/tools for estimating total dose and single event rates for electronic devices used in the space environment, and the publication of these models/tools on the World Wide Web (WWW) as an update to CREME96. As for applications, the model will be used by engineers to select radiation hard electronic parts for the design of circuits that are sufficiently robust to exceed the MTBF specification for their mission. It will also be used during failure analyses to determine the cause of failure by comparing actual failure rates with the predictions of this model. The radiation environment part of the model will be employed to predict the radiation environment that will be experienced by instruments that they are designing for space missions.

Single Event Effect (SEE)-Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF)

This task is managed and supported by NASA's Goddard Space Flight Center (GSFC), but is primarily led by the Air Force Research Laboratory (AFRL) and Sandia National Laboratory (SNL) in partnership with Xilinx and the University of Idaho Center for Advanced Microelectronics and Biomedical Research. Collectively, these contributors are collaboratively developing the design technologies required to implement a radiation-tolerant version of the Xilinx Virtex-5 FPGA. The resulting FPGA will yield the benefits of reconfigurable hardware without requiring the encumbrances (e.g. area, speed, power, complexity) typically needed to harden reconfigurable devices to radiation effects.

Technical Approach

SIRF FPGAs can be used to implement systems that incorporate radiation-tolerant reconfigurable interfaces and digital interconnects. This capability will facilitate design of common 'plug-and-play' modular, adaptive and reconfigurable subsystems. Such subsystems can be field programmed and reprogrammed to implement multiple functions in diverse systems. Table 2 summarizes the primary target objectives of the SIRF task.

TABLE 2. Pertinent objectives of the SIRF task.

Objective	Key Performance Parameters	Units	State of the Art (SOA)	Performance Target (Full Sucess)	Performance Target (Min Sucess)	Validation Method
Develop Total Dose Tolerant Electronics	Total Ionizing Dose (TID)	Krad	100(Si)	1000(Si)	300(Si)	Test
Reduce Single Event Upsets	Single Event Upset Rate	errors/bit-day	1.00E-05	1.00E-10	1.00E-10	Test
Reduce Single Event Latch-ups	Single Event Latch-Up	MeV-cm2/mg	75	Immune	100	Test

Products from this task include the development of Radiation Hardening By Design (RHBD) techniques implemented to produce radiation tolerant Virtex-5 FPGA technology. An example of application includes the scenario where a SIRF-based processor board is removed from a lunar storage depot and inserted into a rover navigation system. Upon insertion, the board autonomously downloads configuration data, configures its electrical interfaces and internal interconnects, and executes the desired functionality. It will also continuously monitor its performance and self-reconfigure to mitigate faults, should they occur. The same board can, should the need arise, be removed from the rover and be used to replace a malfunctioning board in an oxygen generating system. Once inserted, it will be autonomously configured for this application. Significant systems efficiencies including development, fault-tolerance, maintenance, repair, and inventory control will result from this capability.

In addition, SIRF-based technologies can be used for high-bandwidth sensor back-end applications, e.g. vision processing, radar and Light Detection and Ranging (LIDAR) applications, since gate array-based processors demonstrate significant performance advantages over serial processors when implementing tasks that can be parallelized. SIRF will have the additional advantage of being able to realize this performance advantage without the inefficiencies associated with single-event effect mitigation techniques.

High Performance Processors

Implementation ESMD objectives and strategies can be highly constrained by onboard computing capabilities and power efficiencies. RHESE's High Performance Processors project will address this challenge by significantly advancing the sustained throughput and processing efficiency of high-performance radiation-hardened processors, targeting delivery of products by the end of fiscal year 2012.

This task will identify emerging developments of new processors and new applications of existing processors into devices suitable for use in space environments. The included range of applied processors investigated ranges from highly capable flight control computers and special purpose processors to individual personal computers used by crewmembers. While other environmental variables inherent to space applications will be considered, such as extremes of temperature, this task will focus primarily on radiation effects. The task will identify both developments of radiation-hardened by design components, as well as application of mitigation techniques used to reduce component susceptibility to radiation effects. This task is lead by NASA's GSFC, with support from NASA's MSFC, NASA's Langley Research Center (LaRC), and the Jet Propulsion Laboratory (JPL).

It is essential that HPP delivers products consistent with the anticipated processing challenges of Exploration architectures in a timely manner. It is not tractable to wait until all Exploration requirements have been established before this task of processor development is undertaken. The project is therefore implementing a capability-driven approach in lieu of a requirements-driven approach for this phase of the program- performance metrics are derived based on multiple inputs, including architecture studies, working group discussions, interchange discussions, and RHESE team-resident knowledge of system and architecture objectives.

The objective is to identify emerging developments of new processors and new applications of existing processors into devices suitable for use in space environments. The range of applications will include the broad field from flight control computers to individual personal computers used by crewmembers. While other environments inherent in space applications will be considered, such as extremes of temperature, this task will look primarily at radiation effects.

Technical Approach

The HPP task will develop a spaceflight processor that addresses processing-constrained capabilities of Exploration spaceflight systems. It will advance radiation-hardened processor technology state-of-the-art with the goal of improving sustained throughput and power efficiency metrics to values exceeding the capabilities of an industry standard processor, the RAD750, by an order of magnitude. Enabling and enhancing technologies from relevant programs funded by NASA, other government agencies, industry, and academia (e.g. 90 nm RHBD techniques, radiation-hardened systems-on-a-chip, and multi-core processors) will be leveraged in executing this task.

The performance of processors developed with technologies appropriate for aerospace environments lags that of commercial processors by multiple performance generations. For example, one of the "flagship" radiation-tolerant processors— the RAD750— exhibits a sustained throughput rate that is approximately two-orders of magnitude less than the commercially available Intel Centrino processor, used in many desktop and laptop computers.

Whereas radiation tolerant COTS-based boards that offer increased performance are available, the performance is offered at expense of reduced power efficiency. This task seeks to advance the state of the art of two metrics (sustained throughput and processing efficiency) of high-performance radiation-hardened processors by at least one order of magnitude. The resultant goals are throughput greater than 2000 MIPS with efficiency better than 500 MIPS/W. Figure 1 maps the capabilities of multiple commercial grade and radiation-hardened processors against a processor throughput metric. It can be seen that the processors follow a Moore's Law distribution with the radiation-hardened processors generally lagging commercial processors of comparable capability by about a decade. Table 3 summarizes the primary target objectives of the HPP task.
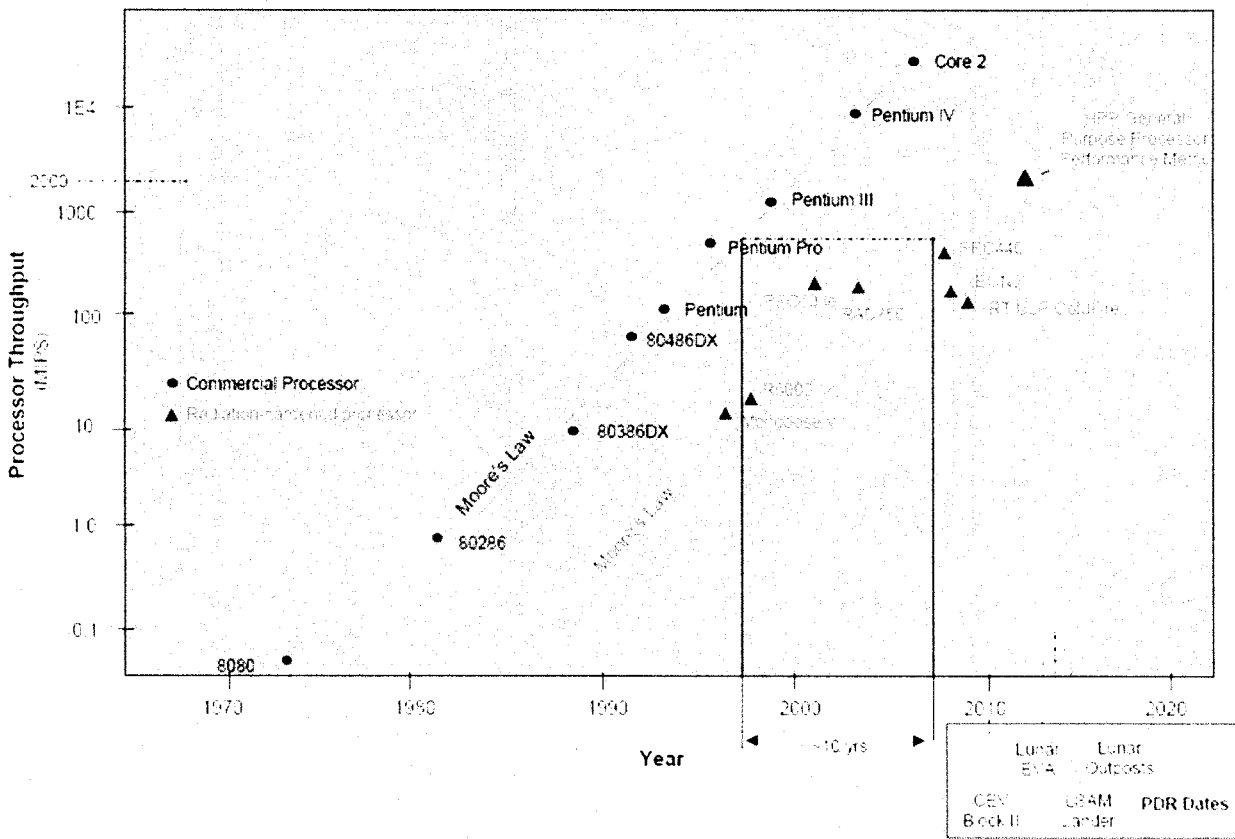

FIGURE 1. Mapping of Commercial and Rad-Hard Processors against "Moore's Law" Curve.

The need for power-efficient high-performance radiation-tolerant processors and the peripheral electronics required to implement functional systems is not unique to NASA; this capability could also benefit commercial aerospace entities and other governmental agencies that require highly-capable spaceflight systems. This task will therefore leverage to the extent practical, relevant external technology- and processor-development projects sponsored by other organizations. An important factor in defining the strategy and the corresponding long-term schedule for this task will therefore be the investment plans of these organizations and documentation on prior NASA investments.

This effort will be addressed from a system-level perspective; meeting the objective will require peripheral devices that exhibit performance and environmental characteristics consistent with the processor. This task will therefore

also investigate the availability and development status of components required to realize nominal high-performance spaceflight systems architecture. Table 3 summarizes the primary target objectives of the HPP task.

TABLE 3. Pertinent objectives of the High Performance Processors task.

Objective	Performance Category	Key Performance Parameter	Units	State of the Art	Performance Target (Full Success)	Performance Target (Min Success)	Validation Method
High Performance Processors	Performance	Sustained Processor Performance	MIPS	200	2000	500	Test
		Sustained Processor Efficiency	MIPS/W	50	500	100	
	Radiation Tolerance	Total Ionizing Dose	Krad (Si)	<100	100	100	
		Single Event Upset Rate	errors/bit-day	1.00E-11	1.00E-13	1.00E-12	
		Single Event Latchup	Mev-Cm2/mg	>75	>105	>105	
	Temperature	Temperature Performance	C	-55 to +125	-55 to +125	-55 to +125	

Products and Applications

Products include: a high-performance radiation-hardened general-purpose processor and a high-performance radiation-hardened special-purpose processor.

As for applications of this technology, the task objective may be accomplished with multiple types of processors or processor cores, given the broad range of applications that will require significant processing capability. Targeted classes include high-capability general purpose processors (e.g. a RAD750-type technology), instrument-level general purpose processors, and special purpose processors.

Reconfigurable Computing

Reconfigurable computing (RC) offers new capabilities in spacecraft system reconfiguration. These capabilities provide reduced flight spares inventories for long-duration missions, adaptability to system failures, and flexibility in connecting components through a variety of data interfaces. A conceptual approach to dynamic avionic configuration is proposed - allowing circuitry to guard against failures in ways other than by redundancy voting schemes alone. This new conceptual approach will not only better detect failed circuitry, but will accomplish actual repair or replacement of defects, adapting circuitry to accommodate system failures.

The concept of reconfigurable computing focuses on the development of a single set of digital processor circuits capable of recognizing and reconfiguring into multiple application-oriented configurations. This capability addresses the flight system requirement of having available spare components, boards and subsystems for all spacecraft processing application hardware. Instead, reconfigurable computing provides a single spare for multiple processing functions. Such architecture adaptability provides a great saving in spares volume and weight required by extended duration missions.

Technical Approach

The development of a reconfigurable computing capability will rely heavily on Field-Programmable Gate Array (FPGA) "fabrics," and controlling firmware capable of recognizing processing states in which the FPGA must be reconfigured into a more protected or capable state of operation. The objectives addressed by this task are presented in Table 4.

TABLE 4. Pertinent objectives of the Reconfigurable Computing task.

Objective	Performance Category	Key Performance Parameter	Units	State of the Art	Performance Target (Full Success)	Performance Target (Min Success)	Validation Method
Reconfigurable Computing	Performance	Sustained Processor Performance	MIPS	200	2000	500	Test
		Sustained Processor Efficiency	MIPS/W	50	500	100	
		Reconfigurability	# Levels	None	4	3	
	Radiation Tolerance	Total Ionizing Dose	Krad (Si)	<100	100	100	
		Single Event Upset Rate	errors/bit-day	1.00E-11	1.00E-13	1.00E-12	
		Single Event Latchup	Mev-Cm2/mg	>75	>105	>105	
	Temperature	Temperature Performance	C	-55 to +85	-55 to +125	-55 to +125	

This task relies heavily on testing to ensure the reliability of the reconfigurable capability and the safety of the process. Verification of the capabilities produced will be accomplished by two means, both involving testing. First, since exposure to harsh environments will not necessarily guarantee errors, it will be necessary to induce known errors. Various means for inducing these errors in a methodical manner will be devised. Second, testing in actual environmental chambers will be carried out to simply demonstrate validity of the schemes under harsh conditions representative of planned target flight environments. Upon conclusion of development and demonstration, general system integration will be undertaken. The end goal of this effort will then be to accomplish technology infusion into current and future flight systems.

Products and Applications

Products include: reconfigurable computers supporting multiple architectures to enable single spares to fulfill multiple electronic functions, reconfigurable computers supporting avionics redundancy by providing adaptable spares, reconfigurable computers supporting recovery from component damage by radiation strikes and other events and, reconfigurable computers supporting multiple interfacing and interconnection options.

Silicon Germanium Electronics for Extreme Environments

The goal of this task is to develop and demonstrate extreme environment electronics components required for lunar robotic systems with distributed architecture, using low-cost, commercial SiGe BiCMOS technology. SiGe BiCMOS offers unparalleled low temperature performance, wide temperature capability, and optimal mixed-signal design flexibility at the monolithic level by offering power efficient, high speed devices (SiGe HBTs) and high density Si CMOS. The current approach for rovers is to locate electronics in protective 'warm boxes' for planetary surface systems. This limits the ability to create a truly distributed, modular electronics system, resulting in excessive point-to-point wiring, increased system weight and complexity and reduced reliability. The challenges in future phases will become more daunting with the planned larger rovers incorporating an increasing number of sensors, imagers, motors and actuators.

Technical Approach

The goals of the SiGe task may be summarized as the ability to demonstrate system-critical SiGe BiCMOS mixed-signal integrated circuit components capable of operating reliably from -180 °C to +120 °C, and under radiation exposure. Included in this demonstration is the packaging required to host the electronics. The work in SiGe will culminate in the fabrication of a flight-ready remote electronics unit (REU) system prototype to serve as a general purpose, extreme environment ready, sensors and control interface system-in-package for NASA missions. The specific objectives addressed by the SiGe task are shown in Table 5.

TABLE 5. Pertinent objectives of the SiGe Electronics for Extreme Environments task.

Objective	Key Performance Parameters	Units	State of the Art (SOA)	Performance Target (Full Sucess)	Performance Target (Min Sucess)	Validation Method
Develop Total Dose Tolerant Electronics	Total Ionizing Dose (TID)	krad(SiO2)	10	300	100	Test
Reduce Single Event Upsets	Single Event Upset Rate	errors/bit-day	1.00E-10	1.00E-13	1.00E-12	Test
Reduce Single Event Latch-ups	Single Event Latch-Up	MeV-cm2/mg	75	Immune	100	Test
Improve the Low Temperature Operating Limits	Temperature Range	C	-55	-230	-180	Test

Products and Applications

This task will produce a series of wide-temperature range (120 °C to -180 °C) mixed-signal SiGe chips with specific circuit components, including:

- Low Temperature Analog Circuits (Voltage References, Current References, General Purpose Op-Amps, Sensor/Image Pre-Amps, Temperature Sensors, Voltage Regulators, Phased Locked-Loop Amplifiers),
- Low Temperature Data Converters (Analog to Digital and Digital to Analog),
- Low Temperature Digital Circuits (Comparators, Mux/Demux, Clock Generator, Modulator/Demodulator),
- Low Temperature Power Electronics (Line Regulators, Bus Interface Circuits, Motor/Actuator pre-drivers, Motor/Actuator drivers, H-Bridges, High Side Drivers, PWM Controllers, dc-dc Converters), and
- Low Temperature Circuit Packaging.

CONCLUSIONS

In summary, the RHESE project takes a multifaceted approach to developing technology to be used in electronics that must operate within the radiation and temperature extremes of the space environment. Included within the fiscal year 2008 project are the MREE task, the SIRF task, the HPP task, the RC task, and the SiGe electronics task. Together, these tasks aim to provide RHESE's primary customers, the missions required to fulfill the Vision for Space Exploration, with the technologies needed to fulfill their missions in space, on the lunar surface and eventually in the exploration of the planet Mars.

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