Technology Developments in Radiation-Hardened Electronics for Space Environments

By Andrew S. Keys[1)] and Joe T. Howell[1)]

[1)]*NASA's Marshall Space Flight Center, Huntsville, Alabama, USA*

The Radiation Hardened Electronics for Space Environments (RHESE) project consists of a series of tasks designed to develop and mature a broad spectrum of radiation hardened and low temperature electronics technologies. Three approaches are being taken to address radiation hardening: improved material hardness, design techniques to improve radiation tolerance, and software methods to improve radiation tolerance. Within these approaches various technology products are being addressed including Field Programmable Gate Arrays (FPGA), Field Programmable Analog Arrays (FPAA), MEMS, Serial Processors, Reconfigurable Processors, and Parallel Processors. In addition to radiation hardening, low temperature extremes are addressed with a focus on material and design approaches. System level applications for the RHESE technology products are discussed.

Key Words: radiation-hardened, microelectronics, extreme environments, FPGA, SiGe

1. Introduction

The Radiation-Hardened Electronics for Space Exploration (RHESE) project is one of many technology development efforts within NASA's Exploration Technology Development Program (ETDP). This program exists to ensure the technology needs of NASA's current and future missions have available the appropriate enabling and enhancing technologies when needed. The RHESE project provides a full spectrum of approaches to harden space electronics against the radiation and thermal extremes of the space environment. Hardening approaches include new materials, design processes, reconfigurable hardware techniques, and software modeling tools. The primary customers of RHESE technologies will be the missions being developed under NASA's Constellation program within the Exploration Mission Systems Directorate (ESMD), including the lunar and Mars missions that will serve to accomplish the goals of the Vision for Space Exploration. Applicable Constellation program missions include the Orion Crew Exploration Vehicle's (CEV's) lunar capability, the Lunar Lander project, Lunar Surface System elements, and Extra Vehicular Activity (EVA) elements. Secondary customers for RHESE technologies include NASA science missions, collaborative efforts with other agencies of the US Government, and commercial applications. NASA's Marshall Space Flight Center (MSFC) manages the RHESE project.

Three broad-based approaches are being taken to address radiation hardening within the RHESE: improved electronic material hardness against radiation, design and configuration techniques to improve radiation hardness and tolerance, and software methods to model, predict, and improve radiation hardness and tolerance of devices. Within these approaches various technology products are being developed. The specific approaches to developing environmentally-hardened electronics within RHESE are accomplished through focused technology tasks. The specific verification and validation approach varies with each technology and is addressed more specifically in each technology description. In general, a ground-based demonstration in a relevant environment validates a technology product. Products are then ready for customer missions to flight test and qualify as part of their specific application of these technology products.

2. RHESE Technology Tasks

Described below are the active technology development tasks within the RHESE project for fiscal year 2008. Each technology task section includes a brief task description, technology approach, and a summary of planned products and applications available for utilization by the technology customer.

2.1. Modeling of Radiation Effects on Electronics (MREE)

RHESE is developing an update to the existing predictive modeling capabilities of radiation effects and how they affect modern advanced electronic architectures. Referenced to as MREE, this modeling tool will be employed to guide the selection of modern radiation hardened components for use in space systems. Designers may also use this model to predict the mean-time-between-failure (MTBF) of their circuit designs when selecting state-of-the-art commercial or radiation-hardened electronics for use in their flight avionics. The MREE task will develop a tool to estimate and predict the frequency of the various single event effects such as logic upsets and circuit latch-up as well as the total radiation dose effects within these microelectronic devices as operated in the space environment.

The Monte Carlo method will be used within the MREE simulation tool - allowing the shielding effect of the vehicle's

exact structure to be considered when assessing the susceptibility of a particular microelectronic circuit to high energy particle radiation. This approach also allows the exact physical structure of the microelectronic circuit and the exact pattern of hole-electron creation within that circuit structure to be taken into account such that the resulting charges and currents within the circuit can be determined accurately. The tool will be developed jointly by MSFC and Vanderbilt University.

The resulting model code will be used to propagate a large sample of particles from the external environment though the vehicle and the device. This allows accurate estimates to be made of total dose and the single event rates for the chip under investigation in its location within the space vehicle under any external environment model and in any orbit that is chosen. This model will be made available over the internet so that engineers can obtain total dose and single event effect rate estimates on line as is now possible with the industry standard CREME96 simulation models.

2.1.1 MREE Technical Approach

MSFC will provide the models for the radiation environments to be used for the estimation of single event effects and total dose under various space weather conditions. MSFC will also provide Monte Carlo computer code to propagate the external radiation environment through the actual design of the spacecraft structure to the microelectronic chip that is being investigated. These codes will propagate individual particles, selected at random from the external particle environment striking the spacecraft, to and through the chip. During propagation the effects of nuclear interactions and energy loss by ionization will be taken into account. The result will be a list of individual particle descriptions and coordinates at the chip which are fed into the code generated by Vanderbilt University. These particle lists will also be used to predict the total radiation dose to the electronics.

Vanderbilt University will model the physical structure of the microelectronic circuit within the semiconductor material of the chip and propagate the individual particles into the device structure. The Vanderbilt code will account for nuclear reactions, energy loss and hole-electron pair creation within and nearby the microelectronic circuit components. Vanderbilt will also develop routines to track the collection of charge onto the nodes of the microcircuit from the distribution of hole-electron pairs created by the ionizing particle. There will also be code that examines how the circuit responds both to the charges collected on various nodes and to the currents resulting from the rates of charge collection at various points in the circuit. In particular, there will be code that predicts whether the passage of the charged particle through the chip leads to any single event effects.

To summarize, the first goal of the MREE task is to develop a revised calorimetric approach to single event effect (SEE) prediction that explicitly includes SEEs caused by the products of inelastic nuclear reactions between the incident particle and nuclei in or near the device. This will allow SEEs caused by interactions with chip fabrication materials such as silicon, aluminum, copper and tungsten to be explicitly accounted for. The second goal of the project is to estimate SEE rates using a physics-based description of charge transport and collection within the semiconductor device. Two approaches will be attempted: direct calculation as is currently done with commercial software tools such as Technology Computer Aided Design (TCAD) and technology-specific approximated calculations based on generalizations from TCAD results in specific devices.

2.2. Single Event Effect (SEE)-Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF)

This task is managed and supported by Goddard Space Flight Center (GSFC), but is primarily led by the Air Force Research Laboratory (AFRL) and Sandia National Laboratory (SNL) in partnership with Xilinx and the University of Idaho Center for Advanced Microelectronics and Biomedical Research. Collectively, these contributors are collaboratively developing the design technologies required to implement a radiation-tolerant version of the Xilinx Virtex-5 FPGA. The resulting FPGA will yield the benefits of reconfigurable hardware without the typical encumbrances of a larger chip area, lower processing speed, higher power consumption, or higher complexities typically needed to harden reconfigurable devices to radiation effects.

2.2.2. SIRF Products and Applications

Products from this task include the development of radiation hardening by design (RHBD) techniques implemented to produce radiation tolerant Virtex-5 FPGA technology. As for applications of the technology, SIRF FPGAs can be used to implement systems that incorporate radiation-tolerant reconfigurable interfaces and digital interconnects. This capability will facilitate design of common ‘plug-and-play’ modular, adaptive and reconfigurable subsystems. Such subsystems can be field programmed and reprogrammed to implement multiple functions in diverse systems. A SIRF-based processor board can, for example, be removed from a lunar storage depot and inserted into a rover navigation system. Upon insertion, the board will autonomously download configuration data, configure its electrical interfaces and internal interconnects, and execute the desired functionality. It will also continuously monitor its performance and self-reconfigure to mitigate faults, should they occur. The same board can, should the need arise, be removed from the rover and be used to replace a malfunctioning board in an oxygen generating system. Once inserted, it will be autonomously configured for this application. Significant systems efficiencies including development, fault-tolerance, maintenance, repair, and inventory control will result from this capability.

In addition, SIRF-based technologies can be used for high-bandwidth sensor back-end applications, e.g. vision processing, radar and LIDAR, since gate array-based processors demonstrate significant performance advantages over serial processors when implementing tasks that can be parallelized. SIRF will have the additional advantage of being able to realize this performance advantage without the inefficiencies associated with single-event effect mitigation techniques.

2.3. High Performance Processors (HPP)

Implementation of processor-intensive mission objectives and strategies can often be highly constrained by available onboard computing capabilities and power efficiencies. RHESE's HPP task will address this challenge by significantly advancing the sustained throughput and processing efficiency of high-performance radiation-hardened processors, targeting delivery of products by the end of fiscal year 2012.

This task will identify emerging developments of new processors and new applications of existing processors into devices suitable for use in space environments. The included range of applied processors investigated ranges from highly capable flight control computers and special purpose processors to individual personal computers used by crewmembers. While other environmental variables inherent to space applications will be considered, such as extremes of temperature, this task will focus primarily on radiation effects. The task will identify both developments of radiation-hardened by design components, as well as application of mitigation techniques used to reduce component susceptibility to radiation effects. This task is lead by the GSFC, with support from MSFC, Langley Research Center (LaRC), and the Jet Propulsion Laboratory (JPL).

It is essential that HPP delivers products consistent with the anticipated processing challenges of Exploration architectures in a timely manner. It is not tractable to wait until all Exploration requirements have been established before this task of processor development is undertaken. The project is therefore implementing a capability-driven approach in lieu of a requirements-driven approach for this phase of the program- performance metrics are derived based on multiple inputs, including architecture studies, working group discussions, interchange discussions, and RHESE team-resident knowledge of system and architecture objectives.

2.3.1. HPP Technical Approach

HPP will develop a spaceflight processor that seeks to benefit processing-constrained capabilities of Exploration spaceflight systems. Enabling and enhancing technologies from relevant programs funded by NASA, other government agencies, industry, and academia (e.g. 90 nm RHBD efforts, radhard system-on-a-chip, and multi-core processors) will be leveraged during the development of this task.

The HPP technology task will attempt to leverage, to the fullest extent appropriate, relevant processor development efforts sponsored by other US government organizations and prior work funded by NASA. An important factor in defining the strategy and the corresponding long-term schedule for this task will therefore be the investment plans of these organizations and documentation on prior NASA investments. Pending these data, this project will seek to deliver a processor with the performance metrics defined above by the end of FY12. In order to better understand the magnitude and complexity of the HPP tasks these next paragraphs will explain current processor technology.

2.3.2. Current Processor Technology

The performance of processors developed with technologies appropriate for aerospace environments lags that of commercial processors by multiple performance generations. For example, one of the "flagship" radiation-tolerant processors, BAE's RAD750, exhibits approximately 100 MIPS sustained throughput. This compares to greater than 6000 MIPS for an Intel Centrino processor, used in many desktop and laptop computers.

Whereas radiation tolerant COTS-based boards that offer increased performance are available (~1000 MIPS), the performance is offered at expense of reduced power efficiency. This task seeks to advance the state of the art of two metrics (sustained throughput and processing efficiency) of high-performance radiation-hardened processors by at least one order of magnitude. The resultant goals are throughput greater than 2000 MIPS with efficiency better than 500 MIPS/W.

The need for power-efficient high-performance radiation-tolerant processors and the peripheral electronics required to implement functional systems is not unique to NASA; this capability could also benefit commercial aerospace entities and other governmental agencies that require highly-capable spaceflight systems. This task will therefore leverage to the extent practical, relevant external technology- and processor-development projects sponsored by other organizations. An important factor in defining the strategy and the corresponding long-term schedule for this task will therefore be the investment plans of these organizations and documentation on prior NASA investments.

This effort will be addressed from a system-level perspective; meeting the objective will require peripheral devices that exhibit performance and environmental characteristics consistent with the processor. This task will therefore also investigate the availability and development status of components required to realize nominal high-performance spaceflight systems architecture.

2.3.3. HPP Products and Applications:

The HPP task's objectives may be accomplished with multiple types of processors or processor cores, given the broad range of applications that will require significant processing capability. Targeted classes include high-capability general purpose processors (e.g. a RAD750-type technology), instrument-level general purpose processors (e.g. ColdFire or microcontroller technology), and special purpose processors (e.g. FPGA-resident soft- or hard-core, reconfigurable processor, digital signal processor, or a host processor/coprocessor combination).

2.4. Reconfigurable Computing (RC)

Reconfigurable computing (RC) offers new capabilities in spacecraft system reconfiguration. These capabilities provide reduced flight spares inventories for long-duration missions, adaptability to system failures, and flexibility in connecting components through a variety of data interfaces. A new paradigm is proposed for circuitry to respond to failures other than by redundancy voting schemes alone. This new paradigm will not only better detect failed circuitry, but will accomplish actual repair or replacement of defects, adapting circuitry to accommodate system failures.

The paradigm also provides the capability of a single

processor conforming to multiple configurations. This yields a reduction in spares required to be carried on long-duration missions, since a single spare will fit many processing functions. Such architecture adaptability will provide a great saving in spares volume and weight required by extended duration missions.

Cyclical and selective periodic testing will mitigate radiation damage and other failure sources commonly feared. Reserve copies of circuitry will be generated and tested in order to bring them online in functional condition without interrupting system tasks. Then, the subsystem to be evaluated will be taken offline and tested with known inputs for known expected outputs in order to isolate possible undesirable response. Provided the subsystem checks out as functionally correct, it can be returned to service, held in reserve for the next cycle of checks, or disassembled so that its circuitry may be returned to overall system reserve. If the subsystem fails verification, the portions of circuitry causing the failure may be further isolated to mark those parts of the circuitry as defective and return the remainder to reserve, much as blocks of a computer hard disk are marked bad and ignored during future operations. Life limitations on electronics can be mitigated by these same means. Circuitry which becomes unstable and unreliable after extended active lifetime can be retired and new reserve circuitry powered up and configured into service, thus extending overall lifetime of the system. Flexibility is also bolstered by RC. Interface reconfiguration can allow a single processor make connections through different networks as needed, providing more options in overall system configuration. This supports vehicle system integrity by allowing processors to be transferred among busses and networks to replace lost functionality, and supports the concept of reduced flight spares required to maintain long duration missions.

2.4.1. RC Technical Approach

Verification of the capabilities produced will be accomplished by two means, both involving testing. First, since exposure to harsh environments will not necessarily guarantee errors, and even supposing errors do result, their nature and behavior cannot be rigorously controlled, it will be necessary to induce known errors. Various means for inducing these errors in a methodical manner, in order to cover the full spectrum of foreseeable malfunctions, will have to be devised. Second, testing in actual environmental chambers will be carried out to simply satisfy the validity of the schemes under harsh conditions representative of planned target flight environments.

Three areas of focus have been identified. These are internal modularity, external modularity, and fault detection and mitigation. The first involves ability of the core processor to emulate any form of computing resource as needed to serve all of the capacities required. The second enables the first by providing a capability to interface resources to any target system, by adapting communication standards, physical and electrical interconnections, and other parameters of the host system to hook up to the computing resource. Finally, increasingly complex forms of fault identification and response are to be studied and applied; those relying particularly on the strengths of RC itself will allow substitution of tested computing resources for those in line for maintenance to allow removal, testing, and refurbishment of the latter without interruption of system operation.

A test bed is under development for the purpose of concept development and demonstration. Several different applications are targeted for emulation on this system, to first enable showcasing of the concepts of modularity in a host processor and later to be able to fold in advancing features of interface modularity and fault handling. Test bed hardware currently centers on FPGA "fabrics," large arrays of FPGA devices encoding algorithms and general digital logic functionality directly into hardware and bypassing much of the slower serial-based processing characteristic of standard CPU- and software-based systems. In the near future, efforts will branch out into more advanced node- or object-oriented hardware options currently showing promise; these tend to trade off some of the general, fine-grained features of FPGA for speed and ease of use improvements gained in semi-custom approaches.

Verification of the capabilities produced will be accomplished by two means, both involving testing. First, since exposure to harsh environments will not necessarily guarantee errors, and even supposing errors do result, their nature and behavior cannot be rigorously controlled, it will be necessary to induce known errors. Various means for inducing these errors in a methodical manner, in order to cover the full spectrum of foreseeable malfunctions, will be devised. Second, testing in actual environmental chambers will be carried out to simply demonstrate validity of the schemes under harsh conditions representative of planned target flight environments. Upon conclusion of development and demonstration, general system integration will be undertaken. The end goal of this effort will then be to accomplish technology infusion into current flight systems.

2.4.2. RC Products and Applications

Anticipated products resulting from the development of the RC technology task include reconfigurable computers supporting multiple architectures, reconfigurable computers supporting avionics redundancy by providing adaptable spares, reconfigurable computers supporting recovery from component damage by radiation strikes and other events and, reconfigurable computers supporting multiple interfacing and interconnection options.

2.5. Silicon Germanium (SiGe) Electronics for Extreme Environments

The goal of this task is to develop and demonstrate extreme environment electronic components required for lunar robotic systems with a distributed avionic architecture, using low-cost, commercial SiGe Bi-Complementary Metal Oxide Semiconductors (BiCMOS) technology. SiGe BiCMOS offers unparalleled low temperature performance, wide temperature capability, and optimal mixed-signal design flexibility at the monolithic level by offering power efficient, high speed devices, such as the SiGe Heterojunction Bipolar Transistor (HBT), and high density Si CMOS. The current approach for rovers is to locate

electronics in protective 'warm boxes' for planetary surface systems. This limits the ability to create a truly distributed, modular electronics system, resulting in excessive point-to-point wiring, increased system weight and complexity and reduced reliability.

The challenges in future phases will become more daunting with the planned larger rovers incorporating an increasing number of sensors, imagers, motors and actuators. This program will raise SiGe BiCMOS extreme environment electronics technology, including packaging, from a low technical maturity level to one that is ready for flight validation.

2.5.1. SiGe Technical Approach:

This SiGe task seeks to demonstrate system-critical SiGe BiCMOS mixed-signal integrated circuit components capable of operating reliably within temperature ranges of -180C to +120C while under radiation exposure. Additionally, this task seeks to demonstrate reliable packaging technologies that perform within the temperature range of -180C to +120C while undergoing multiple thermal cycles between the temperature range extremes. These goals will be achieved through the development of a flight-ready multi-channel remote electronics unit (REU) designed to be located within the extreme environment where it will collect multiple signals from end effectors and sensors, then transmit the aggregate signal to a central processor, located within the protected regions of the spacecraft avionics architecture.

The verification phase of this project will consist of characterization of the various mixed-signal components of the library as a function of temperature, from -180C to 120C. It will also include radiation characterization to a total ionizing dose of at least 100 krad, life testing at the temperature extremes of -180C and 120C, and over-temperature cycle testing. Additional testing of components at cryogenic temperatures under radiation exposure will be used to evaluate the combined effects of temperature and radiation. The requisite pass/fail criterion under these evaluations is that the mixed-signal components should maintain defined performance specifications to within 20% variation.

3. RHESE Potential System Level Applications

Described below are potential future system level applications of RHESE technology for the exploration and development of space. Each section includes a brief application description and discussion of the benefits to space exploration.

3.1. Direct-Drive Solar Electric Transportation Systems

Direct-drive solar electric[1)] transportation systems are low thrust which produce a slow spiral trajectory when going for low Earth orbit (LEO) to geostationary Earth orbit (GEO). The slow spiral trajectory keeps the transportation system sometimes referred to as space tug and the payload being transferred in the Earth radiation belt for an extended period of time. Therefore, the RHESE technology is very important to both the transportation system and the payload. However, RHESE technology is especially important the transportation system since it would be making many trips between LEO to GEO and back.

The slow spiral trajectory takes months (maybe 3 to 6) from LEO to GEO which is certainly a factor in the overall life cycle cost of a mission. However, the cost savings for transferring cargo from LEO to GEO and to lunar orbit with a reusable direct-drive solar electric transportation systems can be enormous. Thus, the saying time is money can go both ways.

3.2. In-Space Cryogenic Propellant Depot

An In-Space Cryogenic Propellant Depot (ISCPD) [2)] can preposition and store propellants in space for exploration and commercial space activities. To be an effective component of space exploration architectures the ISCPD will be exposed to the space environment for many years. Therefore, the RHESE technology is very important to the many systems and subsystems being exposed to the long duration space radiation.

An In-Space Cryogenic Propellant Depot can enable more ambitious and affordable human and robotic exploration of space both near Earth and beyond. The servicing of propellants and consumables in space enables a multitude of mission scenarios, otherwise unavailable due to costs or operational constraints and/or inefficiencies. The ISCPD can support the reusability of space exploration systems as well as servicing of commercial systems.

4. Conclusions

In summary, the RHESE project uses a multifaceted approach to developing technology to be used in electronics that must operate within the radiation and temperature extremes of the space environment. Included within the fiscal year 2008 project are the MREE task, the SIRF task, the RC task, the HPP task, and the SiGe Electronics task. Together, these tasks aim to provide RHESE's primary customers, the missions required to fulfill the US Space Policy, with the technologies needed to fulfill their missions in space, on the lunar surface and eventually in the exploration of the planet Mars.

References

1) Howell, J.T., O'Neill, M.J. and Mankins, J.C.: High-Voltage High-Energy Stretched Lens Array Square-Rigger (SLASR) for Direct-Drive Solar Electric Propulsion, *ISTS 2006*, Kanazawa, Japan, 2006.
2) Fikes, J.C., Howell, J.T. and Henley, M.W., "In-space Cryogenic Propellant Depot (ISCPD) Architecture Definitions and Systems Studies, *IAC-06-D3.3.008*, 2006.