Characterizing SRAM Single Event Upset in Terms of Single and Double Node Charge Collection

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Abstract

A well-collapse source-injection mode for SRAM SEU is demonstrated through TCAD modeling. The recovery of the SRAM's state is shown to be based upon the resistive path from the p+-sources in the SRAM to the well. Multiple cell upset patterns for direct charge collection and the well-collapse source-injection mechanisms are then predicted and compared to recent SRAM test data.

I. Introduction

The study and analysis of static random access memory (SRAM) single event upset (SEU) has been ongoing since the late 1970s [1, 2]. Diehl et al. identified strikes to the OFF nMOSFET drain and OFF pMOSFET drain as the underlying events responsible for SRAM SEU and used circuit modeling to demonstrate the mechanism [3]. Over the years, as SRAM cells have scaled down in size, a new effect was observed: multiple cell upsets (MCU) from a single event [4]. Dodd et al. used mixed-mode device/circuit modeling to demonstrate that the MCU mechanism is due to charge collection in adjacent SRAM cells [5]. However, the most widely considered mechanism for SRAM upset remains charge collection at an OFF transistor drain, which we will denote as direct charge collection (DCC). This paper examines a mechanism for SRAM SEU due to indirect charge collection, called well-collapse source-injection (WCSI). MCU patterns for each respective mechanism are then predicted and compared to recent SRAM test data.

A basic SRAM cell consists of six transistors: two cross coupled inverters (four transistors) and two access pass-gate transistors. A 3-D TCAD model of a SRAM cell was constructed using Synopsys Dessis. A top view of the cell is shown in Figure 1. The SRAM cell is representative of an unhardened 90-nm SRAM cell fabricated in an epitaxial CMOS technology. This SRAM design upsets in TCAD simulations with a charge deposition of 0.005 pC/μm (LET = ~0.5 MeV-cm^2/mg) due to DCC at the drain of the OFF nMOSFET (NHIT) at Point 1 in Figure 1. If the charge deposition is increased to 0.45 pC/μm (LET = ~45 MeV-cm^2/mg), the SRAM cell upsets initially due to direct charge collection, enters a metastable state, and then recovers to the original state as shown in Figure 2. The initial upset is due to DCC. The entrance into and recovery from the metastable state is due to indirect charge collection in the pMOSFETs.

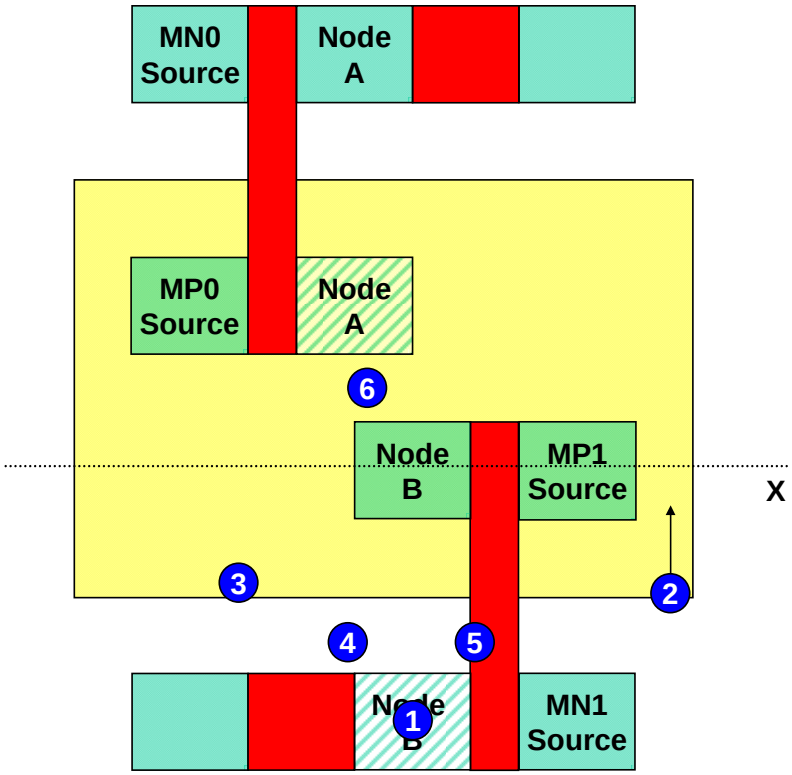

Figure 1. Top view of a 3-D TCAD model for a 90-nm SRAM cell. The pMOSFETs are located in the n-well (yellow region) in the center of the cell. The OFF drains shown with cross-hatch patterns. The numbered points represent different locations of simulated ion strikes.

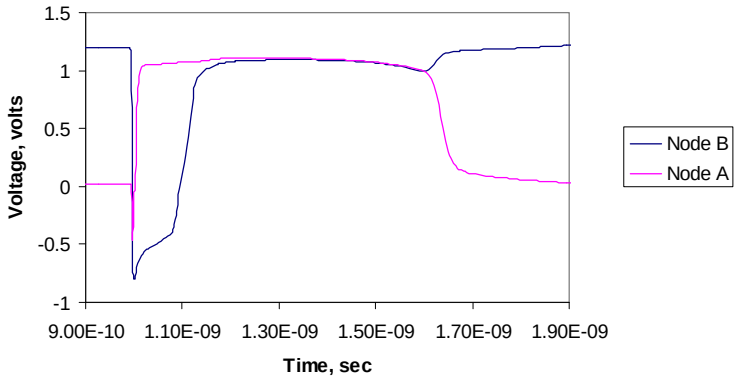

Figure 2. SRAM node voltages versus time for an ion strike (0.45 pC/μm) at the OFF nMOSFET drain (Point 1). The initial SRAM flip is due to DCC; metastability and a second SRAM flip are due to WCSI.

Figure 3 shows the relationship between conventional SEU, initiated by DCC, and SEU initiated by WCSI [3, 4, 5]. We propose that the upset region (described by the amount of charge required to produce an upset) can be divided into two sections, one initiated by DCC and one initiated by WCSI. These regions are separated by a crossover region where either upset mechanism may occur, depending on the strike location. In the DCC region [3], resulting from charge collection at an OFF transistor drain, the SRAM cell will upset if there is enough charge collected on a single sensitive node. For ion strikes near an ON transistor drain, the SRAM cell may be perturbed, but will not always upset. However, there is an ion shunt mechanism through an ON drain (logic high) to the substrate (ground) that can pull this node

low and upset the cell [8]. When there is enough charge deposited into the cell, the potential in the n-well containing the pMOSFETs collapses, initiating the WCSI mechanism.

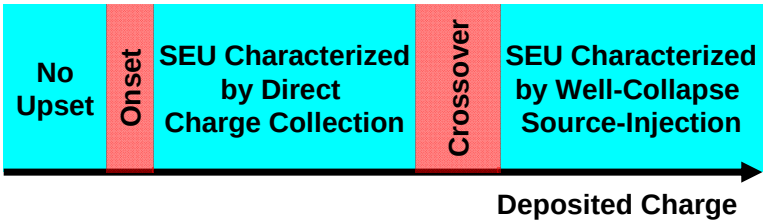

Figure 3. Proposed SRAM SEU modes as a function of deposited charge.

II. Well-Collapse Source-Injection

A. Supplying the Single Event Current

When charge is generated in the n-well, it needs to be removed through the contacts. There are two ways to remove the charge from the n-well: (1) through the well contacts and (2) through the p+-sources (Figure 4). Each path for removing the charge has a resistance from its respective contact to the ion strike location in the well. A significant part of the resistance occurs at the contacts where the current is constricted to flow through the openings in the shallow trench isolation.

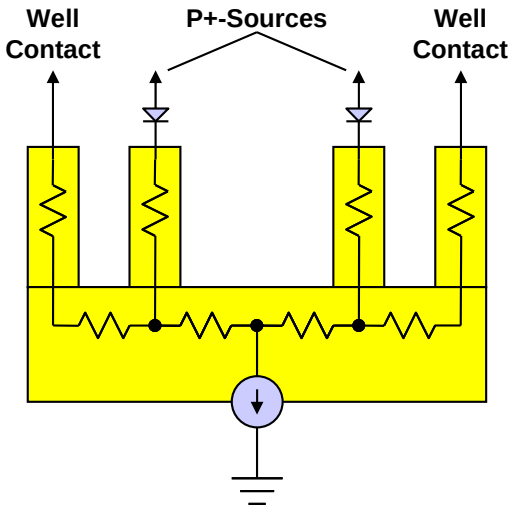

Figure 4. Well contacts and p+-sources remove the charge generated in the n-well by the single event.

The well contacts are limited in the amount of charge that they can remove from the well by the effective resistance between the strike and the contact. The amount of current that can flow through the contact is simply the well voltage divided by the parallel combination of all the resistances from the ion strike to the well contacts. When the ion-generated current approaches this limit, the well voltage near the strike location drops and approaches ground. This corresponds to an accumulation of electrons in the n-well. Since the rate of electron removal is limited primarily by the well contacts, the potential distribution is relatively uniform laterally along the well. When the well potential drops due to the accumulation of electrons, the source/well junctions become forward-biased. These forward-biased junctions become a second method to remove the ion-generated electrons from the n-well.

B. Carrier Injection and Resistivity Modulation

A TCAD simulation is presented to demonstrate the removal of the ion-generated electrons from the n-well. The ion strike is shown in Figure 1 at Point 2 and proceeds at an angle of 60 degrees from normal

to the surface in the direction shown. The simulated charge deposition is 0.12 pC/μm, corresponding to an LET of 12 MeV-cm^2/mg. A current versus time plot for the n-well contact and the two p+-sources is given in Figure 5. The ion strike is initiated at 1 ns. This figure demonstrates that the maximum current that can flow through the well contacts is about 0.2 mA. The figure also demonstrates that the p+-sources supply most of the single event current during the prompt charge collection.

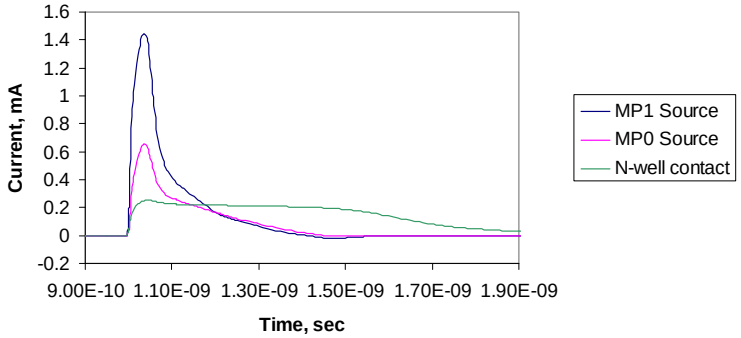

Figure 5. Supply current versus time for two p+-sources and the n-well contact from the TCAD simulation of an angled ion strike at Point 2.

When the source/body p-n junction is in forward-bias and removes electrons from the well, it also injects minority carriers (holes) from the source into the well. A consequence of the injection of holes from the source is the reduction of the vertical resistance for the p+-source to supply the photocurrent. In the example given in **Error! Reference source not found.**, the hole density in the well below the source is ~1.7×10^{18} cm^{-3} and the electron density is ~1.9×10^{18} cm^{-3}. These carrier densities are well above the doping level in the well, $N_D = 1.0 \times 10^{17}$ cm^{-3}. This increase in carriers reduces the resistivity of the well from 0.06 Ω-cm to 0.004 Ω-cm, or lowers the well resistance by over an order of magnitude [9, 10].

C. SRAM Cell Recovery

In the example shown in Figure 2, the WCSI mechanism begins when the voltage at Node B rises at about 1.1 ns. The well potential collapses, and both the p+-sources are forward-biased. The node voltages are then driven into a metastable state. This is the result of the parasitic p-n-p bipolar devices operating in forward-active mode. The drains of each pMOSFET are driven to $V_{CE(sat)}$, where the drain is the collector and the source is the emitter. The plot of node voltages is shown again in Figure 6 along with the two forward-biased source currents. The SRAM cell recovers when the forward-bias current can no longer sustain the bipolar forward-active mode.

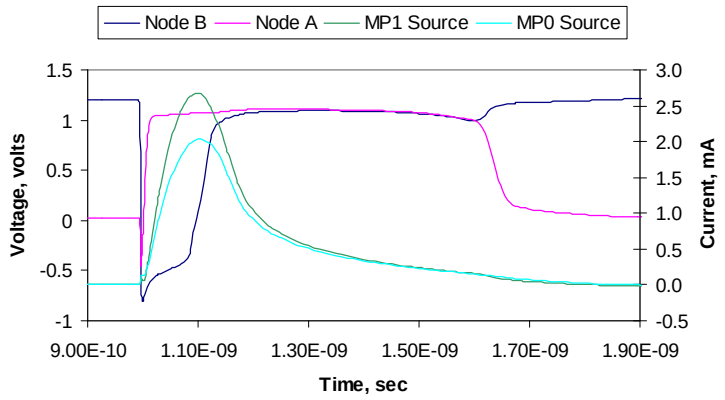

Figure 6. SRAM node voltages and forward-bias currents versus time for an ion strike (0.45 pC/μm) at the OFF nMOSFET drain (Point 1).

The recovery state of the SRAM cell following the metastable state is deterministic and depends on the source with the higher forward-bias current; the source with the higher forward-bias current will be the ON pMOSFET. This corresponds to the p+-source with the lower integrated resistive path to the ion strike location. In the plot in Figure 6, MP1 has the higher forward-bias current. Thus, the pMOSFET connected to Node B will be ON, and that node voltage will recover to the high state. Since this was the initial state of the SRAM cell, no upset will be observed, although the cell actually changed states twice: once from its original state to the upset state and then back again to its original state.

III. MCU Patterns with Respect to SEU Mechanism

DCC and WCSI SRAM SEU mechanisms can be distinguished in MCU patterns that result from single event testing. Figure 7 shows one column of an SRAM array with the n-well shown going down that column. It is assumed that BL is on the left and $\overline{\text{BL}}$ is on the right of the SRAM cells. It is further assumed that each cell is written logic low. The figure shows the locations of all of the OFF MOSFETs given these assumptions. If an ion strike is parallel to the well, the MCU patterns that result from DCC is a constant string of upsets. Figure 8 shows the same SRAM array and starting condition. Assuming that an SEU characterized by WCSI affects all of the SRAM cells in the array and the center of the charge collection is in cell #6, the cells will recover dictated by which p+-source has the least resistive path to the charge collection region. SRAM cells #1-#5 will recover with the ON drain at the bottom of the cell (i.e., the OFF drain at the top of the cell). SRAM cell #6 will recover in one or the other state depending on the specific location of the charge collection region. SRAM cell #7-#12 will recover with the ON drains at the top of the cell. This is shown on the right of Figure 8. The MCU pattern due to this SEU mechanism will be alternating as shown in Figure 9. Thus, the observed patterns from single event testing can indicate the type of SRAM SEU mechanism.

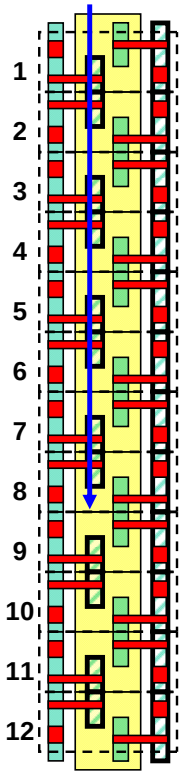

Figure 7. Ion strike parallel to n-well in an SRAM array written with a constant pattern. The OFF drains are shown with cross-hatch patterns.

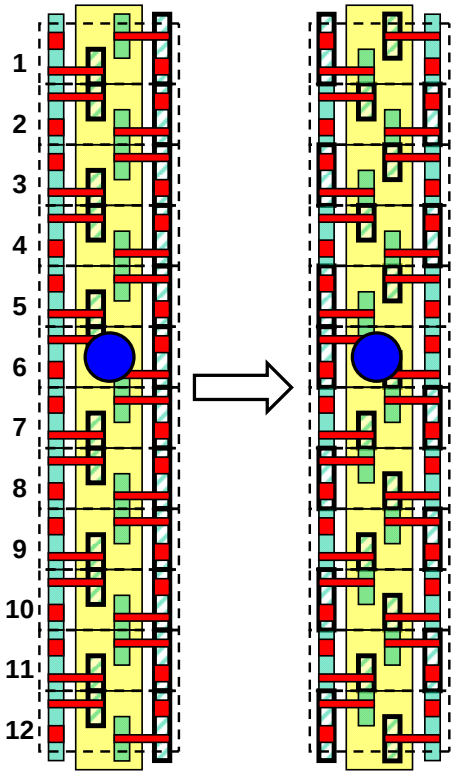

Figure 8. MCU pattern prediction due to the WCSI mechanism (shown on the right). The SRAM array is initialized with a constant input pattern (shown on the left).

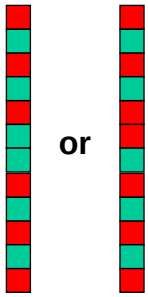

Figure 9. MCU patterns due to the WCSI mechanism. The SRAM array was written with a constant input pattern. Red indicates an observed upset and green indicates no observed upset.

IV. SRAM Single Event Test Results

In the evaluation of a 65-nm SRAM array with a SRAM cell layout similar to the one shown in Figure 1, MCU patterns were observed indicating a combination of the DCC and WCSI SEU modes. The testing was performed the Texas A & M University Cyclotron with ions of Ne (LET = 2.8 MeV-cm^2/mg), Ar (LET = 8.6 MeV-cm^2/mg), and Kr (LET = 28.9 MeV-cm^2/mg). The ions were directed to strike the SRAM array at an angle of 78.5° parallel to the n-well. The SRAM was written with a constant pattern down each well. For Ne, 540 MCU patterns were observed and 30 of them indicated the combination of the DCC and WCSI SEU modes. For Ar, 415 MCU patterns were observed and 75 of them were indicated of both SEU modes. For Kr, 212 MCU patterns were observed and 183 of them indicated both SEU modes. Example of MCU patterns from Kr are shown in Figure 10. These MCU patterns contain elements from both DCC and WCSI and demonstrate that WCSI is occurring in these single event tests.

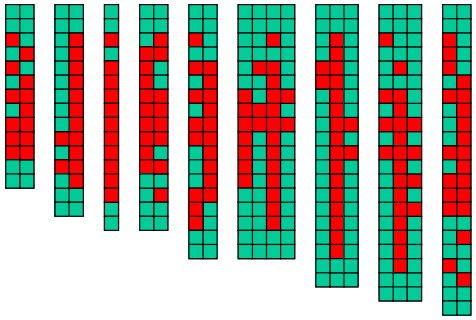

Figure 10. Observed MCU patterns from testing of a 65-nm SRAM array with Kr (LET = 28.9 MeV-cm^2/mg), angled at 78.5° from normal, parallel to the n-well. The MCU patterns show a constant string of upsets where the ion strike occurred with surrounding alternating upsets where WCSI was observed.

V. Conclusion

The study of SRAM SEU mechanisms in TCAD modeling and simulation led to the prediction of the cell recovery from the WCSI mechanism. This mechanism was encountered when charge collection in the well/substrate p-n junction exceeds the amount that can be supplied by the well and/or substrate contacts. The SRAM cell recovery from WCSI was defined by which p+-source had the lowest resistive path to the well/substrate charge collection. This knowledge was used to predict potential observed MCU patterns based on the mechanism. Data from single event testing was shown to verify the pattern dependence.

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