Radiation Test Challenges for Scaled Commercial Memories

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Abstract: *As sub-100nm CMOS technologies gather interest, the radiation effects performance of these technologies provide a significant challenge. In this talk, we shall discuss the radiation testing challenges as related to commercial memory devices. The focus will be on complex test and failure modes emerging in state-of-the-art Flash non-volatile memories (NVMs) and synchronous dynamic random access memories (SDRAMs), which are volatile. Due to their very high bit density, these device types are highly desirable for use in the natural space environment.*

In this presentation, we shall discuss these devices with emphasis on considerations for test and qualification methods required.

Keywords: CMOS; radiation effects; commercial memories.

Introduction

It is a given that there has been and continues to be tremendous changes in both the commercial and radiation-hardened foundry technologies and approaches to semiconductors [1]. A short list of example technology considerations may include:

- Scaling of feature size,
- Thinning of oxides,
- Changes in materials, and,
- Novel gate structures.

These changes alone aren't the only new considerations when one discusses radiation performance and ground-based testing. Areas include, but are far from limited to device performance (operating speeds, gate density, bandwidth, etc.), complex packaging (ex., flip chip ball grid array – fcbga), and reduced power supply voltages and commensurate reduced noise margins. Finally, one must include thoughts on application-specific device configurations, embedded software and processing, and the overall complexity related to systems on a chip (SOAC) such as a state-of-the-art (SOTA) field programmable gate array (FPGA).

In this talk, we shall consider these changes above as they pertain to radiation effects testing of modern commercial memory devices in the natural space environment. In particular, the emphasis will be on heavy ion single event effects (SEE) testing with lesser discussion on proton SEE and traditional total ionizing dose (TID) test considerations. The environments specific to the military radiation environment such as prompt dose and neutron are considered out-of-scope for this presentation.

The approach will be to discuss generally the existing test methods for space radiation effects testing in the natural environment. This will be followed by several examples of specific devices highlighting some additional challenges in preparing for testing, test performance, and data analysis. This should be viewed as a snapshot of issues and not a comprehensive detailed analysis. We shall conclude with some thoughts on implications to cost and risk reduction based on some of these challenges.

Existing Test Methods (for Natural Space)

The prime two accredited SEE test methods were developed circa mid 1990's by the Joint Electron Device Engineering Council (JEDEC) [2] and American Society for Testing and Materials (ASTM) [3] communities. Both of these documents, in the authors' opinions, are excellent bases for practical SEE testing especially for simpler devices when one considers test basics. However, as noted, technology has changed considerably over the past decade. A short list of SEE-related phenomena that have been discovered since then include:

- Angular effects in SOI technologies,
- Role of nuclear reactions from heavy ion particle interactions,
- Role of charge sharing in multi-node effects,
- Role of single event transients (SETs) and commensurate speed-related issues in both analog and digital circuits,
- Ion penetration and range issues in power and packaged components,
- Approaches to die access, and
- Impact of application and reconfigurable approaches to SEE performance.

In a like manner, the commensurate ASTM [4] and MIL-STD-883 Method 1019.7 [5] methods for TID tests provide a solid footing for test approaches. However, practical

considerations still exist when considering device complexity (fault coverage in a billion transistor processor, for example), exposure dose rates, etc…

Commercial Devices and Selected Related Radiation Testing Challenges

Because of the increasing device complexity that has been gained by scaling of technology in terms of gate count, application speed, circuit and control complexity, and so forth, different device types may face differing issues when being characterized for their radiation tolerance. Again, issues include circuit complexity, number of cells, frequency, modes of operation, data analysis, secondary particles, angular effects, and more. Two test examples follow illustrating some of these concerns for commercial memories.

Synchronous Dynamic Random Access Memories (SDRAMs) – A microcontroller with memory:

Changes for Radiation Commercial Volatile Memories: A Ten Year Perspective

In the mid-90s, the use of commercial Static Random Access Memories (SRAMS) was common-place in space craft systems building solid-state recorders (SSRs). However as time has progressed, the SRAM has been replaced by the Dynamic Random Access Memory (DRAM) and then by SDRAM. Table 1 illustrates some of the salient device differences between the older SRAMs and the newer SDRAMS.

Feature	SRAM	SDRAM
Feature size	1 um	90 nm
Memory size	4 Mb	1 Gb
Bus speed	< 50 MHz	> 500 GHz
Package	Ceramic DIP or LCC	TSOP or FBGA
Power supply voltage	3.3 or 5V	1.8 V (with possible internal regulation down to 1.2V)
Other		Built-in microcontroller-like functions (>60 modes of operation)

Table 1: 90's SRAM versus recent SDRAM comparison

Some of the considerations for SEE testing include, but are far from limited to:

Size of memory

- Drives complexity on tester side for amount of storage, real time processing, and length of test runs and data processing

Speed

- Difficult to test at high-speeds reliably
- Need low-noise and high-speed test fixture
- Classic bit flips (memory cell) extended to include transient propagation (used to be too slow a device to respond)
- Thermal and mechanical issues (testing in air/vacuum)

Packaging

- Modern devices present problems for reliable test board fixture, die access (heavy ion tests) requiring expensive facility usage or device repackaging/thinning
- Difficulty in high-temp testing (worst-case)

Hidden registers and modes

- Functional interrupts driving "anomalous data"
- Not just errors to memory cells!
- Microcontroller

Challenge: Preparing a device for SEE testing:

Commercial SDRAMs typically are packaged in either thin small outline package (TSOP) or plastic BGA package. From the SEE test perspective, neither are ideal. The true challenge is ensuring that accelerated energetic particle has sufficient penetration range to impinge on the sensitive silicon volume. The majority of accessible SEE heavy ion test facilities require much, if not all, of the packaging material (on the side in which the ion impinges) needs to be removed. This is non-trivial. Note that the space environment energies for the heavy ions do not have this restricted penetration issue.

Take TSOPs in particular. Often there is a metal lead frame on top side of the package. One can remove the plastic (acid etch, mechanical grinding, etc…) but there is usually a lead frame that impedes the irradiation from the incident direction. Removal of the lead frame has a very low success rate due to stress on the die. The lead frame does not block the entire die, so a partial test can occur with *estimated* number of memory cells being irradiated. To the first order, post-processing of the gathered data via a statistical analysis can provide an approximate percentage of die tested. However, certain critical circuits may well be shielded and the test data may miss failure modes that are hidden.

Plastic FCBGA devices have their own challenges. The SOTA die utilize 90nm feature size and below. The die and the entire package are thin mechanically (but not from the ion penetration perspective). In order to shore up the mechanical strength prior to de-encapsulation, mounting

the devices on a printed wiring board (PWB) prior to de-processing is often performed. However, even so, a low yield is expected after de-processing is complete. The two pictures in Figure1 show two such die failures. The first picture illustrates a cracked die while the second shows a "potato chip" like result. Clearly, this presents a challenge to test organizations.

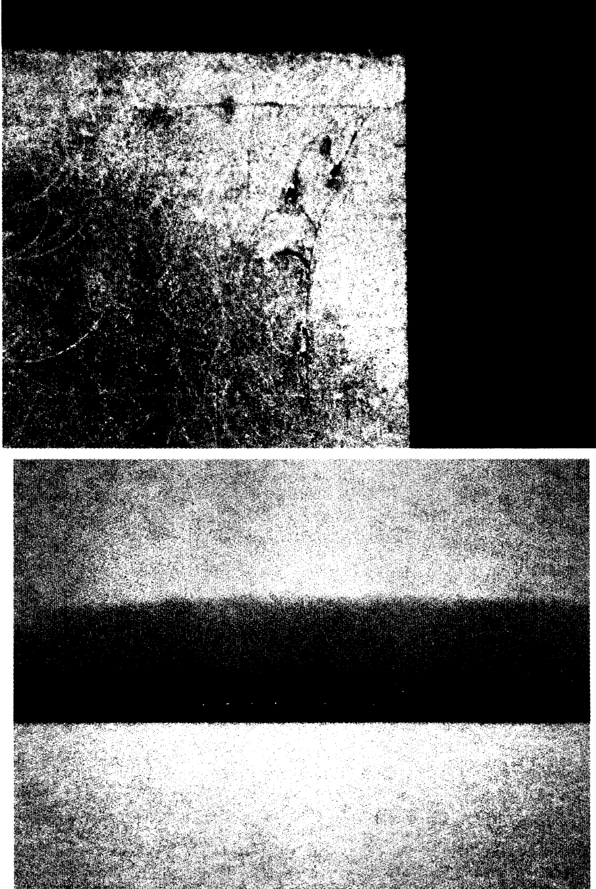


Figure 1. De-processing failure examples of FBGA SDRAM *courtesy of Radiation Assured Devices*

Die repackaging is also a consideration. However, three key thoughts should be considered. First is the low success ratio for removing die from packages. This drives a fairly large sample size be used in order to potentially get a handful of samples for test. The second item is pragmatic: is the vendor willing to sell die (in small commercial volumes) to someone considering their use for space? Not only is there the business consideration for the manufacturer (very small volume request from what is typically a high volume product with constraints such as singe lot, etc.), but also the fear (real or perceived) of International Traffic in Arms (ITAR) restrictions related to space products.

Challenge: At-speed testing:

State-of-the-art (SOTA) SDRAMs use internal frequency multiplication to take an external clock and operate internally at a higher speed. For example, dual data rate (DDR) takes an input frequency and doubles it internally. The slowest of the commercial SOTA SDRAMs will utilize a 100-133 MHz input frequency and double it to operate at 200-266 MHz. The current high-end SDRAMs have doubled (or quadrupled) frequencies up to 800 MHz or more. They also have *minimum* operating frequencies as well as discrete operating points much stricter than the "old-school" devices. This high-speed drives several factors when performing SEE testing. These include:

- Short and balanced traces between the SDRAM (i.e., device under test – DUT) and the test set (note: many testers are currently using FPGA-based motherboards with DUTs on a daughtercard),
- High-speed (>100 MHz to 500 MHz) interface operation between DUT and test set,
- Sufficient data storage to buffer SEE data real-time to allow discrimination between single bit, multiple bit, functional interrupts, single event latchup (SEL), and any other potential event,
- Real-time event determination (i.e., SEL versus functional interrupt) and recovery (for example, power cycle versus refresh of data versus device reset pulse), and,
- Flexibility on test data patterns, control set up, power supply voltages, SEL trip current levels, and so forth.

Given the constraints that testing may occur in a vacuum, local data collection in the vacuum chamber, related thermal control and cabling issues, and remote operation and monitoring concerns must be addressed.

Challenge: Completeness of "generic" datasets and test planning:

A sample 1 Gb SDRAM has on the order of 68 modes of operation. If one were to test each of these modes (and yes, there are documented cases of mode dependence on results since the 1980's) with as a minimum several data patterns (looking at synergistic pattern effects, burn-in effects, state change effects, etc...), clock rates (speed issues), power supply voltage (nominal and worst case), as well as considering temperature (nominal and worst case), one could easily spend an extreme amount of time at an accelerator doing nothing more than performing tests and collecting data. At an average hourly facility rate of $750/hr and adding in labor, travel, and data analysis (HOW many GB of data collected???), the cost would well exceed $>>M for a single device type just for data collection and analysis! Clearly this is not feasible (nor truly desirable). In detail, a test matrix for full testing might look like Table 2.

Sample Single Event Effect Test Matrix
full generic testing

Amount	Item
3	Number of Samples
68	Modes of Operation
4	Test Patterns
3	Frequencies of Operation
3	Power Supply Voltages
3	Ions
3	Hours per Ion per Test Matrix Point

Table 2: Full SEE Test Matrix

When one does the math, this ends up being ~ 7.5 years at the accelerator non-stop! And for those paying attention, this matrix did not include *temperature* as a variable (up to a factor two additional time requirement).

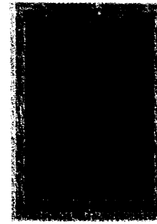
This leaves several clear thoughts to consider. These include:

- Be wary or archival data and it's applicability to a specific device usage,
- Application-specific "qualification" tests should be considered, and
- A downscaling of test matrix to provide representative or "worst-case" results. This may not always be feasible.

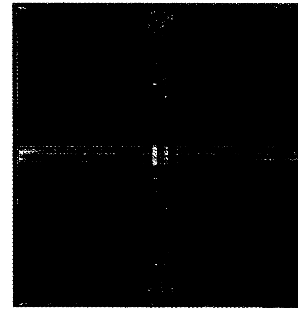
Even with a down-scaled test plan, test costs and schedules have increased commensurate by a factor of three or more over the past decade. Appendix A illustrates a representative comparative spreadsheet for SEE test costing. Please note that these are relative and optimistic numbers with many assumptions.

Challenge: The statistical nature of SEE tests:

The accepted generic SEE test methods such as JEDEC require fluence levels per test run of 1E7 ions/cm^2. When these methods were being developed, commercial devices maxed out at around 256kb per die. With 1E7 ions hitting around 2.5E5 cells, an overtest of ~a factor of 40 occurs. Current state-of-the-art SDRAMs contain ~1E9 cells. Die size, while increased, is still less than 1 cm^2. Hence, approximately 1% of the cells will be struck directly during a heavy ion exposure to 1E7. Thus, the converse occurs if testing by standard, an undertest of device cells by a factor of 100! This provides a less than conservative approach to radiation assurance. Figure 2 illustrates SOTA memory die from ten years ago and today.



32k x 8 SRAM circa early 1990's
Feature size is 0.8 to 1.25 μm



1 Gb SDRAM circa 2006
Feature size is 90nm

Figure 2. SOTA memory die from ten years ago and today

Challenge: Test set development:

In the "old days", test fixtures were a DIP socket on a wirewrap board. With high-speed devices (333 MHx external clock), and low I/O voltages (1.8V or less), devices must be interrogated locally.

Using the power of reprogrammable FPGAs is one way to accomplish this. Reprogramming IO signals by changing design via VHDL or such can aid in debugging and allows flexibility

Boards themselves must take into account signal integrity, signal skew and timing, impedance matching, embedding passives, multi-layer power and ground, power distribution, SEL protection, and more.

Considerations for angular tests, high temp, cooling, etc. complicate further. Figure 3 shows one such FPGA approach as developed by NASA.

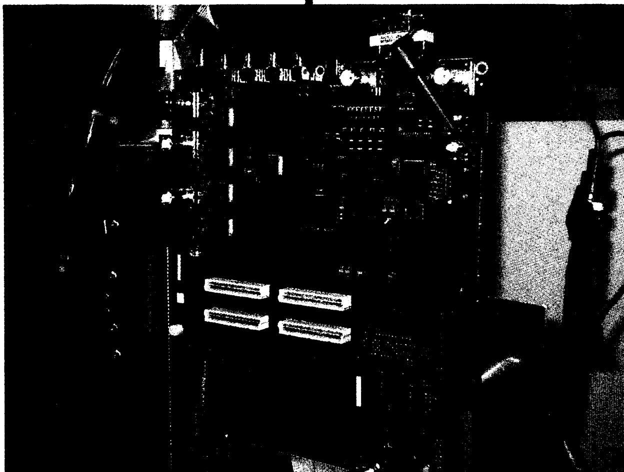


Figure 3. Sample SDRAM Test Set

Challenge: Real-time data gathering and data anlysis:

With the SEE world much more complex than a simple single bit errors, test sets need to be able to capture appropriate information for the plethora of possible SEE error conditions that can occur. A sampling of related test performance concerns beyond the usual error-counting and current monitoring might include:

- Multi-bit upsets (MBUs) and the need to determine physical events from a single particle driving time-tag resolution and bitmap knowledge, and,
- Single event function interrupts (SEFI) and how they manifest themselves and means of recovering from them (and related implication on test statistics such as beam fluence).

The key is to understand enough of the data that is being gathered real-time at the test site to make intelligent decisions for the next test run(s). A representative SEE test run and data capture is shown in Figure 4.

The majority of the data analysis takes place either when the beam is not on the device or after the testing is "completed" (and the hope that a return to test that part is not needed). Automated data processing is desired, however the data complexity may require manual intervention when an unusual event signature is noted. A list of SEE-related modes for analysis might include:

Single bit errors

Multi-bit errors

- Physical vs. logical
- Timetag requirement for verifying single particle strike

Block errors

- Columns, rows, banks,

SEFIs

- Signature and recovery modes. We refer you to the excellent example cited by Benedetto, et al in Figure 5. [6]

Hard errors

SEL

Other (and this may end up falling into one of the other categories when understood).

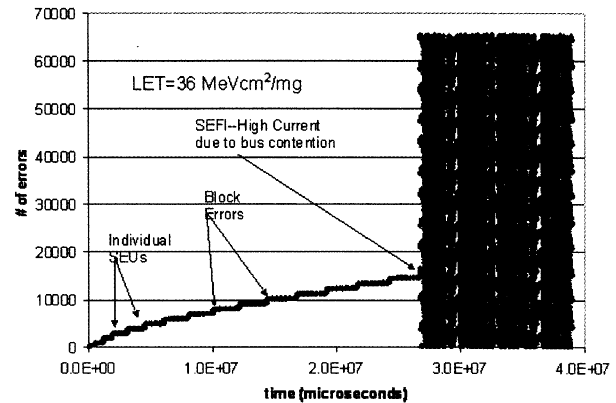


Figure 4. Sample SDRAM SEE Test Run

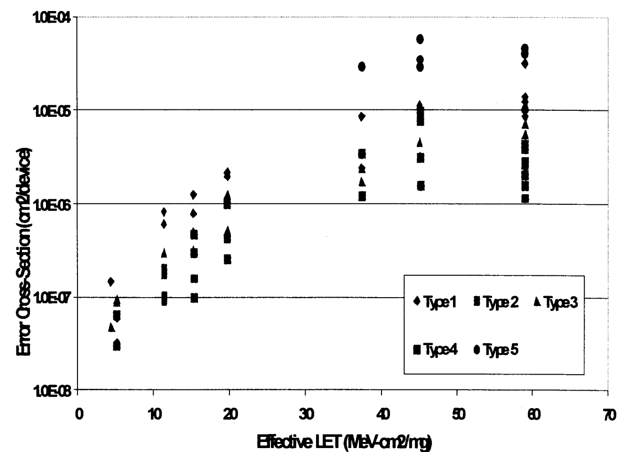


Figure 5. SDRAM SEFI Modes, after Benedetto, et al

FLASH Memories – Brief considerations for TID testing:

TID testing on any device (especially commercial memories) has, of course, some additional concerns that

need to be taken into account for. A random list might include:

- Bias boards, cabling, parametric measurements, etc, BUT,
    - Higher speed, low voltage I/O devices can be problematic
    - Sockets for BGAs can be "troublesome"
    - Repeatability can be a problem with high-speed connectors
- More complex data patterns needed to test to find weak cells or other
- Complete test matrix for generic test would force time constraints much longer than allowed by 1019.7 for time between exposures, and,
- Again, application-specific issues.

Traditionally commercial FLASH memories have had low TID failure levels mostly due to charge pump or other peripheral circuitry more so than the actual storage cells. With deep sub-micron CMOS regularly exceeding 100 krads-Si in tolerance, investigation into more complex structures that may fail at much lower TID levels is required. Numerous groups have investigated FLASH TID failures in the past and have utilized them for space often limiting what mode the device would operate in. For example, if the write mode failed at low TID level and the read at a higher, the device might be used as a programmable read-only memory (PROM). The complexity of the modern FLASH accentuates the need for application-specific testing.

In the example shown in Figure 6, this type of mode dependence showed a clear demarcation of failure levels. [7]

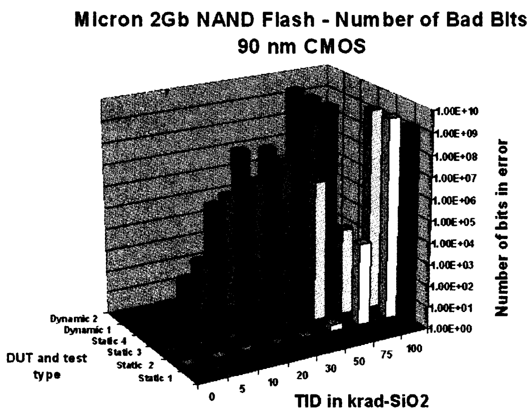


Figure 6. Modern TID Mode Dependence, after Oldham, et al

Discussion

The bottom line challenge to most programs that want to use complex devices is cost and schedule: cost of the test effort and the time it takes to get an answer (good or bad – remember not all devices will necessarily meet mission requirements). It has been estimated that a moderately complex new device type takes on the order of \$1.5 – 3M to perform a full suite of qualification (radiation and reliability) tests. This does not include the most complex SOACs that can easily double or triple this number.

If performance (speed, power, density, etc…) requirements drive this usage such that radiation-hardened options are not feasible (or mission can't perform its prime goals without), programs will need to invest in test efforts focusing its resources for the most risk reducing tests (and/or possibly risk acceptance). This is t food for thought for this paper: the trade space between full test conservatism and risk or risk acceptance. From the NASA perspective, each program will likely view this in a differing manner on what is or isn't a reasonable risk to assume.

One can use some of the lessons learned presented in their test planning, but, nothing is static: evolving technologies require continuous vigilance in test approaches. With coming generations of devices increasing in complexity, looking beyond an existing test standard may be required for adequately determining risk.

References

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6. Benedetto, et al, IEEE TNS Dec 06
7. Oldham, et al IEEE TNS Dec 06

Appendix A: Representative SEE Cost Breakdown

And Drives Cost and Schedule!

1996 SEE Test of a 4M SRAM

Description	Man-weeks or units	Cost in $	Total	Note
Heavy Ion at BNL SEUTF				
Test plan	0.20	$4,000.00	$800.00	Includes eng, rad, other to define what needs to go into test set with project.
Device procurements	10.00	$50.00	$500.00	
Misc parts	1.00	$250.00	$250.00	Sockets, connectors, etc...
Device delidding	0.05	$3,500.00	$175.00	
Test board design - electrical and layout	0.40	$4,000.00	$1,600.00	
Board fab and population	1.00	$3,500.00	$3,500.00	In-house board build
Board/tester debug	0.50	$4,000.00	$2,000.00	
Rad expert (test oversight and plan)	0.40	$5,000.00	$2,000.00	
Heavy ion test performance - contractor	2.00	$1,500.00	$3,000.00	
BNL Beam	6.00	$700.00	$4,200.00	Simple data: bit flips, latchup
Data analysis	1.00	$3,500.00	$3,500.00	
Test report (eng, rad expert, rad lead)	0.50	$4,000.00	$2,000.00	
			Total:	$23,525.00

2006 SEE Test of SDRAM

Description	Man-weeks or units	Cost in $	Total	Note
Heavy Ion at TAMU				
Test plan	1.00	$4,000.00	$4,000.00	Includes eng, rad, other to define what needs to go into test set with project.
Device procurements	10.00	$75.00	$750.00	
Misc parts	1.00	$1,000.00	$1,000.00	Higher speed drives cost
Device thinning and package processing	10.00	$500.00	$5,000.00	Assumes FBGA package; If this does not work, more expensive test facility like NSCL needed: >$100K delta
Daughterboard Board design - electrical	0.80	$4,000.00	$3,200.00	
Daughterboard Board design - PCB	0.80	$3,500.00	$2,800.00	
Test Boards	10.00	$500.00	$5,000.00	
Board population	0.40	$3,500.00	$1,400.00	
Board/tester debug	0.50	$4,000.00	$2,000.00	
Tester VHDL development	4.00	$4,000.00	$16,000.00	
Technician	1.00	$3,500.00	$3,500.00	
Rad expert (test oversight and plan)	0.60	$5,000.00	$3,000.00	
Heavy ion test performance - contractor	3.00	$2,000.00	$6,000.00	
TAMU	16.00	$750.00	$12,000.00	2X time required: more data, more error types, more complex results; partial test
Data analysis	3.00	$3,500.00	$10,500.00	
Test report (eng, rad expert, rad lead)	1.00	$4,000.00	$4,000.00	
			Total in $	$80,150.00

1996 vs 2006 a >3X Cost Delta

Other test costs (radiation and reliability) have increased commensurately with ~3X schedule increase as well!

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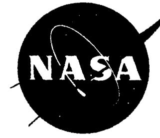

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To be presented by Kenneth LaBel at 9th European Conference Radiation and Its Effects on Components and Systems (RADECS07) Short Course Session, Monday, September 10-14, 2007 - Deauville, France.

Unclassified

Outline of Presentation

- Introduction – a Changing Memory and Test World
- Example: Single Event Effect (SEE) Testing of SDRAMs
  - Device preparation
  - Test set
  - Test planning
  - Test performance
  - Gathering data and statistics
  - Post-test analysis
- Total Ionizing Dose (TID)
  - Example: Flash memories
- Considerations

Disclaimer:
This is not a comprehensive talk, but about considerations and thought processes

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The Changing World of Radiation Testing of Memories – A Ten-Year Perspective

Category	1997	2007	Implication
Device	SRAM	SDRAM DDR2	More complex architecture
Feature Size	>=1.0 um	<=90nm	Miniscule target
Density	4 Mb	1 Gb	Large tester data storage; Difficult data analysis
Speed	<50 MHz	>1 GHz	Drives challenges for at-speed test and data collection; transient propagation; thermal/mechanical challenges
Package	DIP or LCC	TSOP or FBGA	Difficult access for heavy ion and high-temperature testing
Notes	Mostly ceramic, simple operating modes	Plastic, flip-chip, many operating modes	Complex signatures for error and data analysis; "Unknown" features

Commercial memory testing is a lot more complex than in the old days!

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1996 vs 2006 a >3X Cost Delta

Optimistic

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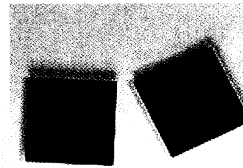
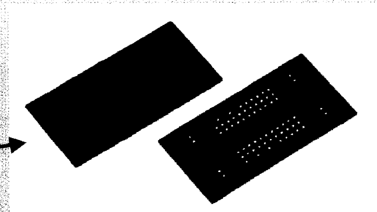
Commercial SDRAM Overview – Sample Device

- 1 Gb of active cells
  - 8 banks of memory
- Dual Data Rate 2 (DDR2) operation
  - 333 MHz clock
    - 667 MHz internal
      - Newest devices are 1066 MHz
- Power conversion/regulation (1.8V Vdd, memory cells may be at different level)
- 90nm feature size with bit spacing between logical bits in a nibble
- 68 modes of operation
  - Small internal microcontroller
- Flipchip Ball Grid Array (FBGA) package
  - Plastic encapsulated

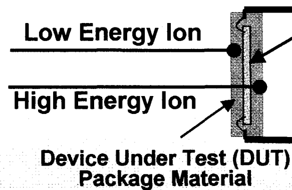


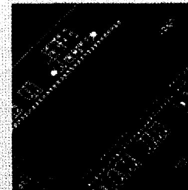


Unclassified

Preparing the Device - Constraints

- Due to constraints of terrestrial-based heavy ion irradiation facilities, devices must be prepared to allow ion(s) of choice to reach the sensitive circuits within the device
- Commercially packaged plastic encapsulated devices must be de-processed sufficiently (thinned, portions removed, etc...)
- Risks associated





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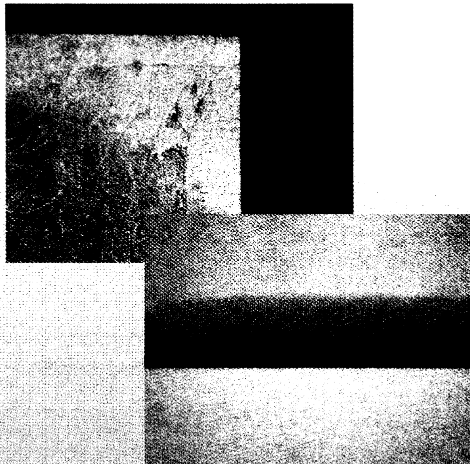
Preparing the SDRAM

- SDRAMs use thin small outline package (TSOP) or plastic FBGA. Two options exist for device preparation:
  - Deprocess (acid etch, grind, etc), or,
  - Repackage.
- TSOPs can be problematic
  - Plastic can be removed, but metal lead frame still shadows die
- FBGAs require die ion access through die backside (top of device given flip chip configuration)
  - Thin devices are fragile
  - Device integrity and yield of de-processing among challenges
  - Removing packaging material removes stress relief
  - Pre-mounting devices on PWBs may aid stability in deprocessing
- Repackaging is challenging
  - Die availability
  - Cost and schedule
  - First pass success



Two examples of deprocessing yield failures
-Cracks (top) and Waffling (bottom)
-Photos courtesy of Radiation Assured Devices

To be presented by Kenneth LaBel at 9th European Conference Radiation and Its Effects on Components and Systems (RADECS07) Short Course Session, Monday, September 10-14, 2007 - Deauville, France. 7

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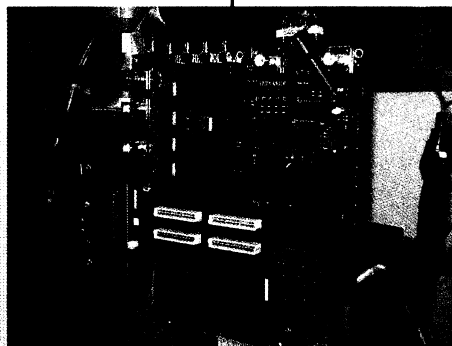
SDRAM Test Set Preparation

- In the "old days", test fixtures were a DIP socket on a wirewrap board
- With high-speed devices (333 MHz external clock), and low I/O voltages (1.8V or less), device must be interrogated locally.
  - Using the power of reprogrammable FPGAs is one way to accomplish this
    - Reprogramming IO signals by changing design via VHDL or such can aid in debugging and allows flexibility
  - Boards must take into account signal integrity, signal skew and timing, impedance matching, embedding passives, multi-layer power and ground, power distribution, SEL protection,and more.
  - Considerations for angular tests, high temp, cooling, etc. complicate further

FPGA-based motherboard



SDRAM mounted on a daughtercard

It's not a TTL-world anymore!

To be presented by Kenneth LaBel at 9th European Conference Radiation and Its Effects on Components and Systems (RADECS07) Short Course Session, Monday, September 10-14, 2007 - Deauville, France. 8

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Can we test anything completely?

SEE Test Matrix

3	Number of Samples
68	Modes of Operation
4	Test Patterns
3	Frequencies of Operation
3	Power Supply Voltages
3	Ions
3	Hours per Ion per Test Matrix Point

66096 Hours
2754 Days
7.54 Years

and this didn't include temperature variations!!!

Test planning requires much more thought in the modern age as does understanding of data collected (be wary of databases).

Only so much can be done in a 12 hour beam run – <u>application-oriented</u>

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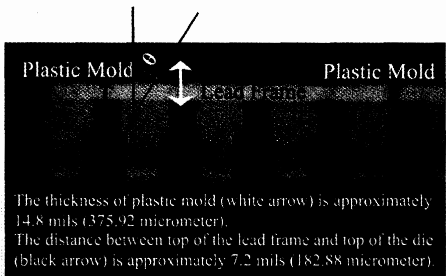
Sample Test Performance Issues

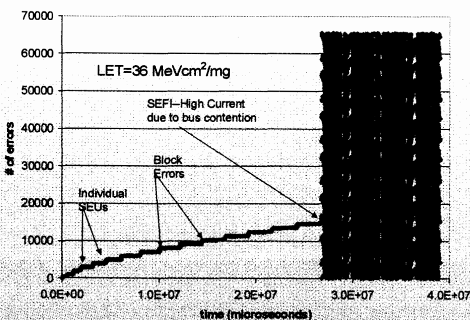


X-Ray Photo of a TSOP DUT

Determining effective LET as a function of angle requires correcting for the energy lost by the ion as it traverses overburden to the sensitive volume, as well the usual 1/cosθ dependence which may or may not apply.

Leadframe of the TSOP complicates this further.

Packaging



Real-time error counts during a test run:
Different types of errors have different signatures, Complicating data collection, test decision making, and analysis

Data

Unclassified

SDRAMs and Statistical Data Gathering

- **Current SEE Test Standards were based on large feature sizes and relatively few cells**
  - **1E5 bits versus the 1E9 bits of today.**
- **Existing test methods typically use 1E7 ions/cm2 as test run particle fluencesor alternately to 100 or so events.**
  - **With the old devices, probabilities favored that every cell was hit (ie., an overtest of 100x) or that statistical coverage wasn't bad.**
  - **In the new devices, ~ 1% of the cells are hit during a test run at max fluence. Alternately, 100 or even 1000 events likely covers only a small percentage of available cells.**
  - ***This lack of conservativeness provides issues for statistics, small probability events, SEFI coverage, weak cells, etc...***

32k x 8 SRAM circa early 1990's
Feature size is 0.8 to 1.25 um

1 Gb SDRAM circa 2006
Feature size is 90nm

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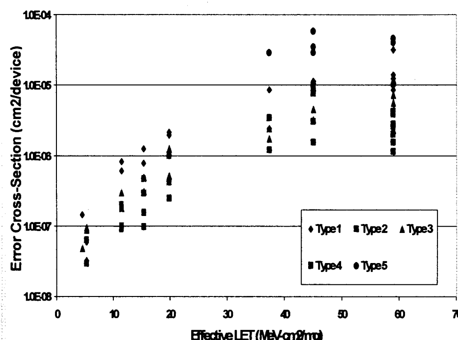
Analyzing SDRAM SEE Data

- **Complexity and density of SDRAMs drives requiring automated data processing (if we know the event signatures)**
  - **Single bit errors**
  - **Multi-bit errors**
    - **Physical vs. logical**
    - **Timetag requirement for verifying single particle strike**
  - **Block errors**
    - **Columns, rows, banks,**
  - **SEFIs**
    - **Signature and recovery modes**
  - **Hard errors**
  - **SEL**
  - **Other**
- **1000 errors x 100 runs equals 100000 data points to analyze! SEFIs!**



Sensitivity of a 512 Mb SDRAM to multiple SEFI modes
After Benedetto, 2006

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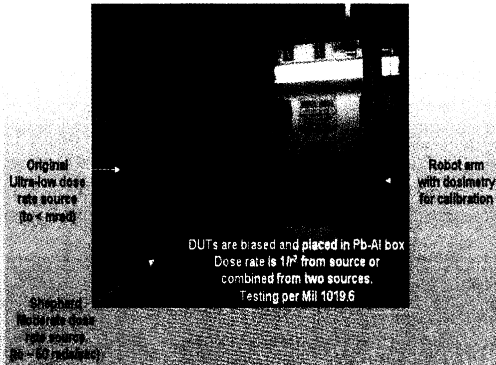
Challenges Go Beyond SEE

- While many of the concerns for SEE apply to total ionizing dose (TID), there are other considerations
  - Bias boards, cabling, parametric measurements, etc, BUT,
  - Higher speed, low voltage I/O devices can be problematic
    - Sockets for BGAs can be "troublesome"
    - Repeatability can be a problem with high-speed connectors
    - More complex patterns needed to test
  - Complete test matrix for generic test would force time constraints >> than allowed by 1019.7
    - Drives application-specific



NASA/GSFC's Radiation Effects Facility

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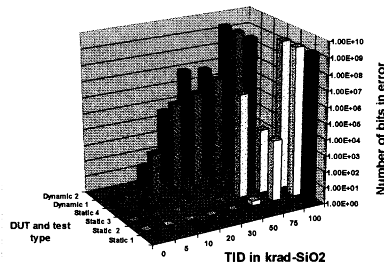
Challenges Go Beyond SEE

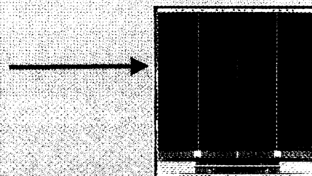
Example:
2006 Commercial Flash TID Evaluation

- Failures noted in dynamic mode at << cumulative dose levels than static mode.
- All devices failed at < 100 krads(Si)
  - Though this device fared better than most Flash, 90nm CMOS is expected, in general, to be >100 krads(Si)
    - It's about more than the base material (circuits!)
  - Note: Newer Samsung 4 Gb device passed 150 krads(Si) tolerance level

Micron 2Gb NAND Flash - Number of Bad Bits
90 nm CMOS



After Oldham, 2006



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Considerations

- Technology changes in memories may engender challenges
  - Impact of new materials and manufacturing methods on radiation response and modeling
  - Increasing difficulty in die accessibility
  - Increasing operating speeds and operating modes
  - More hidden "features" and limited testability
  - Multi-level storage cells (Flash, for example)
- The example issues presented in this talk are just that: examples
  - One can use some of the lessons learned in their test planning, but,
    - Nothing is static: evolving technologies require continuous vigilance in test approaches
- Examples requiring thought
  - Samsung has 8 Gb multi-level Flash available and Toshiba has announced 16 Gb devices
  - DDR3 and beyond clock structures in SDRAMs