Indium Hybridization of Large Format TES Bolometer Arrays to Readout Multiplexers for Far-Infrared Astronomy

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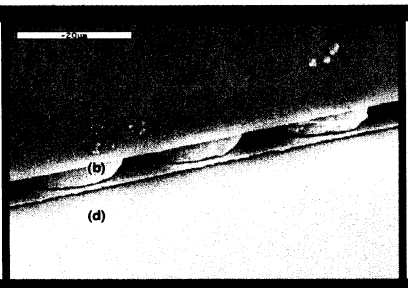
OVERVIEW

- We are developing a key technology to enable the next generation of detectors
  - Hybridization of Large Format Arrays
    - Indium bonded detector arrays containing 32x40 elements
    - Conforms to the NIST multiplexer readout architecture
      - 1135 micron pitch
  - Fabricated and hybridized mechanical models
    - Detector chips are bonded after being fully back-etched
    - Mechanical support consists of 30 micron walls between elements
  - Demonstrated electrical continuity for each element
- Goal to hybridize fully functional array of TES detectors to NIST readout



(a) DETECTOR WALL
(b) INDIUM
(c) UNDER-BUMP-METAL
(d) SUBSTRATE

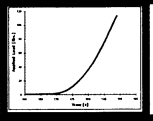
INDIUM BOND QUALITY

Indium bumps were produced by evaporation using a thick photo-resist lift-off mask. Bonding was done with a Suss FC150 Flip Chip Bonder. The strength of the bond has been characterized by tensile pull-testing small test chips that simulate the large number of bumps needed.

- Failure occurs at about 115 pounds of force
  - Indicates a strong "glue" joint
- SEM imaging reveals the geometry of pulled indium coming to a sharp point
  - Characteristic of failure resulting from tensile loading
  - Indicates failure in the bulk indium and not a result of poor adhesion to the under-bump-metal

Indium as-deposited

Indium Pulled Apart



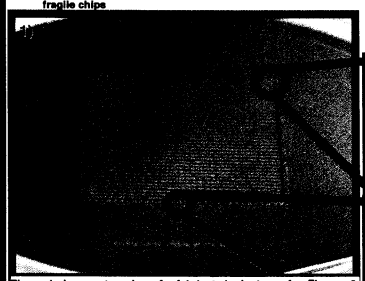
Indium pull-test data

CURRENT EFFORTS

- We have produced GISMO, a working 8x16 array of TES detectors
  - Architecture approaches the limit of utilizing a standard fan-out wiring scheme
- In development is a 32x40 element array on an 1135 micron pitch
  - Compatible with NIST's large format readout multiplexer
  - Our development scheme has produced detector models and readout substrates
    - Fabricated grid-detectors, comprised of 30 micron support walls
      - Used to verify mechanical robustness
    - Fabricated solid-detector models
      - Used to verify electrical continuity for each element in the array
      - Daisy chained pattern connected all the elements in a single column
      - Continuity indicated a good electrical path for each element
  - Fabricated custom tooling for use in holding the detector array during bonding

FABRICATED CUSTOM TOOLING

- 2 part custom tooling
  - SiC plate (not shown) that ports the vacuum
  - Silicon adapter, fabricated in-house, designed to handle fragile chips
- Silicon Adapter Features
  - Vacuum channel (a) along the perimeter for holding the chip in place
  - A grid structure (b) for mechanical support, identical to detector
  - Vent holes (c) in the outer elements
  - A shallow cavity (d) to avoid static forces on the membranes.



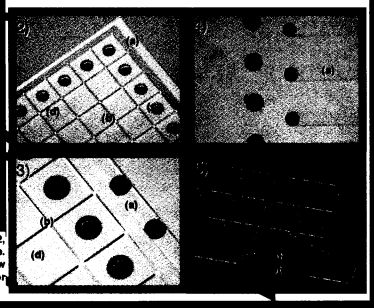


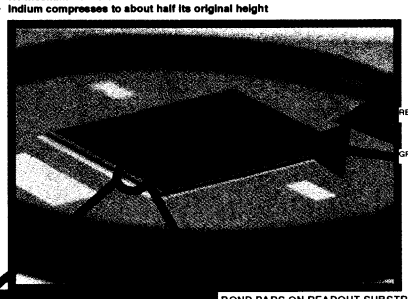
Figure 1 shows a top view of a fabricated adapter wafer. Figures 2, 3, and 4 show close-up views detailing the features outlined above. Figures 2 and 3 are top views, and Figure 4 shows the bottom view of Figure 3. Figure 5 shows a model of a top view of a grid-detector as it would appear being held by the adapter.

ELECTRICAL CONTIUTY

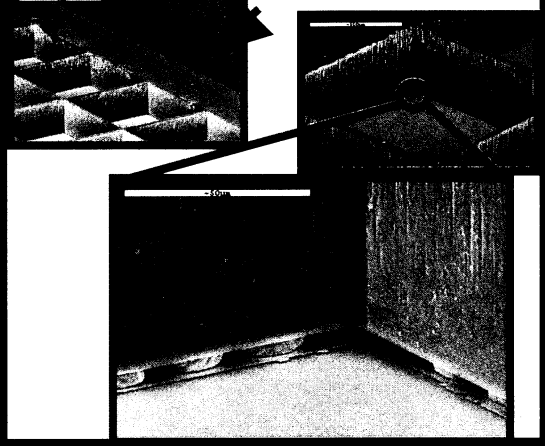
- Solid-detector chip bonded to readout substrates
- Full continuity measured for each of the 32 columns
- Indicated each detector element has continuous electrical path through indium.

BONDED MECHANICAL MODELS

- Bonded grid-detector chips (with-out membranes)
  - Demonstrated mechanical feasibility of bonding large fragile devices
  - 88 kgf peak loading or 0.4 gram-force per bump
  - No mechanical failures
  - Indium compresses to about half its original height



BOND PADS ON READOUT SUBSTRATE



FUTURE PLANS

- Optimization of the indium bond and the interfaces between metal layers to make superconducting paths at detector operating temperatures.
- Our long term plans include hybridizing a fully working detector chip, an array of TES bolometers supported by membranes and thin legs with through wafer via's, to a read-out substrate for testing.
- After passing electrical tests, a similar device will then be bonded to a NIST multiplexer.
- This design is intended to incorporate our "BUG" (Backshort-Under-Grid) architecture, where we place a grid of quarter-wave reflective backshorts behind the detector at a specified spacing. After attaching the BUG to the detector chip, the multi-component array will then be hybridized.

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