Indium Hybridization of Large Format TES Bolometer Arrays to Readout Multiplexers for Far-Infrared Astronomy

Timothy M. Miller,[a,b] Nick Costen,[a,b] Christine Allen[a]

[a]NASA Goddard Space Flight Center Code 553, 8800 Greenbelt Rd., Greenbelt, MD 20771, USA
[b]MEI Technologies, Inc., 4500 Forbes Blvd. Suite 200, Lanham, MD 20706, USA

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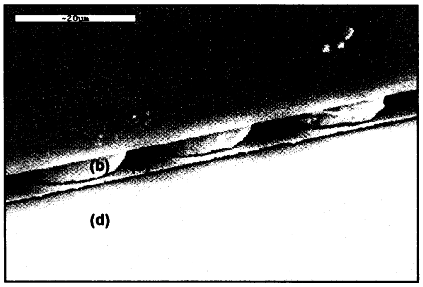
OVERVIEW

- Hybridization of Large Format Arrays
  - Indium bonded detector arrays containing 32x40 elements
  - Conforms to the NIST multiplexer readout architecture
    - 1135 micron pitch
  - Successfully fabricated mechanical models
    - Detector chips are bonded after being fully back-etched
    - Mechanical support consists of 30 micron walls between elements
  - Successfully demonstrated electrical continuity for each element
  - Characterized indium electrical path at cryogenic temperatures
- Goal to hybridize fully functional array of TES detectors to NIST readout



(a) DETECTOR WALL

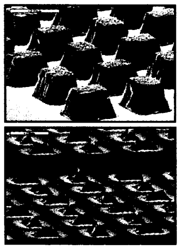
(b) INDIUM

(c) UNDER-BUMP-METAL

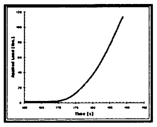
(d) SUBSTRATE

INDIUM BONDING

Indium bumps were producing using a thick photoresist lift-off mask in an evaporation deposition system. A forest of bumps, shown top left, is used along the perimeter of the bond and acts as a glue. The bond, performed in a Suss FC150, has been pull-tested using small test chips that simulate the large number of bumps needed. The graph to the right shows failure of the part at about 115 pounds of force, indicating a strong "glue" joint. SEM imaging of the pulled apart chip reveals the characteristic geometry of failure resulting from tensile loading. The indium comes to a sharp point near the mid-point of it's thickness and indicates that failure is from the indium itself and not a result of adhesion to the under-bump-metal.



SEM IMAGES



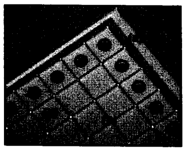
PULL-TEST OF INDIUM

CURRENT EFFORTS

Our current effort to develop a large format have produced GISMO, a working 8x16 array of TES detectors whose architecture approaches the limit of utilizing a standard fan-out wiring scheme. The next generation array in development is a 32x40 element array on an 1135 micron pitch making it compatible with NIST's large format readout multiplexer. In our development scheme we have produced detector models and readout substrates that allow for mechanical verification of the process as well as electrical continuity for each element in the array. Our goal is to hybridize a fully functional array of TES bolometers to a NIST multiplexer. The difficulties of indium bonding such a large delicate array led us to fabricate custom tooling for use in holding the detector array during bonding. Also, we fabricated detector models made of solid silicon for ease of testing electrical continuity, as well as grid detectors comprised of 30 micron walls delineating each element. The electrical path on the substrate was patterned in a way that daisy chained all the elements in a single column. A short path on the detector side connected one element to the next through a pair of indium bumps. Thus, electrical continuity indicated a good electrical path for each element.

CUSTOM TOOLING

The custom tooling includes a SiC plate (not shown) that ports the vacuum, and a silicon adapter, fabricated in-house, designed to handle fragile chips. The silicon adapter has several features that include a vacuum channel (a) along the perimeter for holding the chip in place, an identical grid structure (b) for mechanical support, vent holes (c) in the outer elements and a shallow cavity (d) to avoid static forces on the membranes. Figures 1 and 2 show top views of a fabricated adapter, Figure 3 shows a bottom view, and Figure 4 shows a model of a top view of a grid detector as it would appear being held by the adapter.



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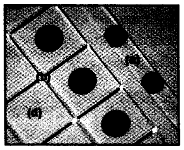

2)

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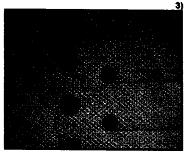

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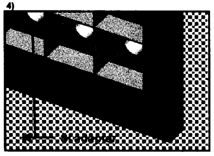


ELECTRICAL CONTIUTY

Measurements made of bonded solid detectors to readout substrates indicate full continuity for each of the 32 columns, indicated that each element has made intimate contact through the indium.

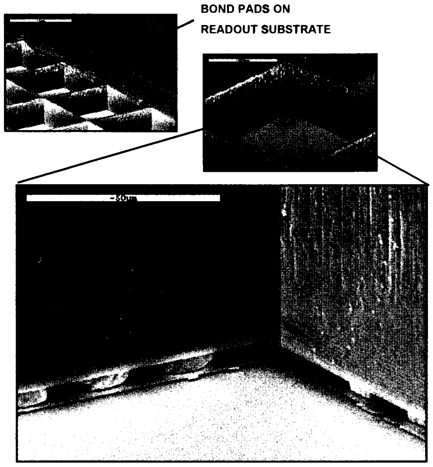
INDIUM CRYOGENIC TEST

PLACEHOLDER

MECHANICAL MODEL

Grid detectors were used to demonstrate mechanical feasibility of subjecting large fragile devices to the forces required to bond. Our test utilized 88 Kg at peak loading or 0.4 grams per bump. In all our test we never saw a mechanical failure. The following sequence on SEM images highlights the indium bond and shows that the indium compresses to about half its original height.

BOND PADS ON
READOUT SUBSTRATE



FUTURE PLANS

- Our long term plans include hybridizing a fully working detector chip, an array of TES bolometers supported by membranes and thin legs with through wafer via's, to a read-out substrate for testing.
- After passing electrical tests, a similar device will then be bonded to a NIST multiplexer.
- This design is intended to incorporate our "BUG" (Backshort-Under-Grid) architecture, where we place a grid of quarter-wave reflective backshorts behind the detector at a specified spacing. After attaching the two parts, the multi-component array will be hybridized.

ACKNOWLEDGEMENTS

The authors would like to thank the members of the Detector Development Lab at Goddard for their continued input and support.

Tim Miller

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1. INTRODUCTION

The advance of new detector technologies combined with enhanced fabrication methods has resulted in an increase in development of large format arrays. The next generation of scientific instruments will utilize detectors containing hundreds to thousands of elements providing a more efficient means to conduct large area sky surveys[1] [SCUBA-2 SPIE 2003 4855]. Some notable detectors include a 32x32 x-ray microcalorimeter for Constellation-X[2] [ref], an infrared bolometer called SAFIRE to fly on the airborne observatory SOFIA[3] [ref], and the sub-millimeter bolometer SCUBA-2 to be deployed at the JCMT which will use more than 10,000 elements for two colors, each color using four 32x40 arrays[4] [ref]. Of these detectors, SCUBA-2 is farthest along in development and uses indium hybridization to multiplexers for readout of the large number of elements, a technology that will be required to enable the next generation of large format arrays.

Our current efforts in working toward large format arrays have produced GISMO, the Goddard IRAM Superconducting 2-Millimeter Observer[5] [CA this conf]. GISMO is a far infrared instrument to be field tested later this year at the IRAM 30 meter telescope in Spain[6] [JS this conf]. GISMO utilizes transition edge sensor (TES) technology in an 8x16 filled array format that allows for typical fan-out wiring and wire-bonding to four 1x32 NIST multiplexers. GISMO's electrical wiring is routed along the tops of 30 micron walls which also serve as the mechanical framework for the array. This architecture works well for the 128 element array, but is approaching the limit for routing the necessary wires along the surface while maintaining a high fill factor. Larger format arrays will benefit greatly from making electrical connections through the wafer to the backside, where they can be hybridized to a read-out substrate tailored to handling the wiring scheme.

The next generation array we are developing is a 32x40 element array on a pitch of 1135 microns that conforms to the NIST multiplexer, already developed for the SCUBA-2 instrument[7] [NIST ltd10-p544]. This architecture will utilize electrical connections that route from the TES to the support frame and through the wafer. The detector chip will then be hybridized to the NIST multiplexer via indium bump bonding. In our development scheme we are using substrates that allow for diagnostic testing of electrical continuity across the entire array and we are testing our process to minimize or eliminate any contact resistance at metal interfaces. Our goal is hybridizing a fully functional 32x40 array of TES bolometers to a NIST multiplexer. The following work presents our current progress toward enabling this technology.

2. FABRICATION

Our architecture is unique in that the hybridization occurs after deep etching a cavity behind each element. What remains is a frame of walls, each 30µm wide supporting membranes on which the TES's will reside. The wiring runs from the TES to the frame via narrow membrane legs, the width and length of which help to control the thermal conductivity. Hybridizing such a fragile part requires custom tooling for handling during the bonding process. In contrast, the SCUBA-2 array is hybridized while the detector array is still a solid chip, and after bonding, trenches are deep etched to delineate each element[8] [ref?need?].

The development stage of this work is such that we are using inexpensive parts that mimic a NIST multiplexer and detector in layout without risking expensive substrates or valued detectors. The fabrication starts with selecting the right wafers. Our process uses four inch silicon wafers 500microns thick. Substrates are made from double side polished (DSP) silicon wafers while detector chips are made from DSP and silicon on insulator (SOI) wafers. Any wafer with flatness non-uniformity greater than 5 microns is rejected. This helps to ensure a high degree of planarity and to reduce gaps that might be larger than the indium itself. After standard cleaning, a thermal oxide 5000 Angstroms thick is grown for electrical isolation. The wiring and under-bump-metal are then deposited and patterned. The substrate is patterned to match a NIST multiplexer, with indium landing pads properly located on an 1135 micron pitch. The substrate metal is patterned so that each of the 32 columns of 40 elements is wired in series. The detector chip is patterned to propagate the signal from one element to the next in a given column and has pads only large enough to accept two indium bumps. Thus, when the two parts are hybridized, electrical continuity throughout one column indicates good electrical contact for each element in the column.

For indium deposition, we have developed a negative and a positive lift-off mask that are similar to previously published lift-off masks for thick indium[9] [ref]. While the positive process typically consists of two layers, we have developed a reliable three layer stack that yields consistent indium bumps. Both processes have their advantages, but most fabrication was done using the quicker negative process with the thick resist NR9-8000 from Futurexx. Thick lift-off masks are required to produce the target 10 micron tall indium bumps. The indium is deposited by thermal evaporation onto the substrate only, as seen in Figure 1 after the lift-off process.

The detector wafers do not get indium deposited on them, and after metal patterning the final processing steps were varied to produce a range of test samples. Some DSP wafers were diced to yield a solid detector chip for ease of bonding. Other wafers (DSP and SOI) were attached to glass backing wafers before being deep etched in a deep reactive ion etch (DRIE) system using the Bosch process. DSP silicon wafers are deep etched in a manner that produces a 32x40 grid structure of walls 30 microns wide, with no membranes. Backside processing of SOI detector wafers proceeds in a similar manner and produces grids with membranes.

Before hybridization, both parts are inspected for particles and undergo an extensive cleaning that involves high pressure solvent spraying and single particle removal using single-whisker brush. With the indium height at 10 microns, large particles could compromise planarity of the final part or even completely prevent a successful hybridization resulting in electrical opens. Prior to hybridization involves each part getting a final gas plasma surface treatment to improve adhesion and cold welding of the indium to the under-bump-metal. The plasma treatment temporarily passivates the indium surface and inhibits native oxide growth.

Detector chips were hybridized to readout substrates using a Suss MicroTec FC150 in a single sided indium bump process. The target bond force was 0.4 grams per bump based on our previous work[10] [ref SMTA]. The design incorporates a forest of indium bumps surrounding the perimeter of the chip as well as individual bumps located along each wall between elements, totaling more than 200,000 bumps and requiring a bond force of 88 Kg. The force is slowly ramped-up to allow for the indium to cold flow.

Standard silicon carbide tooling was used to hold the substrates and solid detector chips in place on the tool's vacuum chuck. In some cases, the grid detector chips were simply mounted to a carrier DSP wafer, meeting flatness tolerances, with wax for vacuum pick-up. While this worked well for proving a mechanical model it is not a preferred method. These chips were released from the carrier wafer in solvents after bonding. Ultimately, for the grid and membrane-grid detector chips, custom tooling is required to properly hold the parts on the tool. The custom tooling includes a silicon carbide plate that ports that vacuum to where it is needed and is combined with an in-house fabricated silicon adapter, shown in Figure 2, designed to handle the fragile detector chips. The silicon adapter has several features that include a vacuum channel along the perimeter for holding the chip in place, an identical grid structure for mechanical support, vent holes in the outer elements and a shallow cavity in which the membranes will sit over and avoid static contact. A grid detector is modeled in Figure 3 as it would appear being held by the adapter.

3. RESULTS

Prior to bonding large format arrays, smaller representative test chips were used to qualify the bonding process. These smaller chips were just under 2 cm square and contained approximately 180,000 bumps. Contact pads were connected through 4 pads of indium bumps and showed low electrical resistance of ~20 Ohms at room temperature in four-wire measurements. Two pairs of pads had the electrical path flow through on only four indium bumps on a pad and was shown to not compromise the circuit.

The success of the indium cold welding to the metallic pad is seen in Figures 4 and 5. Figure 4 shows the results from a pull-test, which indicates the force needed for failure to occur when the two chips are literally pulled apart. The graph indicates failure near 114 pounds for the sample shown. Typical values were 100 pounds, which for 180,000 bumps is 0.26 grams of force per bump. Figure 5 shows an SEM image of the failed bumps. The fact that the indium comes to a sharp point at the top is indicative of ductile failure from tensile loading. Also notice that the adhesion to the metallic landing pads is not compromised, all of which are indications that failure was within the bulk indium and the bond produced a strong cold weld with the landing pad. These results are sufficient to preclude the need for epoxy underfill, which is typical of some hybridized parts, specifically where gold studs are used in place of indium.

The TES arrays will require superconducting leads for the entire path to the readout multiplexer. As such, a test chip was tested cryogenically to characterize the indium at operating temperatures. The electrical response of the indium is shown to be superconducting for the test chip in Figure 6. The indium is seen to transition at xxx Kelvin, consistent with published results [ref]. The critical current was measured to be X.

Mechanical models were produced using grid detectors (without membranes) to prove that the fragile structure could survive the forces during bonding. As seen in Figure 7, the detector grids bonded successfully to substrates without any mechanical failures or defects. In one case, a single grid detector was re-bonded twice without failure. The grid detectors mounted with wax did not yield electrical continuity across the chip, likely due to the wax itself. It was noted that upon pressing the chip into the wax, in some areas, the wax flowed up the walls and may have interfered with the electrical path. Typical values of resistance measured for the full column series was in the mega-Ohms range or higher. The wiring used was measured to have a resistance of 2.3 Ohms/square in a 4-wire measurement. From this value we expect a full column to have resistance of approximately 1.7 kOhms not including contributions from the indium itself, which for a single column contains four bumps per element (2 per pad) totaling 160 bumps.

Parallelism of detector grids bonded to substrates was extremely good. This is typically measured from the top of the detector chip to the surface of the substrate and gives an indication of the gap between parts. A better measure of the gap is a direct measurement of the amount the indium compressed. The detector grid chips offer this unique opportunity as seen in Figure 8. The ten micron tall bumps were compressed to roughly half their original height to 5 microns.

Solid detector chips allowed for a check of electrical continuity as the solid chip did not require special tooling, including waxing to a carrier wafer. Solid chips did yield expected values for resistance along each column in the array.

Detector grids have been successfully bonded using the silicon adaptor for holding the part during bonding. As a result of bonding without the wax, electrical continuity has been successfully demonstrated.

Detector grids with membranes have been successfully bonded using the silicon adaptor for holding the part during bonding. The silicon adapter proved to hold the part while not damaging the fragile membranes. Electrical continuity has been successfully demonstrated on these parts as well.

4. CONCLUSIONS

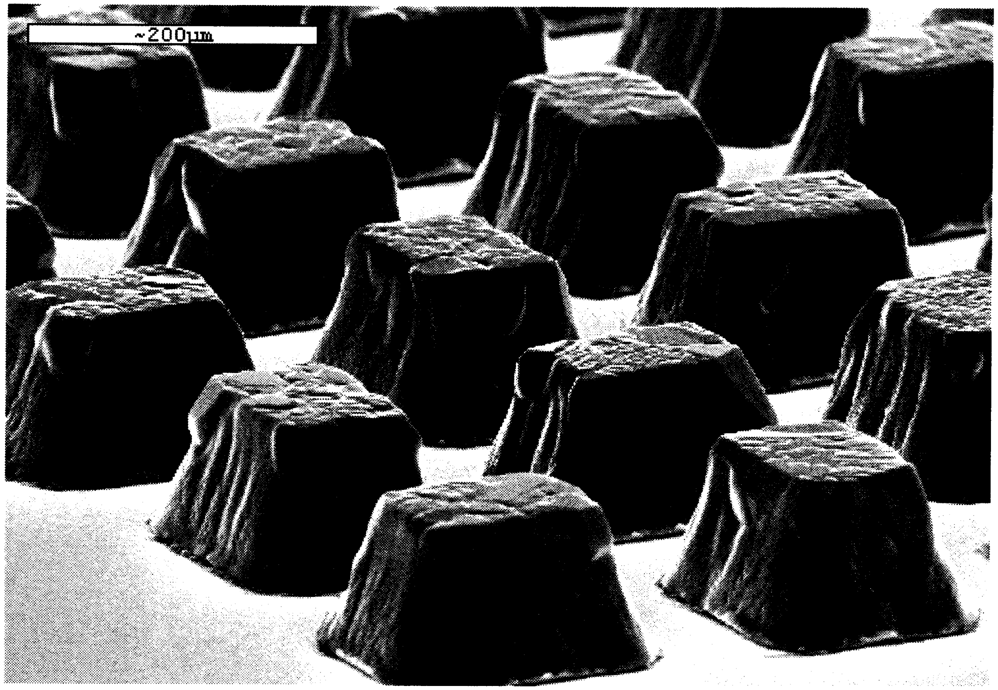
We have shown success in starting down a path that will lead us to enabling large format arrays for us in infra-red astronomy. Our initial tests have yielded fragile parts indium bump bonded to read-out electronics in which we have established electrical continuity. The indium has been characterized as superconducting at cryogenic temperatures suitable for TES's. We have also shown the strength of the indium bond to be independent of the metal interfaces as well as sufficient for joining two parts.

Our current efforts are geared toward demonstrating electrical continuity within expected resistance values of bonded membrane wafers to test substrates. Once we have achieved this milestone we plan to build an array complete with working TES's and membrane legs, and bond this part to a dummy read-out chip. Once this part can be tested cryogenically, showing all elements with working TES's we will commit to bonding a working array to a NIST multiplexer.

The detector chip architecture, with cavities created behind each element, allows for integration of a reflective backshort as a separate part. We have previously demonstrated the feasibility of integrating two separate parts in this way such that a specific spacing (within a certain range) can be met to improve optical efficiency[11] [ref LTD-11]. The main advantage in this scheme is that backshort spacings can be achieved independent of detector chip processing. For this method to work, the backshort would have to be integrated with the detector chip prior to bonding and may present a new set of difficulties. Demonstrating this triple stack of parts is a desirable goal as it will enable new generations of large format arrays.

5. REFERENCES

1 - [SCUBA-2 SPIE 2003 4855]
2 - Constellation-X [ref]
3 - SOFIA [ref]
4 - SCUBA-2 [REF]
5 - [CA this conf]
6 - [JS this conf]
7 - [NIST ltd10-p544]
8 - [SCUBA2 DRIE ref??]
9 - [IN LIFT-OFF ref]
10 - [ref SMTA]
11 - [ref LTD-11]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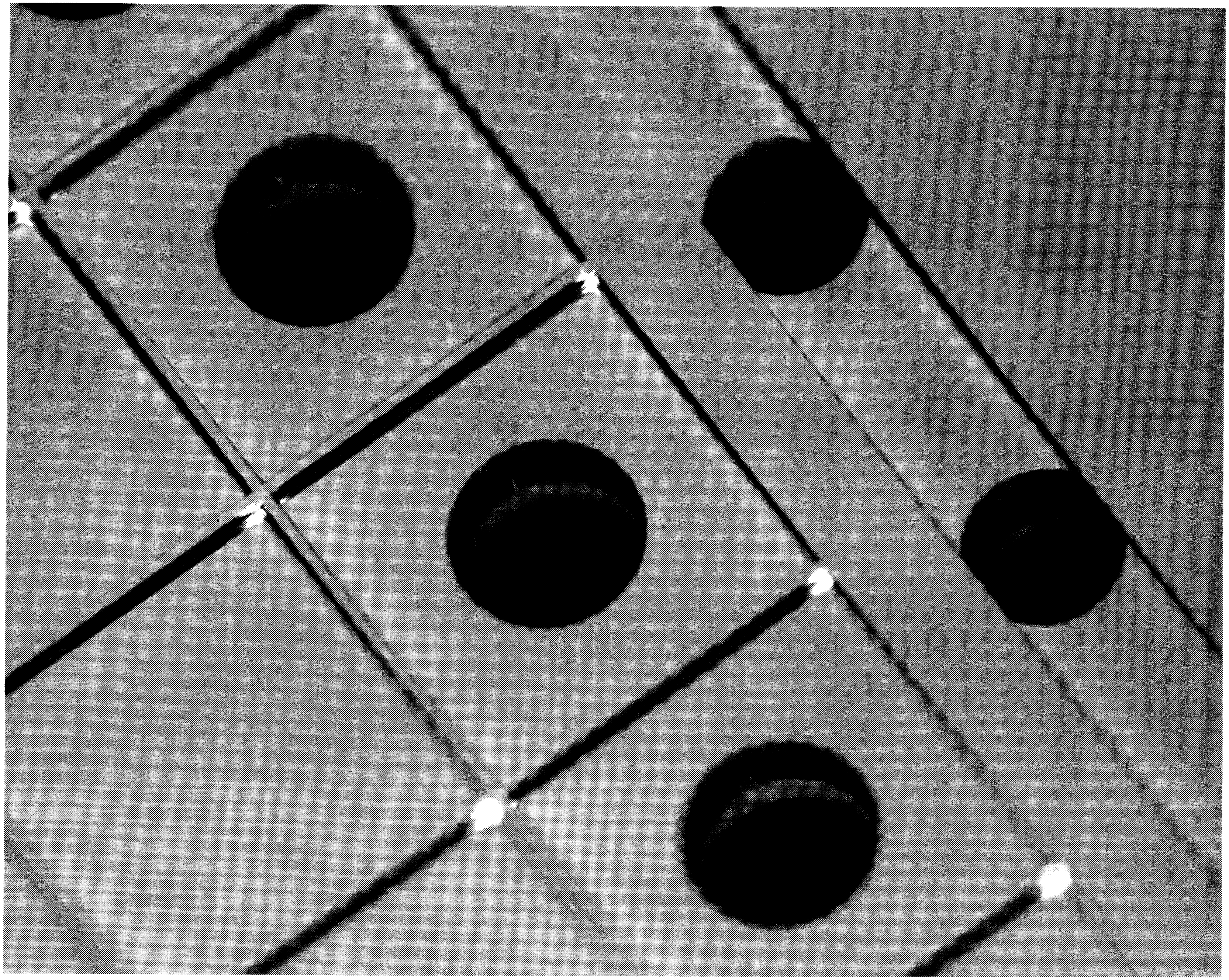

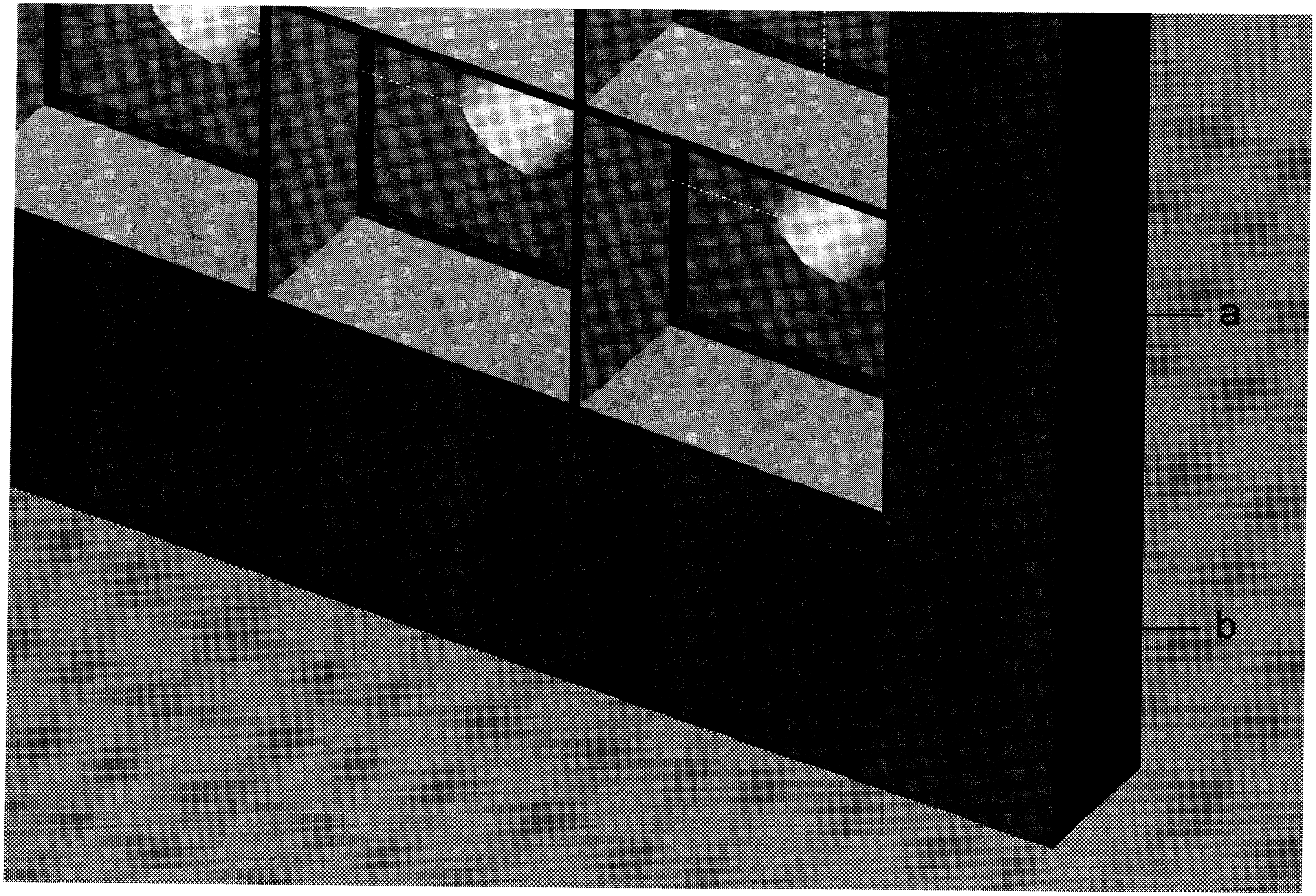
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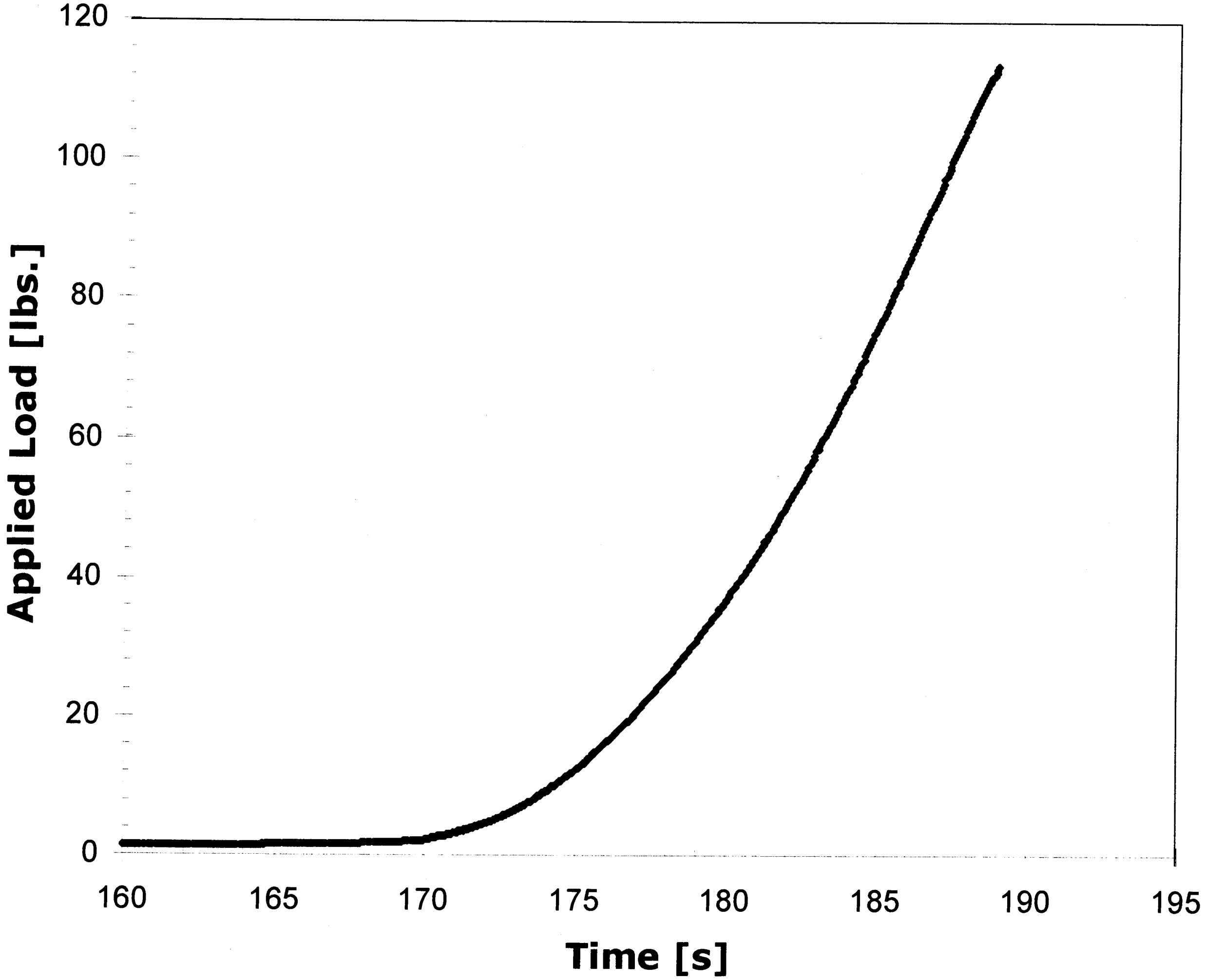
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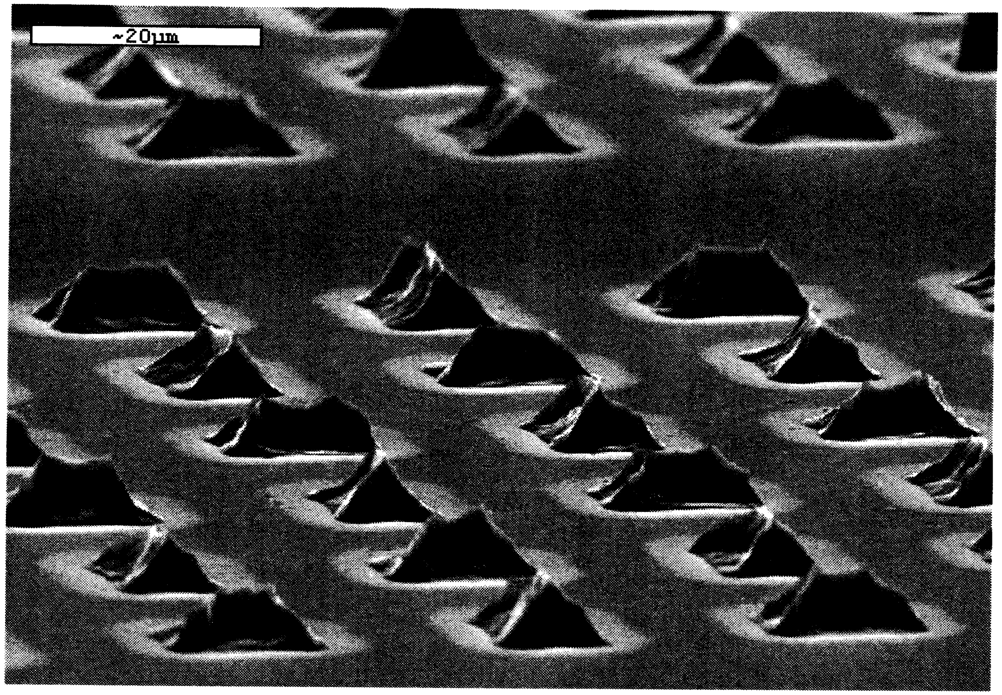
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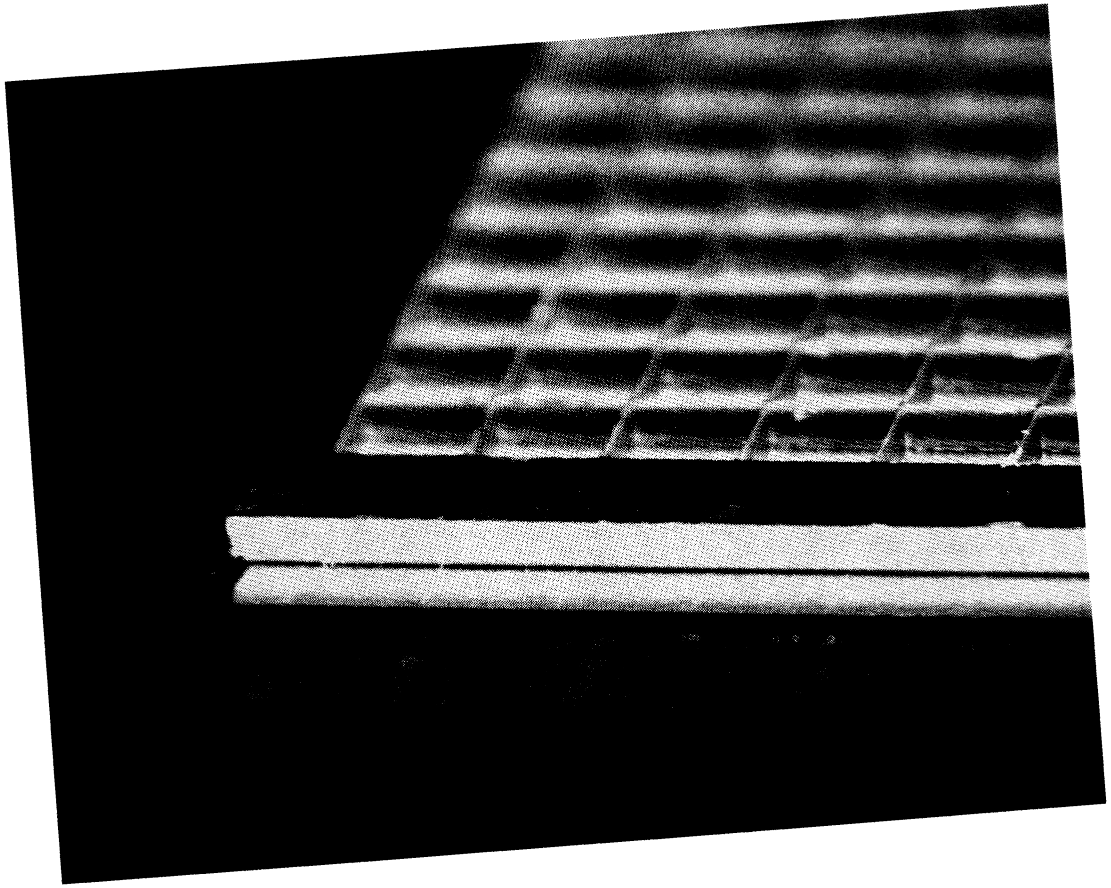
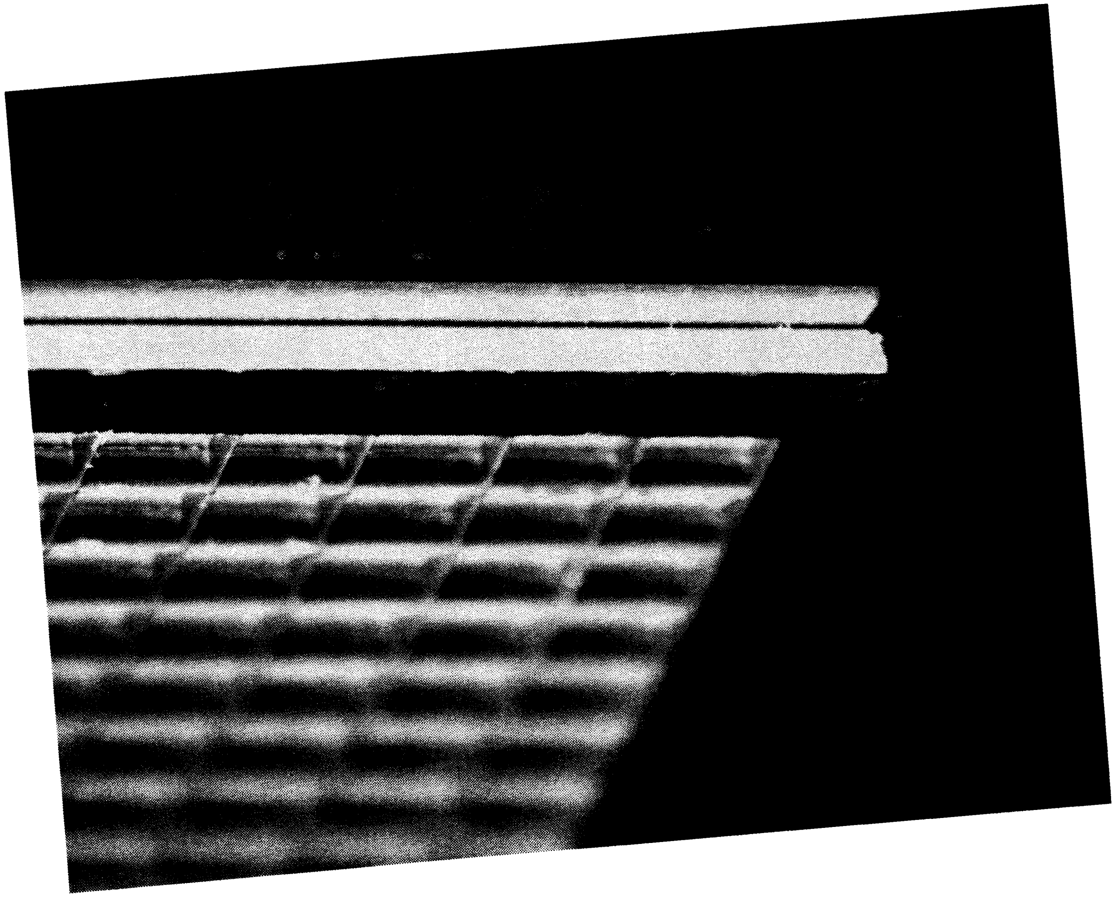
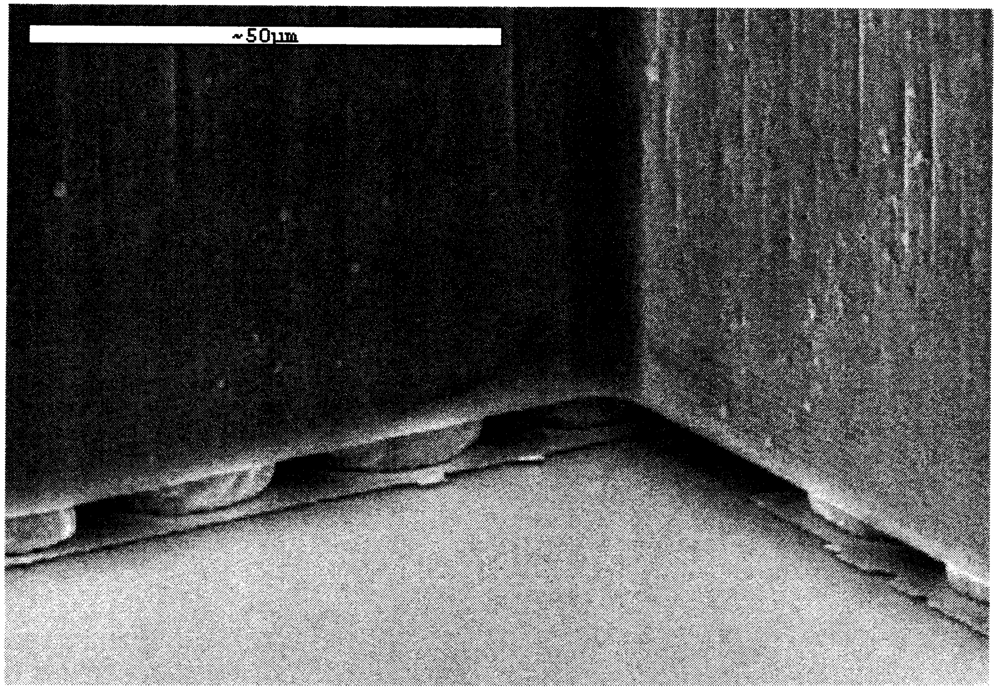
Indium Tc






~50µm

Optical Pic of bonded membrane