Technology Focus: Test & Measurements

Digital Phase Meter for a Laser Heterodyne Interferometer The design is suitable for numerous commercial products that utilize phase measurements.

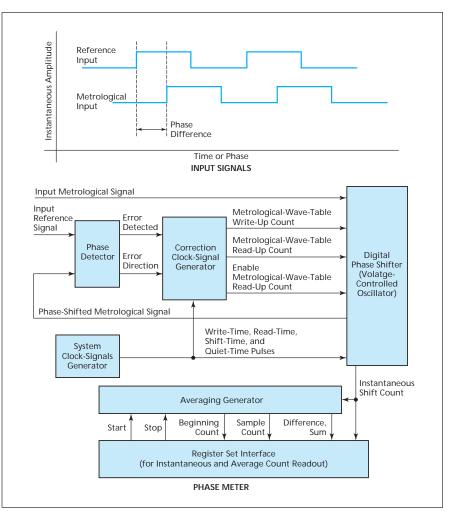
NASA's Jet Propulsion Laboratory, Pasadena, California

The figure depicts two digital waveforms and a block diagram of a digital phase meter for measuring the difference between their phases. This digital phase meter is being developed for incorporation into a laser heterodyne interferometer in a metrological apparatus, but could also be adapted to other uses. Relative to prior phase meters of similar capability, including digital ones, this digital phase meter is smaller, less complex, and less expensive. The phase meter has been constructed and tested in the form of a field-programmable gate array (FPGA) of fewer than 10⁴ gates.

A description of the signals to be processed is prerequisite to a meaningful description of this digital phase meter. There are two digital, half-duty-cycle square-wave input signals, denoted the reference and metrological input, respectively. Both signals oscillate at the same frequency, which, in the original intended application, is the laser heterodyne frequency (typically of the order of 100 kHz). In the original intended application, the phase difference between the two signals is directly proportional to a relative change in the lengths of portions of an optical path traversed by the laser beam.

The three main components at the heart of the phase meter are a phase detector, a correction clock-signal generator, and a digital phase shifter. These components are connected to form a phase-locked loop (PLL) that is a slightly modified version of a conventional PLL. The modification consists mainly in feeding the metrological input signal, instead of the reference input signal, to one of the input terminals of the phase shifter. That is to say, whereas the phase of the reference signal gets shifted in a conventional PLL, the phase of the metrological signal is the one that gets shifted in this PLL.

The reference signal is fed to one of the two inputs of a phase detector, while the phase-shifted metrological signal is fed to the other input of the phase detector, which measures the difference between the phases of its inputs and puts out a correction command (basically, a



The **Digital Phase Meter** is based on a modified phase-locked loop. When phase alignment between the reference input and the phase-shifted metrological input is achieved, the loop locks and the phase shift of the digital phase shifter equals the phase difference that one seeks to measure.

pair of error feedback signals) in an effort to drive the difference toward zero. The correction command is fed to the correction clock-signal generator, the outputs of which are fed as inputs to the digital phase shifter. The overall action of the loop is to shift the phase of the metrological signal until it becomes phase-aligned with the reference signal. When this alignment is achieved, the phase detector stops sending correction commands to the phase shifter.

One of the outputs of the phase detector is a number proportional to the instantaneous phase shift imposed on the metrological signal. This number is fed to an averaging generator and a register set interface for display of instantaneous and time-averaged phase readings, which can include readings from which initial values have been subtracted so as to indicate the change in phase shift from the initial to the current or final state of a metrological process.

This work was done by Frank Loya of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-40318