VHF Wide-Band, Dual-Polarization Microstrip-Patch Antenna

A dual-stacked-patch design incorporates several improvements over a basic design.

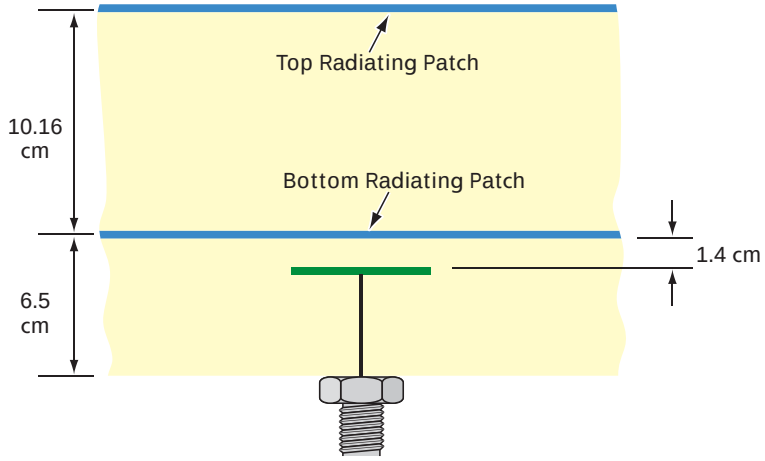
NASA's Jet Propulsion Laboratory, Pasadena, California

The figure depicts selected aspects of a very-high-frequency (VHF) microstrip-patch antenna designed and built to satisfy requirements specific to an airborne synthetic-aperture radar system for measuring the thickness of sea ice. One of the requirements is that the antenna be capable of functioning over the relatively wide frequency band of 127 to 172 MHz — corresponding to a fractional bandwidth of about 30 percent relative to a nominal mid-band frequency of 149.5 MHz. Another requirement is that the antenna be capable of functioning in either or both of two orthogonal linear polarizations. In addition, the antenna is required to be as compact and lightweight as possible.

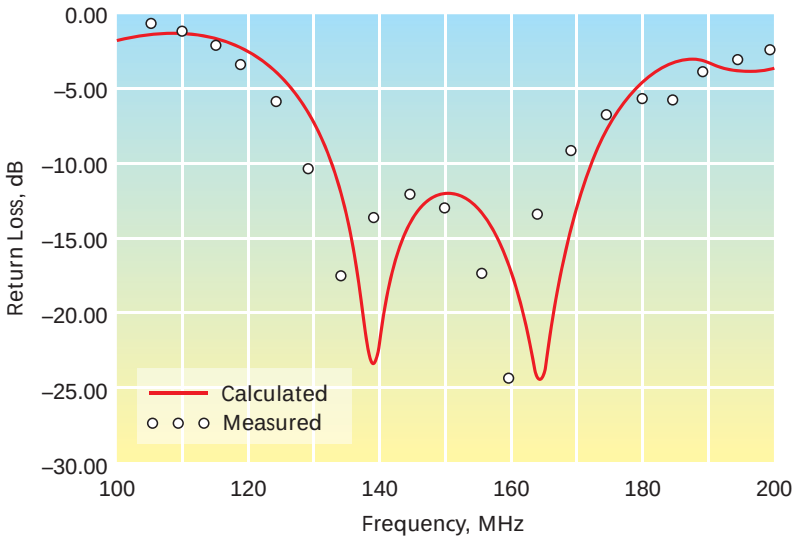
In a basic design according to generally accepted microstrip-patch-antenna-engineering practice, one would ordinarily use a relatively thick dielectric substrate and multiple feed probes to obtain the desired combination of wide-band and dual-polarization capabilities. However, the combination of a thick substrate and multiple feeds would give rise to higher-order electromagnetic nodes, thereby undesirably contributing to cross polarization and to reduction of the isolation between feed probes. To counter these adverse effects while satisfying the requirements stated above, the design of this antenna incorporates several improvements over the basic design.

The antenna features dual stacked square radiator patches, a ground plane, and relatively thick dielectric made of foam having a low value (1.05) of relative permittivity. The sides of the top and bottom radiator patches are 69.3 cm and 76.2 cm long, respectively. The patches are mechanically supported by the dielectric substrates. The bottom radiator patch lies 6.5 cm above the ground plane, which is a square of side length 117 cm. The top radiator patch lies 10.16 cm above the bottom radiator patch.

The bottom radiator patch is excited via square capacitive feed probes, the capacitive patches of which have a side length of 6.35 cm. The top radiator patch is excited parasitically from the bottom radiator patch. Four feed probes (instead of the minimum of two feed probes needed for dual polarization) are used to increase the wide-band capability, suppress higher-order modes, and reduce cross-polarization levels. Each probe is located 2.54 cm from the center of the antenna and its capacitive patch is located 1.4 cm below the bottom radiator patch. Within each pair of oppositely located



PARTLY SCHEMATIC CROSS SECTION OF PORTION CONTAINING A FEED PROBE



MEASURED AND CALCULATED INPUT RETURN LOSS

This **Dual-Polarization Microstrip-Patch Antenna** incorporates several design features to enable wide-band operation with minimal cross polarization and minimal coupling between orthogonal pairs of feed probes.

feed probes, the two probes are excited 180° out of phase with each other to suppress higher-order modes. For additional suppression of higher-order modes, a shorting pin is soldered to both the upper and lower patches and the ground plane at the center of the antenna.

In the absence of corrective action, the use of four feed probes and thick substrates would result in unacceptably large amounts of coupling between oppositely located probes. To reduce this coupling, 24 additional shorting pins, located along the two axes of symmetry, are soldered between the bottom patch and the ground plane. Power is coupled to the antenna via two 180° hybrids, each for exciting one of the pairs of oppositely located probes.

This work was done by John Huang of Caltech for NASA's Jet Propulsion Laboratory. For further information, contact iaoffice@jpl.nasa.gov.
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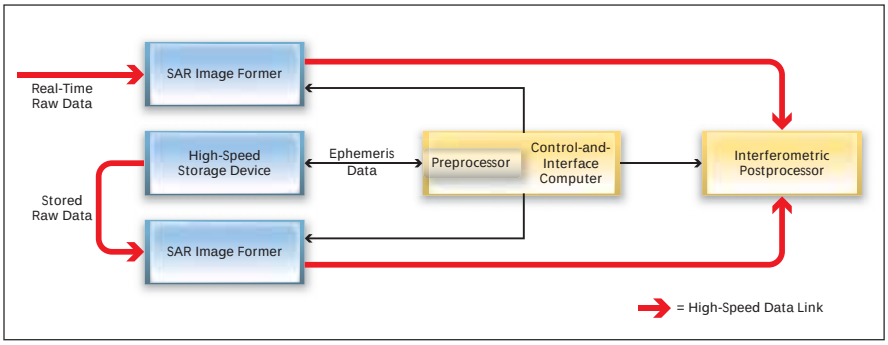
Onboard Data Processor for Change-Detection Radar Imaging

This system could be used to map earthquakes, landslides, floods, and wildfires.

NASA's Jet Propulsion Laboratory, Pasadena, California

A computer system denoted a change-detection onboard processor (CDOP) is being developed as a means of processing the digitized output of a synthetic-aperture radar (SAR) apparatus aboard an aircraft or spacecraft to generate images showing changes that have occurred in the terrain below between repeat passes of the aircraft or spacecraft over the terrain. When fully developed, the CDOP is intended to be capable of generating SAR images and/or SAR differential interferograms in nearly real time. The CDOP is expected to be especially useful for understanding some large-scale natural phenomena and/or mitigating natural hazards: For example, it could be used for near-real-time observation of surface changes caused by floods, landslides, forest fires, volcanic eruptions, earthquakes, glaciers, and sea ice movements. It could also be used to observe such longer-term surface changes as those associated with growth of vegetation (relevant to estimation of wildfire fuel loads).

The CDOP is, essentially, an interferometric SAR processor designed to operate aboard a radar platform. The CDOP design features a compact processor architecture chosen to combine the flexibility of microprocessors with the very high speed of field-programmable gate arrays (FPGAs) so as to optimize throughput performance while maintaining flexibility. The processor design addresses three critical requirements of real-time, onboard processing hardware for interferometric SAR imaging: high computational throughput, a large amount of onboard memory, and high-speed data interconnections throughout the processing chain. The functional blocks of the CDOP (see figure) include the following:



Real-Time and Stored Raw Radar Data are processed in the CDOP to generate images of surface changes in scanned terrain.

- *Preprocessor* — A microprocessor within a control-and-interface computer serves as a preprocessor that generates parameters necessary for generation of SAR image data from a combination of ephemeris and radar-configuration data. For the ephemeris data, the preprocessor implements a six-state (three position and three velocity coordinates) Kalman filter to effect real-time reconstruction of the platform trajectory from the outputs of an inertial navigation unit and a Global Positioning System receiver. The preprocessor also includes an azimuth pre-summer to decimate and re-align range-compressed data in the along-track direction, and an optional motion compensation-module for airborne interferometric SAR. The output of the preprocessor is utilized by the SAR image formers described next.
- *SAR Image Formers* — The raw SAR data are processed into SAR image data by two FPGA SAR processors that implement a range-Doppler algorithm with motion-compensation capability. The two SAR processors accept two input streams of raw radar data: typically, these would be (1) the real-time stream of data from the high-speed digital back end of the operating radar apparatus and (2) a stream of corresponding data from a previous pass retrieved from a high-speed storage device via a fiber-optic link. Alternatively, if the radar platform were to include two radar apparatuses in an interferometric configuration, then the CDOP could process the near-real-time streams of data from these apparatuses for use in generating a single-pass interferogram.
- *Interferometric Postprocessor* — Another microprocessor generates SAR interferometric image data from the outputs of the two SAR processors. In a typical application, the output of this processor would be transmitted to a ground station (downlinked). Because all of the processing up to the point of downlinking would be done onboard, the downlink data rate necessary for observing changes in the terrain would be significantly reduced.

This work was done by Yunling Lou, Ronald J. Muellerschoen, Steve A. Chien, and Sasan S. Saatchi Caltech and Duane Clark of Leeward Engineering for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).
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