to glass, of the robust, forgiving nature of the silicone material. The cover contains pockets that hold the solar cells in place during the lamination process. The cover is coated with indium tin oxide to make its surface electrically conductive, so that it serves as a contiguous, electrically grounded electromagnetic shield over the entire panel surface.

The cells are mounted in proximity to metallic printed wiring. The printed-wiring layer comprises metal-film traces on a sheet of Kapton (or equivalent) polyimide. The traces include contact pads on one side of the sheet for interconnecting the cells. Return leads are on the opposite side of the sheet, positioned to form the return currents substantially as mirror images of, and in proximity to, the cell sheet currents, thereby minimizing magnetic moments. The printed-wiring arrangement mimics the back-wiring arrangement of conventional solar arrays, but the current-loop areas and the resulting magnetic moments are much smaller because the return-current paths are much closer to the solar-cell sheet currents.

The contact pads are prepared with solder for electrical and mechanical bonding to the cells. The pocketed cover/shield, the solar cells, the printed-wiring layer, an electrical-bonding agent, a mechanical-bonding agent, a composite structural front-side face sheet, an aluminum honeycomb core, and a composite back-side face sheet are all assembled, then contact pads are soldered to the cells and the agents are cured in a single lamination process.

This work was done by Theodore G. Stern and Anthony E. Kenniston of DR Technologies, Inc. for Glenn Research Center.

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steve Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18156-1.

Improved Short-Circuit Protection for Power Cells in Series

Lyndon B. Johnson Space Center, Houston, Texas

A scheme for protection against short circuits has been devised for series strings of lithium electrochemical cells that contain built-in short-circuit protection devices, which go into a high-resistance, current-limiting state when heated by excessive current. If cells are simply connected in a long series string to obtain a high voltage and a short circuit occurs, whichever short-circuit protection device trips first is exposed to nearly the full string voltage, which, typically, is large enough to damage the device. Depending on the specific cell design, the damage can defeat the protective function, cause a dangerous internal short circuit in the affected cell, and/or cascade to other cells.

In the present scheme, reverse diodes rated at a suitably high current are connected across short series substrings, the lengths of which are chosen so that when a short-circuit protection device is tripped, the voltage across it does not exceed its rated voltage. This scheme preserves the resetting properties of the protective devices. It provides for bypassing of cells that fail open and limits cell reversal, though not as well as does the more-expensive scheme of connecting a diode across every cell.

This work was done by Francis Davies of Hernandez Engineering Inc. for Johnson Space Center. Further information is contained in a TSP (see page 1).. MSC-23446-1

Electromagnetically Clean Solar Arrays

Cells are laminated with shielding, narrow-current-loop wiring, and structural supports.

John H. Glenn Research Center, Cleveland, Ohio

The term "electromagnetically clean solar array" ("EMCSA") refers to a panel that contains a planar array of solar photovoltaic cells and that, in comparison with a functionally equivalent solar-array panel of a type heretofore used on spacecraft, (1) exhibits less electromagnetic interference to and from other nearby electrical and electronic equipment and (2) can be manufactured at lower cost. The reduction of electromagnetic interference is effected through a combination of (1) electrically conductive, electrically grounded shielding and (2) reduction of areas of current loops (in order to reduce magnetic moments). The reduction of cost is effected by designing the array to be fabricated as a more nearly unitary structure, using fewer components and fewer process steps. Although EMSCAs were conceived primarily for use on spacecraft, they are also potentially advantageous for terrestrial applications in which there are requirements to limit electromagnetic interference.

In a conventional solar panel of the type meant to be supplanted by an EMCSA panel, the wiring is normally located on the back side, separated from the cells, thereby giving rise to current loops having significant areas and, consequently, significant magnetic moments. Current-loop geometries are chosen in an effort to balance opposing magnetic moments to limit far-field magnetic interactions, but the relatively large distances separating current loops makes full cancellation of magnetic fields problematic. The panel is assembled from bare photovoltaic cells by means of multiple sensitive process steps that contribute significantly to cost, especially if electromagnetic cleanliness is desired. The steps include applying a cover glass and electrical-interconnection tabs to each cell to create a cell-interconnect-cell (CIC) subassembly, connecting the CIC subassemblies into strings of series-connected cells, laying down and adhesively bonding the strings onto a panel structure that has been made in a separate multi-step process, and mounting the wiring on the back of the panel. Each step increases the potential for occurrence of latent defects, loss of process control, and attrition of components.

An EMCSA panel includes an integral cover made from a transparent silicone material. The silicone cover supplants the

individual cover glasses on the cells and serves as an additional unitary structural support that offers the advantage, relative to glass, of the robust, forgiving nature of the silicone material. The cover contains pockets that hold the solar cells in place during the lamination process. The cover is coated with indium tin oxide to make its surface electrically conductive, so that it serves as a contiguous, electrically grounded electromagnetic shield over the entire panel surface.

The cells are mounted in proximity to metallic printed wiring. The printed-wiring layer comprises metal-film traces on a sheet of Kapton (or equivalent) polyimide. The traces include contact pads on one side of the sheet for interconnecting the cells. Return leads are on the opposite side of the sheet, positioned to form the return currents substantially as mirror images of, and in proximity to, the cell sheet currents, thereby minimizing magnetic moments. The printed-wiring arrangement mimics the back-wiring arrangement of conventional solar arrays, but the current-loop areas and the resulting magnetic moments are much smaller because the return-current paths are much closer to the solar-cell sheet currents.

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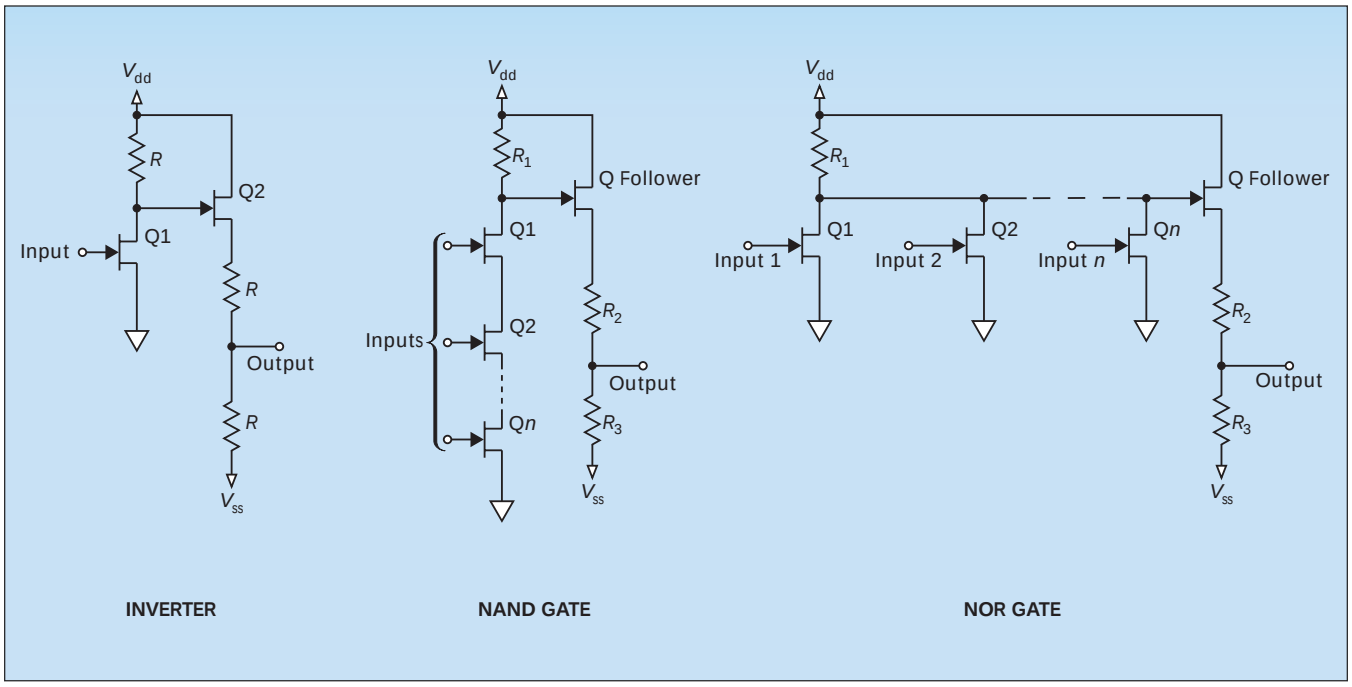
Logic Gates Made of N-Channel JFETs and Epitaxial Resistors

Gates could be implemented in SiC ICs for operation at high temperatures.

John H. Glenn Research Center, Cleveland, Ohio

Prototype logic gates made of n-channel junction field-effect transistors (JFETs) and epitaxial resistors have been demonstrated, with a view toward eventual implementation of digital logic devices and systems in silicon carbide (SiC) integrated circuits (ICs). This development is intended to exploit the inherent ability of SiC electronic devices to function at temperatures from 300 to somewhat above 500 °C and withstand large doses of ionizing radiation. SiC-based digital logic devices and systems could enable operation of sensors and robots in nuclear reactors, in jet engines, near hydrothermal vents, and in other environments that are so hot or radioactive as to cause conventional silicon electronic devices to fail.

At present, current needs for digital processing at high temperatures exceed SiC integrated circuit production capabilities, which do not allow for highly integrated circuits. Only single to small number component production of depletion mode n-channel JFETs and epitaxial resistors on a single substrate is possible. As a consequence, the fine matching of components is impossible, resulting in rather large direct-current parameter distributions within a group of transistors typically spanning multiples of 5 to 10. Add to this the lack of p-channel devices to complement the n-channel FETs, the lack of precise dropping diodes, and the lack of en-



This **Inverter, NAND Gate, and NOR Gate** are examples of logic circuits designed according to the principles described in the text. Other gates having greater complexity have also been designed.