# Fault-Tolerant, Multiple-Zone Temperature Control

NASA's Jet Propulsion Laboratory, Pasadena, California

A computer program has been written as an essential part of an electronic temperature control system for a spaceborne instrument that contains several zones. The system was developed because the temperature and the rate of change of temperature in each zone are required to be maintained to within limits that amount to degrees of precision thought to be unattainable by use of simple bimetallic thermostats.

The software collects temperature readings from six platinum resistance thermometers, calculates temperature errors from the readings, and implements a proportional + integral + de-
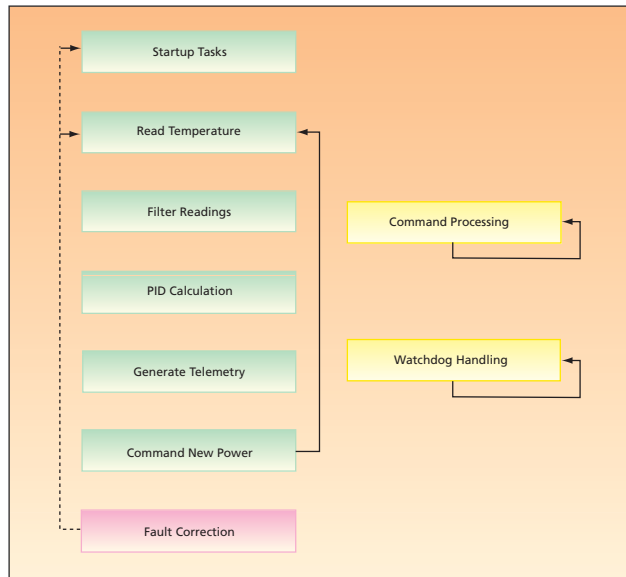
Logical Architecture of the active thermal control software.

rivative (PID) control algorithm that adjusts heater power levels. The software accepts, via a serial port, commands to change its operational parameters. The software attempts to detect and mitigate a host of potential faults. It is robust to many kinds of faults in that it can maintain PID control in the presence of those faults (see figure).

This program was written by James Granger, Brian Franklin, Martin Michalik, Phillip Yates, Erik Peterson, and James Borders of Caltech for NASA's Jet Propulsion Laboratory.

This software is available for commercial licensing. Please contact Karina Edmonds of the California Institute of Technology at (626) 395-2322. Refer to NPO-45230.

Implementing a Digital Phasemeter in an FPGA

NASA's Jet Propulsion Laboratory, Pasadena, California

Firmware for implementing a digital phasemeter within a field-programmable gate array (FPGA) has been devised. In the original application of this firmware, the phase that one seeks to measure is the difference between the phases of two nominally-equal-frequency heterodyne signals generated by two interferometers. In that application, zero-crossing detectors convert the heterodyne signals to trains of rectangular pulses (see figure), the two pulse trains are fed to a fringe counter (the major part of the phasemeter) controlled by a clock signal having a frequency greater than the heterodyne frequency, and the fringe counter computes a time-averaged estimate of the difference between the phases of the two pulse trains.

The firmware also does the following:
• Causes the FPGA to compute the frequencies of the input signals;
• Causes the FPGA to implement an Ethernet (or equivalent) transmitter for readout of phase and frequency values; and
• Provides data for use in diagnosis of communication failures.

The readout rate can be set, by programming, to a value between 250 Hz and 1 kHz. Network addresses can be programmed by the user.

This program was written by Shanti R. Rao of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

The software used in this innovation is available for commercial licensing. Please contact Karina Edmonds of the California Institute of Technology at (626) 395-2322. Refer to NPO-45575.
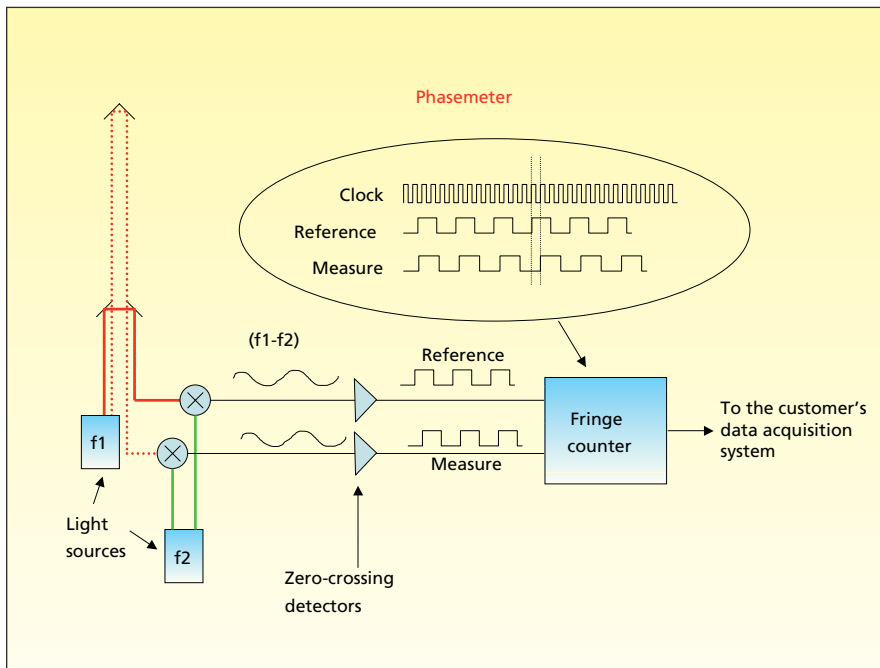
The **Firmware Code** converts two inputs (reference and measure) into a time-averaged estimate of the phase difference between the two signals.