

A Review of NASA's Radiation-Hardened Electronics for Space Environments Project

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NASA's Radiation Hardened Electronics for Space Exploration (RHESE) project develops the advanced technologies required to produce radiation hardened electronics, processors, and devices in support of the requirements of NASA's Constellation program. Over the past year, multiple advancements have been made within each of the RHESE technology development tasks that will facilitate the success of the Constellation program elements. This paper provides a brief review of these advancements, discusses their application to Constellation projects, and addresses the plans for the coming year.

Nomenclature

°C = Temperature (degrees Celsius)

I. Introduction

The Radiation Hardened Electronics for Space Environments (RHESE) project endeavors to expand the current state-of-the-art in radiation hardened electronics and avionics for high performance devices robust enough to withstand the extreme radiation and temperature levels of the space environment. The primary customers for RHESE technologies are the multiple mission elements of NASA's Constellation Program, including the Orion Crew Exploration Vehicle, the Earth Departure Stage of the Ares V launch vehicle, the Altair Lunar Lander project, Lunar Surface Systems elements, and Extra Vehicular Activity (EVA) elements. Secondary customers for RHESE technologies include NASA science missions, collaborative efforts with other agencies of the US Government, and commercial applications. The RHESE project is a part of the Exploration Technology Development Program (ETDP), which funds an entire suite of technologies needed for accomplishing many of the goals outlined in NASA's Vision for Space Exploration¹. For an external review of the ETDP and its multiple technology development projects, including the RHESE project, reference the recently released report from the National Research Council².

The individual technology development tasks that comprise the RHESE project are broad-based and diverse, but all carry the common goal of providing the customer with the ability to endure the extreme space environment with hardened electronics and avionics. Specifically, the individual RHESE technology development tasks that comprise the project are:

- Model of Radiation Effects on Electronics (MREE),
- Single Event Effects (SEE) Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF),

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- Radiation Hardened High Performance Processors (HPP),
- Reconfigurable Computing (RC), and
- Silicon-Germanium (SiGe) Integrated Electronics for Extreme Environments.

Because the RHESE project is an active technology development effort, advancements are continually being made to address the environmental hardness requirements of the multiple Constellation program projects. This paper builds on the project information provided in a previously publicized article³ and summarizes some of the more recent accomplishments made within each RHESE technology development tasks during the U.S. Federal Government's 2008 fiscal year, ranging from 01 October 2007 through 30 September 2008. Each of the five RHESE technology development tasks is addressed in the following sections, including a brief description of the task followed by a short summary of the past year's achievements.

A. RHESE Project Management

The RHESE project management function handles the day-to-day administrative and programmatic concerns of the project including budget planning, schedule development, accomplishment monitoring, risk assessment, and project execution. The project management function serves to enable the technology development tasks and to represent the task accomplishments to the ETDP program office. NASA's Marshall Space Flight Center (MSFC) manages the RHESE project. Within the past fiscal year, the RHESE project was baselined in its plan for technology development by the ETDP office with the details captured in the RHESE Project Management Plan.

As a strategy to reduce duplicative efforts between NASA and other government-sponsored developers that may also be investing in environmentally hardened electronic and avionic technology, it is the responsibility of the RHESE project management function to be cognizant of external activities and investments being made by these other U.S. Government agencies, federal laboratories, academic institutes, and commercial developers and to develop collaborative efforts where appropriate. Collaborative efforts strive to leverage the technology investments of multiple sources to deliver products that may otherwise not be realized through independent and competing efforts. To maintain cognizance of current activities, the RHESE project manager and task leads regularly attend reviews, presentations, and conferences where multiple other non-NASA technologists are working to improve the state-of-the-art in radiation hardened electronics. Over the past year, the RHESE project was represented at many of these gatherings to discuss and coordinate technology development activities, including the AIAA SPACE 2007 conference, the Air Force Research Laboratory (AFRL)-sponsored Radiation Hardened Electronics Technology workshop, the Space Technology and Application International Forum 2008, the Institute of Electrical and Electronics Engineers (IEEE) Aerospace 2008 conference, the Government Microcircuit Applications and Critical Technology (GoMACTech) 2008 conference, and the Nuclear Science and Radiation Effects Conference (NSREC) 2008. Coordination activities with other government-sponsored developers continue into the coming fiscal year with particular emphasis on the six technology development tasks as summarized in the following sections.

B. Model of Radiation Effects on Electronics (MREE)

RHESE's MREE task is focused on developing an updated model of radiation effects on electronics. The previously used model, Cosmic Ray Effects on Micro Electronics 96 (CREME96)^{4,5}, has been for years the industry standard modeling tool for estimating single event effects (SEEs) in electronics. However, over the past twelve years since its release, the state-of-the-art in microelectronics has continued to advance toward architectures that incorporate smaller feature sizes and more complex electronic structures that often include heavy metals – all of which make today's modern electronic architectures more susceptible to SEEs and radiation induced failures. The paradigm for SEE prediction in the CREME96 model is deficient in accounting for the small complex features common to modern electronic architectures. It is therefore the goal of the MREE task to develop a more physics-based approach to SEE prediction that will provide accurate results for modern electronics parts.

The new modeling tool will also be capable of taking into account the spacecraft's structure for purpose of calculating spacecraft self-shielding when assessing the susceptibility of a particular microelectronic circuit to the external radiation environment. This approach also allows the detailed physical structure of the microelectronic circuit and the pattern of hole-electron creation within that circuit structure to be taken into account so that the collected charge and the resulting currents within the circuit may be estimated more accurately. This new model employs Monte Carlo simulations to predict SEE rates, allowing the updated software to be referred to as "CREME-MC." The CREME-MC codes account for a propagating particle's energy loss attributable to interactions with the spacecraft, the electronic packaging, the metallization used to build the circuit, and the metallization located within the semiconductor itself. During propagation, the effects of nuclear interactions and energy loss by ionization are taken into account as well. The calculated radiation environment at the chip will be used to not only estimate the

device's accumulated total dose, but to also drive a second Monte Carlo simulation that predicts the SEE rate as described above.

Most of the accomplishments achieved by the MREE task within the past fiscal year stem from the establishment of the online CREME-MC website⁶ that will be employed to host the final Monte Carlo version of the CREME software. The online site currently offers the user the opportunity to execute a Monte Carlo based simulation of the energy deposition within a single defined sensitive volume that represents a single junction within the electronic device under evaluation. The site also offers a user the ability to define a multi-layered material stack that approximates the structure of the electronic device under evaluation. For continuity, the site will host the older CREME96 and CREME86 versions of the software. User files from the CREME96 site at Naval Research Laboratory⁵ will be moved to the new CREME-MC site⁶ at Vanderbilt allowing users the ability to access previously run data files. In order to ensure that the tool is appropriately addressing the needs of the electronics and avionics community, a period of "alpha" testing allowed select users the opportunity to run the code, evaluate the results, identify software problems, and submit comments that identify problems, deficiencies, or even desired capabilities that are not currently implemented. As of this past summer of 2008, the alpha testing concluded and the software began a period of "beta" testing.

The capabilities of the CREME-MC site will be upgraded as the new model is improved and extended. The models that define the space environment, such as the lunar neutron environment, the galactic cosmic ray environment, and the solar particle environment are all being updated. Features planned for implementation in the coming years include the development of a multiple, nested sensitive volume assessment capability, further upgrades to the environmental models, and full hosting of the CREME96 and CREME86 software tools and associated users' files.

Additionally, there are tools enable the conversion of spacecraft CAD drawings into a format used for Monte Carlo transport code calculations. The current plan is to incorporate these in a downloadable software package that can be used to compute the radiation environment at the part of interest within the spacecraft. The resulting environment will then be uploaded to the CREME-MC site for SEE calculations. This approach avoids the need for users to upload a CAD model of the spacecraft to the CREME-MC site over the internet. Instead, the users can maintain the security of their CAD model by doing the radiation transport calculations at their facilities.

This task is led by NASA's Marshall Space Flight Center with contracted support from Vanderbilt University.

C. Single Event Effects (SEE)-Immune Reconfigurable Field Programmable Gate Array (FPGA) (SIRF)

The FPGA is an electronic component that has experienced widespread usage in multiple applications due to its ease of programmability. Because the FPGA can be customized, it is also an inexpensive, and therefore attractive, alternative to the design and development of a non-programmable, hardwired application-specific integrated circuit (ASIC). FPGAs are available in multiple architectures. The most common is the SRAM-based FPGA, which is reprogrammable within an active system to perform a large variety of functions. But these FPGAs are much like volatile memory in that they require reconfiguration after each power cycle. Also, due to their CMOS-based architecture, they are susceptible to radiation events. Antifuse FPGAs solve the volatility and radiation susceptibility problem by allowing a single configuration to be permanently programmed onto the device. The nature of the antifuse architecture makes it intrinsically radiation-hardened, but the main disadvantage of this architecture is that it can only be programmed once prior to use.

In an effort to address the radiation hardness of a SRAM-based FPGA, the RHESE project is teaming with multiple government and industry partners to support the development of a radiation-tolerant version of the Xilinx Vertex-5 FPGA. The resulting device will yield the benefits of reconfigurable hardware without requiring the encumbrances typically required to harden reconfigurable devices to radiation effects, such as chip area, speed, power, and complexity. SIRF FPGAs can be used to implement systems that incorporate radiation-tolerant reconfigurable interfaces and digital interconnects. This capability will facilitate design of common 'plug-and-play' modular, adaptive and reconfigurable subsystems. Such subsystems can be field programmed and reprogrammed to implement multiple functions in diverse systems.

Though the effort is primarily supported by the SIRF task partners, NASA provides support to the effort to ensure the availability of this radiation hardened FPGA product for use within future space systems. The SIRF task has progressed toward maturity over the past fiscal year with incremental versions of the final product being fabricated and tested within a radiation environment. With each increment, more functional blocks within the FPGA are radiation hardened by design, bringing the total SIRF FPGA closer to maturity. Final delivery of the radiation hardened Xilinx 5 component is expected in June of 2010.

D. High Performance Processors (HPP)

Certain capabilities within the Constellation architecture, such as autonomous spacecraft operations, surface mobility, and hazard avoidance and landing, require intensive data processing capabilities. Whereas numerous systems with these capabilities have been developed and deployed, their requirements and implementations are typically constrained by data processing throughput, power resources, and radiation effects. The RHESE HPP task seeks to expand the capabilities of data processing-intensive, spaceflight systems by significantly advancing the sustained throughput and processing efficiency of high-performance radiation-hardened processors.

The performance of processors developed from technologies appropriate for aerospace environments lags that of commercial processors by multiple performance generations. For example, one of the “flagship” radiation-tolerant processors—the RAD750—exhibits a sustained throughput rate that is approximately two-orders of magnitude less than the commercially available Intel Centrino processor, used in many desktop and laptop computers.

Whereas radiation tolerant, commercially produced electronic boards offering increased performance are currently available, the performance is offered at expense of reduced power efficiency. The HPP task seeks to concurrently advance the state-of-the-art of two metrics, sustained throughput and processing efficiency.

The need for power-efficient high-performance radiation-tolerant processors and the peripheral electronics required to implement functional systems is not unique to NASA; this capability could also benefit commercial aerospace entities and other governmental agencies that require highly-capable spaceflight systems. This task will therefore leverage to the extent practical, relevant external technology- and processor-development projects sponsored by other organizations. Accordingly, important factors in defining and implementing the HPP strategy and implementation are the investment plans of these organizations and cognizance of relevant prior and ongoing NASA investments. The HPP team is address both of these factors through ongoing communication and collaboration with these other organizations.

In the end, the HPP task deliverables shall include a high-performance, radiation-hardened general-purpose processor and a high-performance, radiation-hardened special-purpose processor. This task objective may be accomplished with multiple types of processors or processor cores, given the broad range of applications that will require significant processing capability. Targeted classes include high-capability general purpose processors (e.g. a RAD750-type technology), instrument-level general purpose processors (e.g. microcontroller technology), and special purpose processors (e.g. FPGA-resident soft- or hard-core, reconfigurable processor, Digital Signal Processors (DSPs), host processor/coprocessor).

Within the past fiscal year, the HPP task has fostered two promising processor development activities that are currently undergoing evaluation for their suitability for use in NASA’s Constellation program. The first development is a collaboration between the RHESE project and NASA’s Innovative Partnership Program (IPP). A proposed effort between GSFC, JPL, and Coherent Logix Incorporated entitled “Extremely High-Performance, Ultra-Low Power, Radiation-Tolerant Processor: An Enabling Technology for Autonomous and Computationally Intensive Capabilities,” was selected for funding by the IPP. This effort seeks to assess the radiation susceptibility of the base HyperX processor, then formulate and implement radiation hardening strategies. The effort was awarded in 2008 and has already accomplished a baseline radiation test of the HyperX processor. To validate the radiation mitigation techniques, the processor will be flown as a part of the Materials International Space Station Experiment-7 (MISSE-7). The MISSE series of flight experiments provide an opportunity to assess the durability and functionality of various hardware components and materials during long duration exposure to the as the space environment. Launch of MISSE-7 is planned for 2009.

The second processor development activity being worked through the HPP task is the assessment of the On-board Processing Expandable Reconfigurable Architecture (OPERA) Processor. This effort began as a DARPA initiative to develop a processor that performs with a high level of efficiency across all categories of application processing ranging from bit-level stream processing to symbolic processing, and encompassing processor capabilities ranging from special purpose digital signal processors to general purpose processors. Evaluation versions of the OPERA processor have been procured and are currently being benchmarked to ensure the capabilities match the needs of the targeted Constellation applications.

This task is lead by NASA’s Goddard Space Flight Center, with support from NASA’s Marshall Space Flight Center, NASA’s Langley Research Center, and the Jet Propulsion Laboratory.

E. Reconfigurable Computing (RC)

The concept of RC offers the promise of new capabilities within any particular plan of exploration that involves complex spacecraft. These new capabilities focus on the reduction of subsystem level flight spares inventories for long-duration missions, adaptability to system failures, and flexibility in connecting components through a variety of data interfaces.

The RC task proposes a new paradigm for circuitry to respond to failures other than by redundancy voting schemes alone. The RC task strives to provide better failed circuitry detection, enablement of autonomous repair and/or replacement of defects, and support adapting circuitry to accommodate system failures. The goals of the RC task also include the concept of requiring a single configurable processor to autonomously conform to multiple configurations. Accomplishment of this goal yields a reduction in spares required to be carried on long-duration missions, since a single spare would then fit many processing functions. Such architecture adaptability will provide a great saving in spares volume and weight required by extended duration missions.

Three areas of focus have been identified for the RC task; internal modularity, external modularity, and fault detection and mitigation. The first involves ability of the core processor to emulate any form of computing resource as needed to serve all of the capacities required. The second enables the first by providing a capability to interface resources to any target system, by adapting communication standards, physical and electrical interconnections, and other parameters of the host system to hook up to the computing resource. The final allows the detection of an internal fault and autonomous isolation and recovery from the fault without required external involvement.

Cyclical and/or selective periodic testing will mitigate radiation damage and other commonly-feared failures. Reserve copies of circuitry will be generated and tested in order to bring them online in functional condition without interrupting system tasks. Then, the subsystem to be evaluated will be taken offline and tested with known inputs for known expected outputs in order to isolate possible undesirable responses. Provided the subsystem checks out as functionally correct, it can be returned to service, held in reserve for the next cycle of checks, or the reconfigurable processing units can be returned to a managed store for later redeployment. If the subsystem fails verification, the portions of circuitry causing the failure may be further isolated to mark those parts of the circuitry as defective and return the remainder to reserve, much as blocks of a computer hard disk are marked bad and ignored during future operations. Life limitations on electronics can be mitigated by these same means. Circuitry which becomes unstable and unreliable after extended active lifetime can be retired and new reserve circuitry powered up and configured into service, thus extending overall lifetime of the system.

Flexibility is also bolstered by the RC task. Interface reconfiguration can allow a single processor to make connections through different external interfaces as needed. By providing this external modularity, vehicle system integrity is enhanced by allowing processors to be transferred among busses and networks to replace lost functionality. Further, this directly supports the concept of reduced flight spaces required by long duration missions.

Over the past fiscal year, the RC task has procured a prototype hardware development platform from ElementCXI. This platform, referred to as the Elemental Computing Array (ECA), is being used to prove out reconfigurable computing concepts and to demonstrate these concepts through a controlling interface to multiple external peripherals. Immediate plans for the RC task include a demonstration of the RC concepts developed to date as executed on the ElementCXI hardware platform. This demonstration is planned for September of 2008.

Also, to ensure continued leadership in the reconfigurable computing community, the RC team sponsored two academic memberships in the Center for High Performance Reconfigurable Computing (CHReC), a consortium of academic representatives assembled to recommend Reconfigurable Computing research activities. Additionally, development of the Universal Reconfigurable Translator Module (URTM) continues, as contracted to Sigma Space. The URTM is capable of receiving a bus data stream in some predefined standard format, translating the data stream into a different predefined format, and then transmitting the data stream in the new format. A final acceptance review of the URTM deliverable is planned for the end of September of 2008.

This task is managed by NASA's Marshall Space Flight Center with support from NASA's Langley Research Center.

F. Silicon-Germanium (SiGe) Integrated Electronics for Extreme Environments

The RHESE SiGe task has as its goal the development and demonstration of extreme environment electronic components required for lunar robotic systems with distributed architecture, using low-cost, commercial SiGe Bipolar junction transistors within Complementary Metal Oxide Semiconductor (BiCMOS) technology⁷⁻¹¹. The SiGe BiCMOS offers unparalleled low temperature performance, wide temperature capability, and optimal mixed-signal design flexibility at the monolithic level by offering power efficient, high speed devices, such as the SiGe Heterojunction Bipolar Transistor (HBT) and high density Si CMOS.

The approach to implementing this task is to demonstrate system-critical SiGe BiCMOS mixed-signal integrated circuit components capable of operating reliably from -180°C to +120°C while under radiation exposure. In addition to the electronics, the packaging of the developed part is also required to be reliable for the specified temperature range. The SiGe development effort culminates in the development and test of a flight-ready remote electronics unit (REU) system prototype to serve as a general purpose, extreme environment ready, sensors and control interface system-in-package for NASA missions. The planned verification and testing strategy will consist

of characterization of the various SiGe mixed-signal components as a function of temperature, from -180°C to 120°C. Tests will also include radiation characterization to a total dose of at least 100 krad, life testing at the temperature extremes (-180°C and 120°C), and over-temperature part and package thermal cycle testing. Additional testing of components at cryogenic temperatures under radiation exposure will be used to evaluate the combined effects of temperature and radiation. When complete, the SiGe task will have matured a critical technology allowing many electronic components and data devices to be mounted such that they are exposed to the extremes of the space environment and no longer require the conditioning provided by the system's warm box.

The SiGe task has been producing increasingly complex designs that successively build toward the fabrication of a final REU prototype system. The "CRYO" moniker is used to identify the progressive stages of the development effort. Completed in 2005, the first iteration of the CRYO series, CRYO 1, was a proof-of-concept fabrication run containing SiGe-based basic circuit building blocks such as operational amplifiers, digital-to-analog converters, and standard characterization and test structures. The final REU prototype system, the CRYO 5 design, will be fabricated, tested and delivered in 2009. It will include a SiGe-based REU Sensor Interface (RSI) ASIC chip and a REU Digital Control (RDC) ASIC chip.

For purposes of testing the SiGe technology in the space environment, multiple flight experiments are underway which include SiGe-based electronic chips. Mounted on the MISSE-6 experiment are passive, unpackaged SiGe chips that function as a voltage reference. These circuits were protectively coated against atomic oxygen damage and tested prior to flight. Upon the retrieval of the MISSE-6 experiment, these circuits will be recovered and tested for operation. The NANOSAT program is another target for flying SiGe-based electronics. In cooperation with the Boeing Company, the SiGe team is planning to include an active, packaged version of the voltage reference circuit. And, in 2009, an active, packaged SiGe-based control circuit, the CRYO 3a design, will fly as an integrated portion of a Boeing experiment on the MISSE-7 experiment.

The contract for this task is managed by NASA's Langley Research Center with support from the Jet Propulsion Laboratory. The Georgia Institute of Technology is the prime contractor and leads a team made of multiple academic and industrial partners.

II. Conclusion

In response to the Constellation Program's need for environmentally hardened electronics and avionics, the RHESE technology development project is actively working to provide advancements in the areas of modeling of the radiation environment and its effect on advanced, modern electronics, FPGAs designed such that they are hardened against the radiation environment, High Performance Processors that will provide high efficiency, radiation hardened performance, Reconfigurable Computing capabilities that allow a single processor board to fulfill multiple functions, and SiGe-based electronics that allow operation in the low-temperature and radiation environments of the lunar surface. This overview paper provides a summary of each of these technology development tasks with an emphasis on the significant progress of the past fiscal year and identification of the additional development milestones planned for the coming fiscal year.

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