Channel Temperature Determination for AlGaN/GaN HEMTs on SiC and Sapphire

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Abstract

Numerical simulation results (with emphasis on channel temperature) for a single gate AlGaN/GaN High Electron Mobility Transistor (HEMT) with either a sapphire or SiC substrate are presented. The static I–V characteristics, with concomitant channel temperatures (T_{ch}) are calculated using the software package ATLAS, from Silvaco, Inc. An in-depth study of analytical (and previous numerical) methods for the determination of T_{ch} in both single and multiple gate devices is also included. We develop a method for calculating T_{ch} for the single gate device with the temperature dependence of the thermal conductivity of all material layers included. We also present a new method for determining the temperature on each gate in a multi-gate array. These models are compared with experimental results, and show good agreement. We demonstrate that one may obtain the channel temperature within an accuracy of ±10 °C in some cases. Comparisons between different approaches are given to show the limits, sensitivities, and needed approximations, for reasonable agreement with measurements.

I. Introduction

AlGaN/GaN HEMT amplifiers have achieved record power densities at microwave frequencies (refs. 1 and 2). Many of these "hero" devices have been small, and the aim of the experiments was to determine the power generation capability. The small units often consisted of one or two gates, so the problems of heat dissipation were not addressed. The large power density generated in power amplifiers causes considerable self-heating, and an accurate estimate for the channel temperature is needed for both design purposes and reliability estimates. For a practical device that will develop power at the multiple watt level, self-heating in the channel will be extreme. For power densities of 10 W/mm, the thermal management schemes will need to be more robust than those for other existing technologies, since the power density dealt with in AlGaN/GaN HEMTs is an order of magnitude larger. Knowledge of the strength of the self-heating is essential as increasing temperature reduces the mobility (it decreases as $T^{-2.3}$), and other basic material parameters, with resulting decrease in DC and RF performance (ref. 3). Thus severe reduction occurs in the output power, transconductance, cutoff and maximum oscillation frequencies, and the reliability. Preliminary results (refs. 4 to 6) for device failure or permanent damage, have indicated failures occur when the channel temperature rises into the 200 to 300 °C range. However, reports of undamaged devices after operation at 600 °C have been reported (ref. 7). Both the long and short period output power changes measured in many devices under stress testing are related to the device temperature. The trade-off in the number of fingers in a MMIC cell is controlled to some extent by the thermal hot spots that develop near the edge of the gate in the gate-drain access regions in the center of a multi-finger cell. These factors show the need for reasonably accurate estimates of the channel temperature in multi-gate devices.

The calculation of the channel temperature is, however, a difficult task for the following reasons. In principle, one should use a 2–D electro-thermal solver which performs a self-consistent calculation for

currents and temperatures for at least the basic cell (one source-gate-drain section). However, due to the large scale differences in the dimensions of the two-dimensional electron gas (2DEG) and the overall structure (substrate on the order of 350 μm), the simulations require complex meshing, and subsequently run for up to 15 hr. The 2–D self-consistent solver provides the initial estimate of the temperature field and the heat generation function $g(x,y)$ at the chosen bias point. The 2–D slice is 1 μm thick and is assumed to be in the center portion (with respect to z) of the device. Next one should use a 3–D thermal simulator with $g(x,y,z)$ as the source function, to obtain a more refined estimate for the temperature field. However, the prescription of generating $g(x,y,z)$ from $g(x,y)$ depends on the particular device geometry, etc. This approach has been emphasized in (ref. 8), as large inaccuracies from the 2–D runs may be present. Apparently the heat flow from the ends of the gate fingers can significantly affect the temperature field near the center (by up to 43 percent). One must also accurately define the boundary conditions; so the details of the top surface (passivation and metal layers) are needed. This information is usually not known precisely. This is a problem, as the heat generation region is sensitive to changes in physical details, bias, and the baseplate temperature. In any situation one must include the change in thermal conductivity with temperature of all material layers, or large errors will quickly accumulate.

Several 2–D and 3–D simulators (refs. 9 to 12) are available to determine temperature profiles. A 2–D electro-thermal package, MINIMOS-NT (ref. 13) considers the coupling between the current and heat transport equations, and thereby performs a self-consistent calculation. The SILVACO (ref. 14) software package, which we use, is also a self-consistent 2–D electro-thermal simulator.

In this memo we first present analytical models for channel temperature determination, and compare their predictions with measurements and simulations found in the literature. The accuracy is generally within 10 percent of measurements, and in some cases much better. These analytical methods are for both single and multiple gate devices, with any epitaxial layer sequence. We can handle effects of package dimensions, chip separations, and include the dependence of the thermal conductivity on temperature for all materials. Then we present results from the 2–D self-consistent electro-thermal solver ATLAS from SILVACO. We simulate I–V curves and measured temperatures from the only set of publications in the literature that have presented simultaneous I–V characteristics, and concomitant thermal measurements (refs. 15 to 18). We find good to excellent agreement. We have, for the first time, replicated measured I–V characteristics and channel temperatures for AlGaN/GaN HEMTs on both sapphire and SiC substrates.

As stated earlier, the calculation of the channel temperature is not easy, and its measurement is also not easy. Achieving both accuracy and spatial resolution is difficult, so a reasonably simple analytical prediction for amplifier/device level design purposes can be very helpful. When using such approximations, it is helpful to know the sensitivity of the final temperature with the many parameters involved. This sensitivity is investigated here. A final comment concerns the uncertainty in many of the critical device parameters. One can question the use of sophisticated software packages, when some of the material parameters are unknown by as much as an order of magnitude. Unfortunately this is the case, as the critical parameter (thermal conductivity) depends on a given layer's doping, growth procedure, process steps, and physical condition (cracks, etc.). This bolsters the need for a reasonably accurate analytical treatment.

II. Previous Analytical Methods

At the present time many investigators have studied the thermal properties of AlGaN/GaN HEMTs and GaN FETs under various conditions (refs. 19 to 31). They have presented combinations of measured data, 2–D and 3–D simulations, Monte Carlo results, and analytical schemes. The aim was to determine the channel temperature T_{ch} as the dissipated power changed. The change in T_{ch} may be due to changes in the bias point, baseplate temperature, or power added efficiency (PAE). In many cases constant thermal conductivity values were assumed, as this simplifies the problem (treats the system as linear). Figure 1

displays two possible plots of the channel temperature versus dissipated power. By definition, ΔT_{ch} (the increase in channel temperature) and the dissipated power P_{diss} are related by the "thermal resistance" R_{th},

$$\Delta T_{ch} = R_{th} \cdot P_{diss} \tag{1}$$

The final temperature T_{ch}, is ΔT_{ch} + reference temperature. The reference temperature is generally the baseplate's value. From inspection of the figure one sees that R_{th} is not constant, but varies with P_{diss}. This variation is due to many factors. One is the change in thermal conductivity as the temperature increases (it decreases with increasing temperature), and another is the change in the heat generation function $g(x,y,z)$ as the dissipated power increases. Generally $g(x,y,z)$ increases in magnitude and the volume over which this region extends gets more sharply defined. Also, the location of the peaks of $g(x,y,z)$ change as the current path through the device changes with bias and RF drive. The nonlinearity may be concave up or down, depending on circumstances. These differences may be due to the geometry of the finger layout, the edge effects, or the rise in the baseplate temperature with increasing power dissipation. For example, for a sapphire substrate, the channel temperature may be in the 320 to 370 °C range for dissipation near 6 W/mm. This temperature may be about 100° higher than the extrapolation from the low temperature linear assumption. For SiC at this same dissipation, the temperature may be only 95 °C. But in both cases, one cannot extrapolate from the low temperature line. In general then, R_{th} is a function that depends on many parameters, such as thermal conductivity and the detailed device geometry. This functional dependence will be explored in detail in subsequent sections.

The determination of channel temperature from analytical expressions is very difficult at the present time for many reasons. One complication is the appropriate form for the thermal conductivities $\kappa(T)$ as a function of the temperature T, for the various material layers. While assuming constant κ simplifies the analysis (treats the system as linear), we will show that the error is quite large for AlGaN/GaN HEMTs on either sapphire or SiC substrates. Even when this dependency is included, uncertainty exists for the proper values of $\kappa(T)$ in each layer. Since different growth methods and doping levels produce very different material properties, the reported measured values for $\kappa(T)$ have a large dispersion. For GaN (refs. 32 to 37), for sapphire (refs. 38 to 40), and for SiC (refs. 41 to 44). A second problem is the choice of the
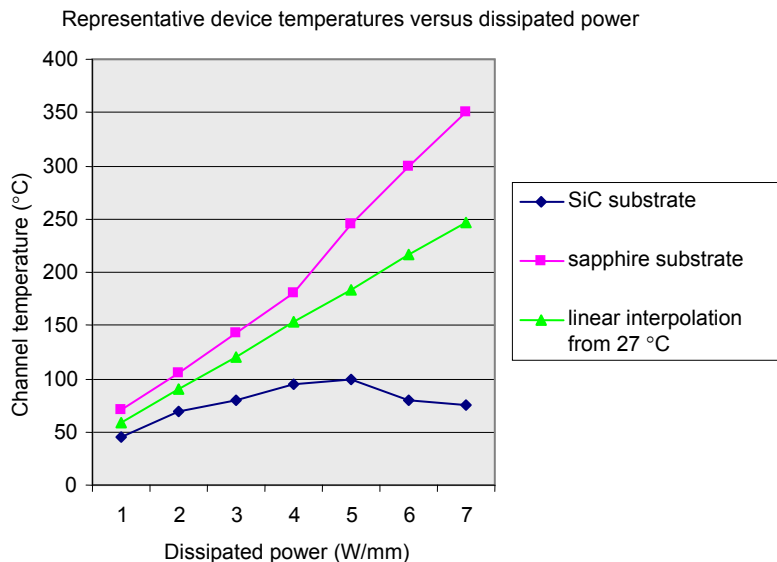
Figure 1.—Representative channel temperatures versus dissipated power for devices on sapphire or SiC substrates. The secants to the curves (originating from T_{ch} = 27 °C) are representative of the thermal resistances. The fact that the slopes are not constant reflects the changes in thermal resistance with dissipated power.

best approximate equations to use, as many have been published, and in many cases they don't all converge to a common value. We have also found that the discrepancies are due in part to errors in published equations and mislabeling of plots. We list a few problem areas:

1. In self-consistent 2–D simulators, does it matter that one uses the simpler drift-diffusion (D-D) approximation, or the more basic hydro-dynamic model? However, for the latter, what are the appropriate relaxation times? In the D-D formulation, one does not treat hot carrier effects (due to large electric fields) adequately. Also, what is the proper form for the mobility as a function of field, temperature, and doping? What is the effect of changing scatter-limited velocity with temperature? We assume some of these effects are minor, as will be shown later when we show excellent agreement with experiment.

2. Shorter gates enhance self-heating, and this is a very strong function of gate length.

3. Some experiments have shown variation of temperature *along* the gate fingers to be as much as 100 °C.

While many papers have appeared with methods to calculate the channel temperature, we will only concentrate on a few in this section. Recently Darwish, Bayba, and Hung (refs. 45 to 47) presented original closed-form expressions for calculating the thermal resistance of multi-finger AlGaN/GaN HEMTs and FETs. The two papers are complementary (one primarily for HEMTs, the other for FETs) in that somewhat different assumptions were used in each. The model consists of a vertical slice through a multi-fingered device, wherein the slice width is determined by inclusion of the source and drain pads with the gate in the center. The HEMT model specifies the GaN layer as region I, and the substrate is divided into two layers; regions II and III. In the first paper the isotherms were assumed to be circular cylinders, prolate spheroids, and elliptic cylinders, in regions I, II, and III, respectively. In the second paper, only a single layer is considered (appropriate for FETs), and the isotherms were assumed to be confocal ellipsoids and elliptical cylinders, as one moves from the gate to the heat sink. Attempts to verify the model included comparison with numerical simulation using ANSYS (for shapes of the isotherms and thermal resistance), and experimental data. The calculation assumes constant thermal conductivity and is restricted to multiple finger (greater than about 5) devices. They state the effects of non-constant thermal conductivity may be included by using the Kirchhoff transform; however they do not demonstrate the calculation. The wafer is assumed to be large in lateral extent, so end effects are neglected. The heat is generated by the gate electrode, and the thermal resistance is calculated assuming adiabatic boundary conditions on the vertical walls of the slice. This assumption implies that a few identical cells must exist on either side, so good results should be expected for devices with at least 5 or more gates. The demonstration of the close fit between the analytical equations and the shapes of the isotherms and thermal resistances as determined by the simulator ANSYS, makes the use of their results very compelling. There are, however, some drawbacks. The dependence on gate length is questionable; by this we mean the model for the gate shape is not completely convincing. The fact that the analytical equations results agree with the numerical simulations, means that the analytical model is correct. It does not mean that the model correctly reflects the heat source shape in actual HEMTs. The neglect of $\kappa(T)$ may have some effect on the shape of the isotherms as the temperature increases, and the resultant thermal resistance. In other words, the change in R_{th} with dissipation level (due to changes in $g(x,y,z)$ and $\kappa(T)$) is omitted. Also the variation of R_{th} with the number of fingers is eliminated by the nature of the calculation. Their equations are given below; see figure 2 for clarification of parameters. Note that Darwish et al. uses the symbol Θ for the thermal resistance R_{th}.

$$R_{th}(\text{total}) = R_{th}(\text{I}) + R_{th}(\text{II}) + R_{th}(\text{III})$$

$$R_{th}(\text{total}) = \frac{1}{\pi\, w_g\, k_{\text{Gan}}} \ell n\left(\frac{4\, t_1}{\pi\, L_g}\right) + \frac{1}{\pi\, w_g\, k_{\text{sub}}} \ell n\left\{ \frac{f\left(w_g / 2\rho\, t_1\right)}{f\left(\sqrt{1 + \left(\dfrac{w_g}{\sqrt{2}\,s}\right)^2 - \left(\dfrac{\rho\, t_1}{\sqrt{2}\,s}\right)^2}\right)} \right\}$$

$$+ \frac{1}{\pi s\, k_{\text{sub}}} \ell n\left\{ \frac{h\left[\left(\dfrac{w_g}{\pi\, t_2}\right)^2 - 4\left(\dfrac{\rho\, t_1}{\pi\, t_2}\right)^2\right]}{h\left[\left(\dfrac{w_g}{\sqrt{2}\,s}\right)^2 - 4\left(\dfrac{\rho\, t_1}{\sqrt{2}\,s}\right)^2\right]} \right\}$$

(2)

where

$$\rho = \frac{4\, k_{\text{GaN}}}{\pi^2\, k_{\text{sub}}}$$

$$f(x) = \frac{\sqrt{x+1} + \sqrt{x-1}}{\sqrt{x+1} - \sqrt{x-1}}$$

$$h(x) = \sqrt{\frac{\sqrt{x+1} + 1}{\sqrt{x+1} - 1}}$$
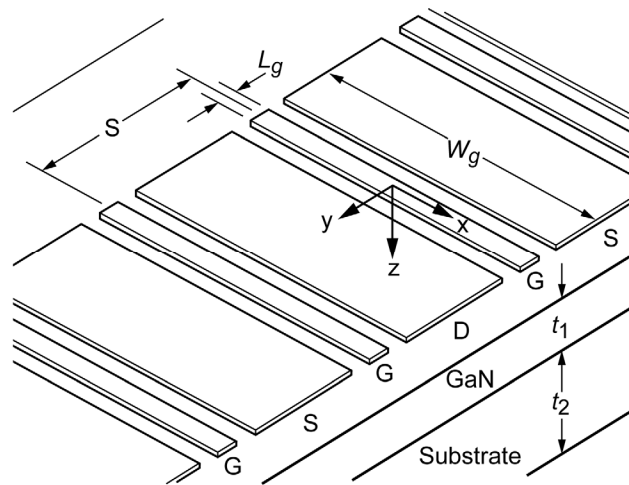
Figure 2.—Geometry for calculating thermal resistance, $R_{th} \equiv \Theta$, as given by Darwish, Bayba, and Hung (refs. 45 to 47).

III. Thermal Resistance Formulas for Single and Multigate HEMTs

In this memo we consider both single and multiple gate devices and include the dependence on temperature of the thermal conductivity as well as the actual size of the MMIC chip (end effects). The general layer structure for a typical device is shown in figures 3 and 4. Figure 3 gives a top view of an eight gate device, while figure 4 shows the approximate layer thicknesses and thermal conductivity ranges for all materials. Our procedure to determine the temperature of the gate electrode (which we assume is nearly the same as the temperature in the GaN channel) is a series of about nine steps. In general we determine the thermal resistance of each layer of the device, and from that along with the I–V product of the bias point, the temperature is determined. The schematic in figure 5 gives the geometry for both single and multiple gate situations for the calculation of the thermal resistance, R_{th}. The following list of steps gives a detailed explanation of our calculation procedure.
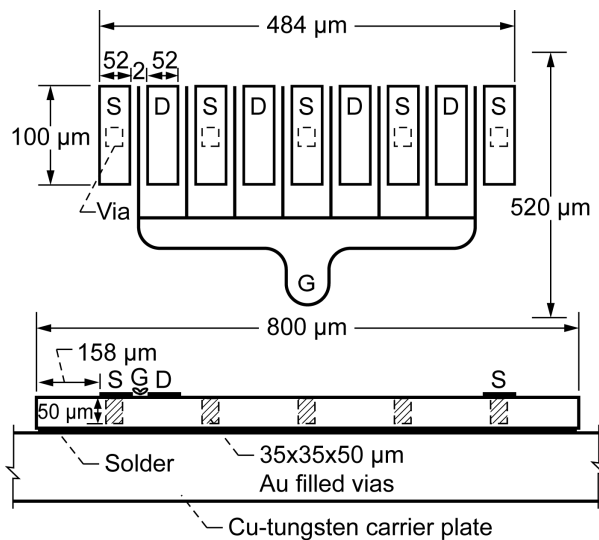
Figure 3.—Schematic of an eight gate AlGaN/GaN
HEMT for a microwave power amplifier.

Figure 4.—Cross-section model of the HEMT device,
showing approximate layers of material with average,
or ranges, of thermal conductivities.

Thickness	Material	Thermal conductivity
0.1-.175 µm	Si$_3$N$_4$ (passivation layer)	$\kappa = 0.0096$
0.02 µm	GaN (cap layer)	$\kappa = 1.6$
0.022 µm	Al$_{0.2}$Ga$_{0.8}$N (barrier layer)	$\kappa = 1.6$
0.5 µm	GaN (buffer layer) 2 deg*	$\kappa(T_0) = 1.6$ $\kappa(T) = $ calculated
0.015 µm	AlN (nucleation layer)	$\kappa = 0.1$
100 µm	SiC	Au source via $\kappa = 3.18$ $\kappa(T_0) = 3.4$ $\kappa(T) = $ calculated 35 µm
20 µm	AuSn AuGe Epoxy Silver epoxy	$\kappa = 2.4$ $\kappa = 0.9$ $\kappa = 0.3-.6$ $\kappa = 0.016-.075$
1000 µm	Cu-tungsten (carrier)	$\kappa = 4$

Note: The units for thermal conductivity κ are W/(cm-K)
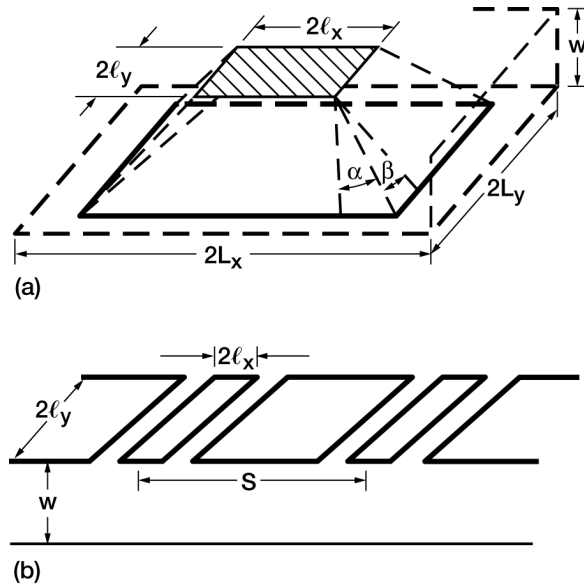* Two dimensional electron gas

Figure 5.—Geometry for calculating thermal resistance for (a) a device with a single gate finger, (b) multi-gate structures.

Thermal Analysis Procedure

1. For a single gate device, start at the bottom surface and assume the baseplate temperature T_b is known. Assume the temperature drop across the adhesive (solder) layer is small, so the bottom of the substrate is near T_b.

2. Calculate $\kappa(T_b)$ for either the sapphire or SiC substrate.

3. Calculate R_{th} for the substrate. We recommend the formulas published by Masana (ref. 48), which are valid for a single heat source with the overall size of the chip considered. See figure 5(a) for the geometry. The equations are:

$$L_g = 2l_x$$

$$W_n = W/L_x$$

$$\gamma_e = l_y/l_x$$

$$\gamma_s = L_y/L_x$$

$$l_{xn} = l_x/L_x$$

$$\rho_s = \kappa_i/\kappa_{i+1}$$

$$\tan \alpha = \left(1 - l_{x_n}\right) \frac{w_n + \dfrac{\rho_s}{1+\rho_s} l_{x_n}}{w_n + \dfrac{1}{1+\rho_s} l_{x_n}}$$

$$\tan \beta = \left(1 - l_{x_n} \frac{\gamma_e}{\gamma_s}\right) \frac{w_n + \dfrac{\rho_s}{1+\rho_s} l_{x_n} \gamma_e}{w_n + \dfrac{1}{1+\rho_s} l_{x_n} \gamma_e} \qquad (3)$$

$$R_{th}(\mathrm{T}) = \frac{1}{4\kappa(\mathrm{T})l_x} \frac{1}{\left[\gamma_e \tan \alpha - \tan \beta\right]} \ell n \left[\frac{l_x + w \tan \alpha}{l_x + \dfrac{w \tan \beta}{\gamma_e}}\right]$$

4.   In the previous step one needs the dimensions ($2l_x$, $2l_y$) of the effective flat strip heat source on the top surface of the substrate. The critical parameter is the effective gate length $2l_x$. For SiC use 4.5·(gate length), and for sapphire use 6.5·(gate length). There is some question as to the sensitivity of this assumption, as the actual size of the heat source is dependent on the bias point and the geometry of the structure. This is a critical step, as the final temperature is sensitive to the size of the heat source. All simulators that are not coupled electro-thermal calculators suffer with this problem, as they require the user to define the heat generation region $g(x,y,z)$. The formula for R_{th} is for constant κ, and the value is that for the temperature of the lower surface. With R_{th} determined, calculate the linearized or "equivalent temperature" θ at the top of the substrate (called the interface, int)

$$\theta_{\mathrm{int}} = R_{th} \cdot P_{diss}$$

where P_{diss} is the power dissipated for the single gate device, $P_{diss} = V_d \cdot I_d$, i.e., the product of the quiescent drain voltage and current.

5.   Find the actual temperature at the interface using the inverse Kirchhoff transform (discussed in more detail later)

$$T_{\mathrm{int}} = K^{-1}\left(\theta_{\mathrm{int}}\right)$$

6.   Calculate $\kappa(T_{\mathrm{int}})$ for the bottom of the GaN layer.
7.   Calculate R_{th} for the GaN layer similar to the above, but now use $2l_x = 1.125$·(gate length) for sapphire or (gate length + gate-drain access) for SiC.
8.   Calculate the linearized temperature at the top of the GaN layer, which we assume (define) to be the channel value,

$$\theta_{\mathrm{top}} = R_{th}(\mathrm{GaN}) \cdot P_{diss}$$

9.   Calculate the channel temperature

$$T_c = K_{\mathrm{GaN}}^{-1}\left(\theta_{\mathrm{top}}\right)$$

where the inverse transform used is that which is appropriate for the form of the thermal conductivity variation in GaN.

Observe $\rho_s = \kappa_i(T)/\kappa_{i+1}(T)$, for the i-th layer above the i-th +1 layer, thus the spreading angles α and β depend on the temperature T. We neglect the AlN layer which exists at the interface, as only a few

degrees exist across it in most cases. The effect of the low thermal conductivity of the AlN layer is reflected in the effective gate lengths used in the calculation. The low κ of the AlN tends to funnel the heat entering the top surface from the higher conductivity GaN layer into a narrower region than a spherical spread would be expected to do, before it enters the substrate.

For the multi-gate problem, we suggest the following procedure; first use the equations of either Darwish et al. (ref. 45), or Cooke (refs. 49 to 51, and 26). In these equation sets, use either the actual gate lengths for the heat source regions, or those indicated above. Next, use our more detailed calculation method; which will be described in detail in the following section. This procedure gives the temperature on each finger, unlike that of the above schemes, which can only give an "average" channel temperature. The formulas from (ref. 49), with typos corrected, are as follows (again refer to fig. 5):

$$
u = \frac{\cosh\left[\frac{\pi}{4}\left(\frac{s + 2l_x}{w}\right)\right]}{\cosh\left[\frac{\pi}{4}\left(\frac{s - 2l_x}{w}\right)\right]}
$$

$$
M = \frac{2\sqrt{u} + 1}{\sqrt{u} - 1}
$$

$$
P = 2\sqrt{\frac{\cosh\left[\frac{\pi}{4}\frac{2l_x}{w}\right] + 1}{\cosh\left[\frac{\pi}{4}\frac{2l_x}{w}\right] - 1}}
$$

$$
R_{th}(T) = \frac{\frac{n}{2l_y \kappa(T)\pi}}{\left[\frac{2(n-1)}{\ln M} - \frac{(n-2)}{\ln P}\right]}
$$

(4)

We digress here to review the Kirchhoff transform. In principle, in any heat transport problem, one solves for the temperature field from the heat flow equation

$$
\nabla \cdot \{\kappa(T)\nabla T\} = -g(x, y, z),
$$

(5)

where $\kappa(T)$ is the temperature dependent thermal conductivity in the i-th layer, T is the temperature, and $g(x,y,z)$ is the dissipated power density in W/cm^3. This quantity is also called the heat generation density (source) region. The equation is altered by defining an equivalent, artificial, "linearized" temperature via the Kirchhoff transform (refs. 53 and 54),

$$
\theta = T_o + \frac{1}{\kappa(T_o)}\int_{T_o}^{T}\kappa(\xi)d\xi
$$

(6)

which relates the three temperatures T, T_o, θ; the actual, reference, and linearized or transformed value, respectively. The transformed, linearized, or effective, temperature on the top surface of the substrate is

$$
\theta_2 = T_b + R_{th}(\text{substrate}) \times P_{diss},
$$

(7)

where the known constant value for $\kappa(T_o)$ has been used in the determination of R_{th}(substrate). The real, or actual, or physical temperature at the top surface is determined from the inverse of the Kirchhoff transform

$$T_2 = K_{\text{sub}}^{-1}\{\theta_2\} \tag{8}$$

For the functional form

$$\kappa(T) = \kappa(T_o)(300/T)^r, \tag{9}$$

where T_o = 300 K unless stated otherwise. The inverse Kirchhoff transform formula is

$$T_{\text{actual}} = \left\{[\theta - r(\theta - T_o)]/T_o^r\right\}^{(1/(1-r))} \tag{10}$$

and the inverse is

$$\theta = 1/(r-1)\left[rT_o - T_o^r T^{1-r}\right]. \tag{11}$$

When $r = 1$, we have

$$T_{\text{actual}} = T_o \exp\left([\theta - T_o]/T_o\right), \tag{12}$$

where θ is the effective temperature, and T_o is the temperature at the bottom surface (the reference value). The temperature on the AlN top surface is

$$T_3 = T_2 + R_{th}(\text{AlN}) \times (P_{diss}/n), \tag{13}$$

where n is the number of gates. This assumes each gate dissipates the same power. Experimentally we know the gates near the middle are the hottest, and they probably dissipate the largest power. Finally, the junction, or channel temperature, at the AlGaN/GaN interface is found by

$$\theta_4 = T_3 + R_{th}(\text{GaN}) \times (P_{diss}/n) \tag{14}$$

$$T_4 = K_{\text{GaN}}^{-1}\{\theta_4\}. \tag{15}$$

Figure 6 summarizes the approximate heat flow pattern and the temperatures in the thermal resistance stack. Observe the AlGaN layer is neglected as it is extremely thin (up to maybe 500 Å at most).

At this stage of development of GaN technology, the actual values of the thermal conductivities of the various epitaxial layers, and their variations with temperature are not known to great accuracy. This necessitates that we must generate reasonable expressions to continue with the calculation. We choose the following expressions:

GaN:

Old
$$\kappa(T) = 1.6\left(\frac{300}{T}\right)^{1.4} \tag{16}$$

New
$$\kappa(T) = 1.97\left(\frac{300}{T}\right)^{0.48} \tag{17}$$

Kuball's (ref. 15)
$$\kappa(T) = 1.6 \left(\frac{300}{T} \right) \tag{18}$$

SiC:

For doping levels near 10^{17} cm^{-3}
$$\kappa(T) = 3.4 \left(\frac{300}{T} \right)^{1.5} \tag{19}$$

For semi-insulating (S.I.)
$$\kappa(T) = 5.2 \left(\frac{300}{T} \right)^{2.4} \tag{20}$$

Sapphire:

$$\kappa(T) = \frac{73.9}{T - 159} \approx 0.49 \left(\frac{300}{T} \right). \tag{21}$$

Figures 7 and 8 display the variations with temperature for GaN, and SiC, and sapphire, respectively. For GaN, the old expression was developed by assuming the coefficient was similar to that of GaP (which was measured), and averaging published room temperature values. The new equation utilizes some recently measured data. Observe at 300 K they differ by 18 percent. The expression by Kuball assumes a $1/T$ variation, and was used in his simulations. The value for SiC is an average of many experimental determinations. For sapphire, the first expression is a curve-fit of experimental data, while the second is an approximation for the basic $1/T$ form. Figure 9 gives the variations of GaAs, Si, and InP; and the analytical expressions are:

GaAs:
$$\kappa(T) = 0.47 \left(\frac{300}{T} \right)^{1.2} \tag{22}$$

Si:
$$\kappa(T) = 1.45 \left(\frac{300}{T} \right)^{1.324} \approx 1.45 \left(\frac{300}{T} \right)^{1.2} \approx 1.7 \left(\frac{300}{T} \right)^{1.4} \tag{23}$$

InP:
$$\kappa(T) = .658 \left(\frac{300}{T} \right)^{1.48} \tag{24}$$

It is obvious that the value for all materials at room temperature, is uncertain by 8 to 18 percent, and the variation with temperature has some dispersion. The reasons are due to the quality of the tested films, and the range over which the fit was obtained. Thus we must be prepared to predict temperatures only to within 5 to 10 percent of measured values due to these uncertainties.
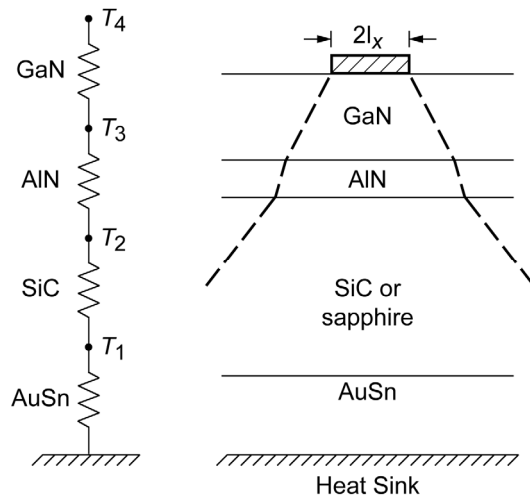
Figure 6.—Thermal resistance stack and schematic
(not to scale) of heat flow through the layers.

Thermal conductivity approximations for GaN
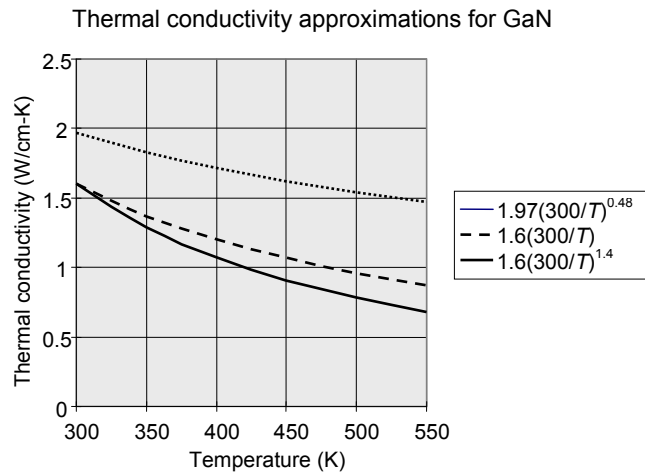
Figure 7.—Approximations for the temperature
dependence of the thermal conductivity of GaN.

Thermal conductivity approximations for SiC and sapphire
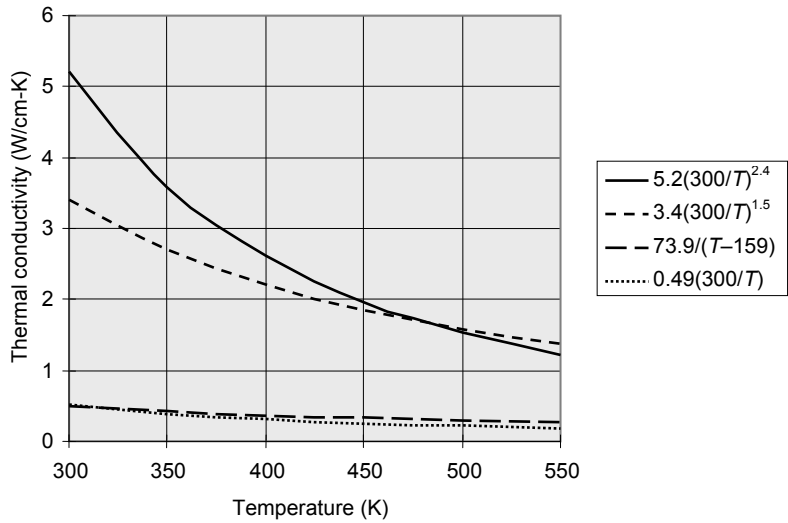
Figure 8.—Approximations for the thermal conductivities of SiC and sapphire. The upper-most curve is for semi-insulating SiC, while that below it is for doped SiC. The sapphire values are the lower two curves.

Semiconductor thermal conductivities
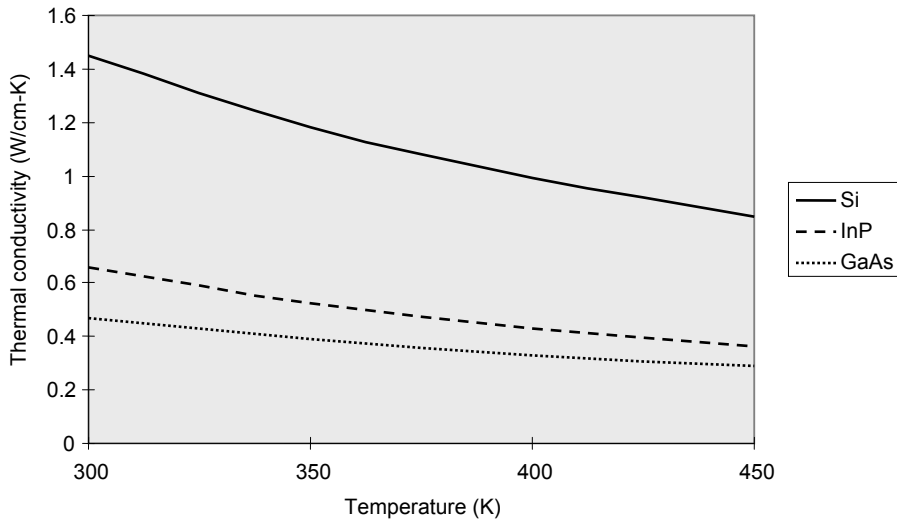
Figure 9.—Approximations for the thermal conductivities of Si, InP, and GaAs.

Figure 10 gives an indication of the differences between θ and T for our situation. The dotted curve is the actual temperature T versus θ for the specific form for $\kappa(T)$ given on the plot. The form is that for SiC, the best heat conductor of all considered substrates. The reference temperature is $T_o = 300$ K. A similar shaped (displaced) curve would occur for a different value for the reference. The lower line has unity slope that would correspond to the actual temperature equaling the transformed value (i.e., constant κ). It is there to aid the eye to show how rapidly the actual temperature climbs as the equivalent one increases. The increase above the $T = \theta$ line shows the effect of the decrease of $\kappa(T)$ from its value at T_o. For example, the conductivity at 300 K is 3.3 W/(cm·K). If the conductivity were constant at this value, the thermal resistance would be calculated with this value for κ. For a given heat flux, suppose one calculates
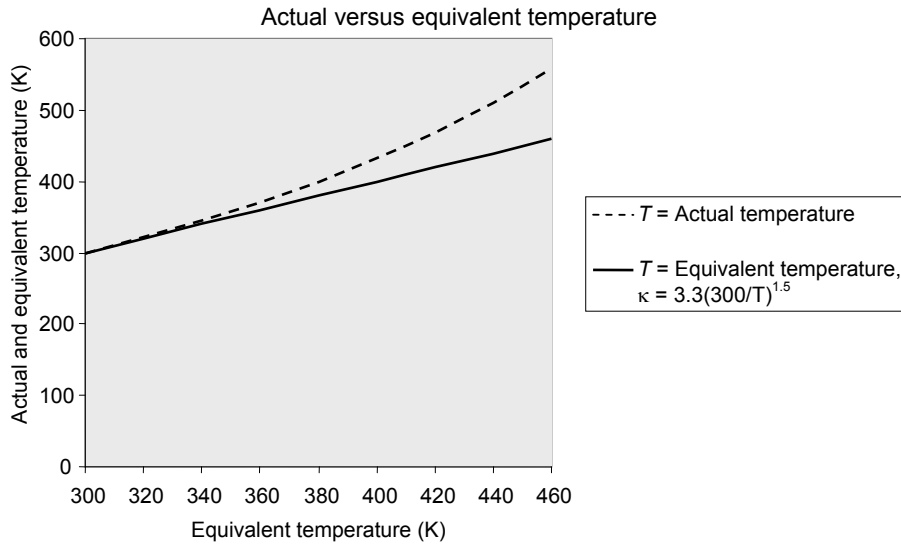
Figure 10.—Actual (*T*) and equivalent (θ) temperatures versus θ. The equivalent temperature graph is a straight line. The actual temperature curve (upper-most) is curved. The reference temperature is 300 K.

θ to be 450 K, then the actual value would be 534 K (see the plot). Observe the increase is 84 K, which is extremely large! This shows the need to include the variation of κ(*T*) in the calculation. One difficulty with the transform method is that jumps in the effective temperature occur at material interfaces, unless the forms for κ(*T*) satisfy certain constraints (ref. 54). The constraint is that the ratio of conductivities of adjacent layers must be independent of temperature. In other words, the nonlinearity in the basic heat equation is removed with the transform, but makes itself felt, and must be dealt with, in the boundary conditions. For our case of multiple layers and sequential calculation steps, we calculate the actual temperature in each layer, and thus avoid any complications.

The following table provides a compilation of reported values for thermal conductivities for components that are of interest to one studying the field of high temperature amplifiers.

TABLE 1.—THERMAL CONDUCTIVITIES FOR
MATERIALS USED IN HIGH POWER AMPLIFIERS

Material	κ(W/(cmK))
GaAs	$\kappa(T) = \kappa(300)(300/T)^{1.2}$ $\kappa(300) = 0.44$ $= 745\ T^{-1.3}$ $= 56\ T^{-0.87}$ 350 K< T < 500 K
SiC	$3.3(T_o/T)^{1.5}$ (doped) ~ 5 for S.I.
Si$_3$N$_4$	0.016
Sapphire (Al$_2$O$_3$)	$\kappa(300) = 0.25 - 0.5$ $\kappa(T) = \kappa(300)(T/T_o)^{0.8}$
Au	2.95 to 3.18
AuSn solder	0.573
Silver epoxy	0.0714 to 0.075
Epoxy cements	0.0188 to 0.0376
Solders	1.88 to 2.4
Copper	4
Si	$\kappa(T) = \kappa(300)(T/T_o)^{1.324}$ $= 1.54(300/T)^{4/3}$
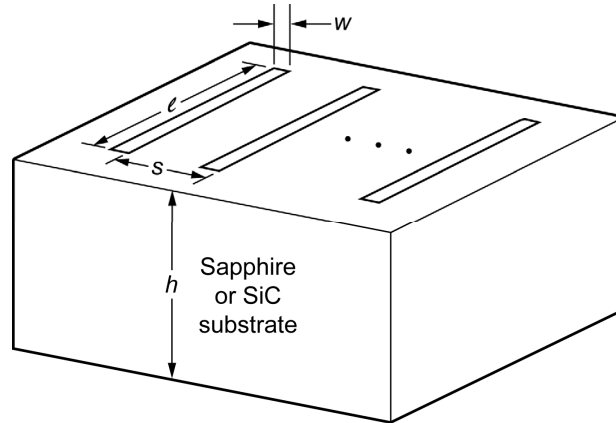
Figure 11.—Geometry for multiple gate (heat sources) on a substrate.

IV. Multiple Gate Thermal Resistance Via Multiconductor Coupling Model

The previous sections presented the accurate model from Masana for single stripes, and the two methods for multiple gates (Cooke and Darwish et al.). The equations of Cooke yield a single temperature, which is apparently an average value of all fingers involved. The formula is dependent on the number of gate fingers. Those of Darwish also give an average temperature, which is apparently that of the central region. The equation is assumed valid for a device with at least five fingers, as the number of fingers is not considered.

Since the layout of gates is similar to the arrangement of multiple conductors above a ground plane, concepts from multiple conductor theory should be applicable for our problem. The problem to be solved is the determination of R_{th} and temperature for each gate electrode as shown in figure 11. In general, the Source-Drain (S-D) spacing is much smaller than the separation between each S-D region, so the heat generated in each GaN section can be assumed to not couple to heat generated by adjacent sections in the uppermost part of the device. Therefore, we are considering rectangular sources (the appropriate footprints) on the substrate top surface. Once the temperature on this surface is determined, then similar calculations, as given previously, will determine the temperature at the channel. Recall the equation for steady state heat conduction (assume constant κ) is

$$\nabla^2 T = -\frac{g(x,y,z)}{\kappa}, \tag{25}$$

Where $g(x,y,z)$ is the heat generation function. Poisson's equation is $\nabla^2 V = -\frac{\rho(x,y,z)}{\in}$, and the similarities are obvious.

We will use developments in electrical theory to ascertain corresponding results for temperature. This is the same motivation utilized in Cooke's formula; his model uses the capacity for strips above a ground plane. For a finite number of conductors above a ground plane we know the charges and potentials are related by the Maxwell capacitance matrix $[C]$.

$$\begin{bmatrix} Q_1 \\ Q_2 \\ . \\ . \\ Q_N \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & . & . & C_{IN} \\ C_{21} & . & . & . & . \\ . & . & . & . & . \\ . & . & . & . & . \\ C_{N1} & . & . & . & C_{NN} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ . \\ . \\ V_N \end{bmatrix}$$

or

$$\begin{bmatrix} V \\ V_2 \\ . \\ . \\ V_N \end{bmatrix} = \begin{bmatrix} P_{11} & P_{12} & . & . & P_{1N} \\ P_{21} & . & . & . & . \\ . & . & . & . & . \\ . & . & . & . & . \\ P_{N1} & . & . & . & P_{NN} \end{bmatrix} \begin{bmatrix} Q_1 \\ Q_2 \\ . \\ . \\ Q_N \end{bmatrix}$$

where the matrix $[P]$ is the inverse of $[C]$, and is called the potential coefficient matrix. If the conductors are assumed to propagate a pure TEM mode, then an inductance matrix is defined where

$$[L][C] = \mu_\circ \in_\circ [I] \tag{26}$$

or

$$[L][C] = \mu_\circ \in_\circ \left[C^{-1}\right][I] = \mu_\circ \in_\circ [P]$$

or

$$[P] = \frac{1}{\mu_\circ \in_\circ}[L] \tag{27}$$

Now we make the analogy $V \leftrightarrow T$, $Q \leftrightarrow P_{diss}$ where P_{diss} is the dissipated power (no relation to the potential coefficient matrix). Now assume $p_{ij} \leftrightarrow R_{ij}$, where R_{ij} are the self and mutual coupling thermal resistances of the gates; then

$$\begin{bmatrix} T_1 \\ T_2 \\ . \\ . \\ T_N \end{bmatrix} = \begin{bmatrix} R_{11} & R_{12} & . & . & R_{IN} \\ R_{12} & . & . & . & . \\ . & . & . & . & . \\ . & . & . & . & . \\ R_{N1} & . & . & . & R_{NN} \end{bmatrix} \begin{bmatrix} P_{dISSI} \\ P_{dISS2} \\ . \\ . \\ P_{dISSN} \end{bmatrix} . \tag{28}$$

We assume all gates dissipate the same power, so the temperature on any gate is

$$T_k = (R_{k1} + R_{k2} + R_{k3} + \ldots + R_{kN})\, P_{dissk} \tag{29}$$

or just the sum of all thermal resistances in row k. Here P_{dissk} is the dissipated power in gate k, which is the same for all gates. We then assume

$$\frac{R_{11}}{R_{12}} = \frac{p_{11}}{p_{12}}, \tag{30}$$

that is, the ratios of the self and mutual terms are the same. This should be exact due to the analogy. We will determine R_{jj} for any single conductor; then scale all other R_{ij} accordingly. For our typical cases the parameter ranges are:

$$W \sim 24 \ \mu m \qquad h \sim 350 \ \mu m \qquad W/h \sim 7 \cdot 10^{-2} \qquad S/W \sim 2$$

$$S \sim 40 \ \mu m \qquad l \sim 200 \ \mu m \qquad l/h \sim 0.6 \qquad S/h \sim 0.1,$$

which are not typical for most microstrip coupled line structures.

Notice the thermal conductivity κ and ε correspond in the analogy. The analogy holds for homogenous materials, but for the inhomogeneous case, problems arise. Our case is inhomogeneous as we are assuming strips on a material with air above in the electrical case. The thermal case is that for finite thermal conductivity below the strips, but zero above. The electrical case cannot have zero for the permittivity of the air. Recall that microstrip is quasi-TEM and an effective permittivity ε_{re} is used. There are flux lines and potential contours in the air above the substrate, and ε_{re} is a measure of this effect. For the electrical case we have

$$\mu_o \varepsilon_o \varepsilon_{re} [P] = [L], \tag{31}$$

and thus we might replace κ of the substrate with some effective value. We don't have to deal with this however, as we are using ratios, and all terms carry the same κ. Actually the gate footprints on the substrate are about 1 μm below the actual air (i.e., beneath the GaN and AlN layers), so we can assume we are dealing with an almost completely homogeneous region. Then the analogy will hold, i.e., we are solving Laplace's equation in a source-free homogenous region. Recall that we use $\kappa(T_o)$ to treat the problem as linear, then obtain the true temperature via the Kirchhoff transform.

Our task is to determine the self and mutual inductance entries in the $[L]$ matrix

$$[L] = \begin{bmatrix} L_{11} & L_{12} & . & . & L_{1N} \\ L_{21} & . & . & . & . \\ . & . & . & . & . \\ . & . & . & . & . \\ L_{N1} & . & . & . & L_{NN} \end{bmatrix}. \tag{32}$$

Due to symmetry $L_{ij} = L_{ji}$ and for say a 5×5 array we have

$$[L] = \begin{bmatrix} L_{11} & L_{12} & L_{13} & L_{14} & L_{15} \\ L_{12} & L_{11} & L_{12} & L_{13} & L_{14} \\ L_{13} & L_{12} & L_{11} & L_{12} & L_{13} \\ L_{14} & L_{13} & L_{12} & L_{11} & L_{12} \\ L_{15} & L_{14} & L_{13} & L_{12} & L_{11} \end{bmatrix}. \tag{33}$$

Observe all entries on any diagonal (top left to bottom right) are the same. The actual determination of the L_{ij} is a complex problem. For one thing, inductance requires closed loops, whereas the $[L]$ entries which are in units of H/m are distributed values for assumed infinitely long lines. We choose two alternate methods to calculate $[L]$; the distributed, and the partial inductance approach. The partial inductances

depend on the length of the conductors as opposed to the distributed idea for infinitely long conductors. Therefore we are including the 3–D effect for heat emerging from the ends of the fingers.

For N circular wires spaced S meters apart, the self inductance L_{ii} and mutual inductances L_{ij} (distributed) are (refs. 55 and 56)

$$L_{ii} = \frac{\mu_\circ}{2\pi} \ell n\left(\frac{2h}{a}\right) \quad h\rangle\rangle a , \tag{34}$$

where a = radius, h = height above ground plane, and

$$L_{ij} = \frac{\mu_\circ}{4\pi} \ell n\left\{\frac{S_{ij}^2 + (2h)^2}{S_{ij}^2}\right\}. \tag{35}$$

For a 5 conductor array we have, $S_{12} = S$, $S_{13} = 2S$, $S_{14} = 3S$, $S_{15} = 4S$; thus

$$L_{12} = \frac{\mu_\circ}{4\pi} \ell n\left\{\frac{S^2 + (2h)^2}{S^2}\right\} \tag{36}$$

$$L_{13} = \frac{\mu_\circ}{4\pi} \ell n\left\{\frac{(2S)^2 + (2h)^2}{(2S)^2}\right\} \tag{37}$$

$$L_{14} = \frac{\mu_\circ}{4\pi} \ell n\left\{\frac{(3S)^2 + (2h)^2}{(3S)^2}\right\} \tag{38}$$

$$L_{15} = \frac{\mu_\circ}{4\pi} \ell n\left\{\frac{(4S)1 + (2h)^2}{(4S)^2}\right\}. \tag{39}$$

Due to symmetry of $[L]$, we need only generate the first row terms. Observe

$$L_{1k} = \frac{\mu_o}{4\pi} \ell n\left\{\frac{[(k-1)s]^2 + (2h)^2}{[(k-1)s]^2}\right\}. \tag{40}$$

For rectangular conductors:

$$L_{ii} = \frac{\mu_\circ}{2\pi} \ell n\left\{1 + 2\pi \frac{h}{(w+t)}\right\}, \tag{41}$$

where w = width of stripe, t = thickness, and

$$L_{ij} = \frac{\mu_\circ}{4\pi} \ell n\left\{\frac{S_{ij}^2 + \left[2\left(h + t/4\right)\right]^2}{S_{ij}^2}\right\}. \tag{42}$$

We can also use the self inductance of microstrip to express L_{ii},

$$L_{ii} = \frac{\mu_\circ}{4\pi} \ell n \left\{ 1 + 32 \left(\frac{h}{w}\right)^2 \left[1 + \sqrt{1 + \left(\frac{\pi w}{8h}\right)^2} \right] \right\}. \tag{43}$$

All of the above formulas are for external inductances, which should be appropriate for our case of widely separated gates. The previous formulas may be found scattered in the literature with slight modifications. One basic assumption is that L_{ij}, the mutual inductance between conductors i and j, depends only on the distance between them. The presence of the other conductors is ignored. Experimentally this has been verified, and for our case of not strong coupling, it should hold well. Numerical solutions in the literature shows the errors incurred with this assumption (ref. 56); and for our parameter ranges the errors are a few percent at most.

As stated earlier, our lines are not extremely long with respect to spacing and ground plane distance, so perhaps partial inductances could make for a better model. We choose only two forms; those for self and mutual inductances of rectangular conductors and filaments, respectively.

$$L_{ii}^p = 0.2\ell \left[\ell n \left(\frac{2\ell}{w+t}\right) + 0.5 + .2235 \frac{(w+t)}{\ell} \right] \mu H \tag{44}$$

$$L_{ij}^p = 0.2\ell \left[\ell n \left(\frac{\ell}{S_{ij}} + \sqrt{1 + \left(\frac{\ell}{S_{ij}}\right)^2} \right) - \sqrt{1 + \left(\frac{S_{ij}}{\ell}\right)^2} + \frac{S_{ij}}{\ell} \right] \mu H \tag{45}$$

Then the entries in the $[L]$ distributed matrix are (ref. 57)

$$L_{ij} = L_{ij}^p - L_{ik}^p - L_{kj}^p + L_{kk}^p \qquad\qquad i,j = 1,2,\ldots N \tag{46}$$
$$i,j \text{ not equal to } k,$$

where the superscript p means partial inductance value. For example see figure 12.

$$[L] = \begin{bmatrix} \left(L_{11}^p - L_{13}^p - L_{31}^p + L_{33}^p\right) & \left(L_{12}^p - L_{13}^p - L_{31}^p + L_{33}^p\right) \\ \left(L_{21}^p - L_{23}^p - L_{31}^p + L_{33}^p\right) & \left(L_{22}^p - L_{23}^p - L_{32}^p + L_{33}^p\right) \end{bmatrix} \tag{47}$$

For the ground plane partial self inductance L_{33}^p, we will use the image of a single conductor, i.e., 1 or 2.
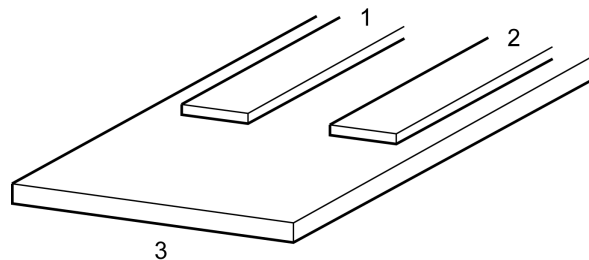
Figure 12.—Notation for calculation of self and mutual partial inductances for two conductors over a ground plane.

All of the equations presented in this section have been checked with reports in the literature (refs. 58 to 65), and we found good agreement in most cases. The worst cases were numerical simulations with tight coupling (not our case). For geometries close to our range (ref. 56), the error was ~3 percent.

V. Comparison of Analytical Models—Single Finger

This section compares the theoretical predictions for thermal resistance and channel temperature for single gate (finger) devices with the measurements of Kuball (ref. 15).

One Stripe on Sapphire

Kuball's group simultaneously measured the channel temperature using Raman spectroscopy and the I–V characteristics of AlGaN/GaN HEMTs. Figure 13 gives the schematic of a single 200 µm wide gate on a GaN layer grown on sapphire. The gate length is 4 µm. The source and drain pads are omitted for clarity, and their shape and presence did not have any affect on the channel temperature, as stated by the authors. The measured I–V characteristics are also shown.

Table 2 summarizes the measured channel temperature, the drain current, and the dissipated power, for several drain voltages V_d, all for the gate at 0 V. Notice that the dispersion in the data is from 10° to 20°. At the bottom of figure 13 is a schematic of the gate region with the temperatures at several points determined by simulation (which will be discussed in detail in section VIII) at $V_d = 20$ V. Observe the simulation values fall into the measured range of 179 to 190 °C.

TABLE 2.—DATA FOR A SINGLE STRIPE HEMT ON A SAPPHIRE SUBSTRATE

V_d, V	4	8	12	20
T, °C	40 to 60	80 to 95	120 to 140	179 to 190
$< T >$ avg. temperature	45	90	129	180
I_d, mA, drain current	39	42.5	39.5	32.5
P_{diss}, W, dissipated power	0.156	0.34	0.474	0.65
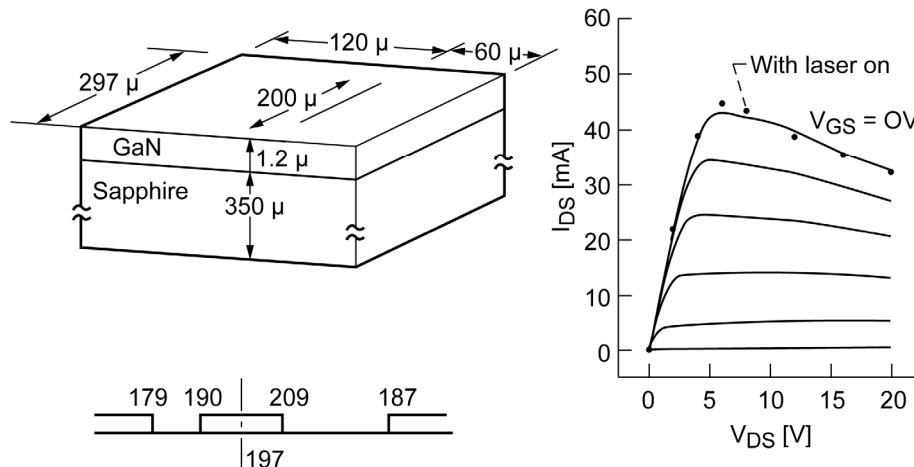
Figure 13.—Schematic of single gate HEMT and the measured I–V curves. Notice the gate is not centered on the chip.

The procedure to calculate the channel temperature is simplified by noting that over 95 percent of the thermal drop occurs in the sapphire substrate due to its thickness. The sapphire constitutes $350/351.2 = 99.7$ percent of the thickness of the device. The key step is the determination of the effective gate length footprint on the top surface of the sapphire. For this case the actual gate length is 4 μm. If we assume the heat is generated uniformly under the gate, and it diffuses downward at 45° angles from the gate edges, the footprint at the bottom of the GaN layer is 6.4 μm. The assumption of 45° implies no edge effects, so the heat moves away into an unbounded semi-infinite half-space. Now passing through the AlN region causes some change in the heat flow, and we obtain best results by assuming the footprint on the sapphire to be 6 μm. This focusing effect in the AlN is demonstrated in section VIII. The parameters in section III, the *Thermal Analysis Procedure,* section II, for this case are:

$$2l_x = 6 \text{ μm} \qquad\qquad \varepsilon_x = 0.943$$

$$2l_y = 200 \text{ μm} \qquad\qquad w = 350 \text{ μm}$$

$$2L_x = 180 \text{ μm}$$

$$2L_y = 300 \text{ μm.}$$

Then

$$W_n = 3.89$$

$$\gamma_\varepsilon = 33.3$$

$$\gamma_s = 1.67$$

$$l_{xn} = 0.033 \ \rho_s = 0.49/4 = 0.123,$$

where we assume the solder layer on the copper heatsink is so thin as to be negligible. The thermal conductivity of copper is taken to be 4 W/(cm K). We find $\alpha = 43.8°$, $\beta = 15.7°$, and $R_{th} = 174.3$ K/W. Table 3 provides the sensitivity of R_{th} for several effective footprints.

TABLE 3.—THE SENSITIVITY OF R_{th} AND THE SPREADING ANGLES
α AND β WITH THE FOOTPRINT ON THE SAPPHIRE LAYER

$2l_x$ (μm)	0.5	1.25	2	4	6	8
R_{th} (K/W)	294	248.6	226	193	174.3	161.7
α (°)	44.9	44.8	44.6	44.24	43.8	43.5
β (°)	15	15.1	15.7	15.7	15.7	15.7

    It will be shown later that only a few degrees are dropped across the GaN and AlN layers, so we can estimate R_{th} (sapphire) from the measured data. The procedure is the following. For the 4 V case the measured average channel temperature was 45 °C (318 K). Assume 2 °C dropped across the GaN and AlN layers, then the top of the substrate is at 316 K. Then the corresponding transformed temperature is therefore 315.6 K (from eq. (12)). The drop in the transformed temperature across the sapphire is thus 315.6 K – 300 K = 15.6 K. Then R_{th} (4 V) = $\Delta\theta/P_{diss}$ = 15.6 K/0.156 W = 100 K/W. Table 4 gives the results for all drain values.

TABLE 4.—THERMAL RESISTANCE AT SELECTED DRAIN VOLTAGES
EXTRACTED FROM MEASURED RESULTS OF KUBALL

V_d (V)	4	8	12	20
R_{th} (K/W)	100	163	182	188

Observe the average for the last three entries is 177.7 which is slightly less than 2 percent different from our calculated value. Using R_{th} = 174.3 K/W we find the channel temperature at V_d = 20V as follows. The linear drop across the sapphire is $\Delta\theta$ = (174.3) (0.65) = 113.3 K, so the top surface is at 300 + 113.3 K = 413.3 K. The actual temperature from equation (12) is 437.7 K (164.7 °C). For the 1.2 μm GaN channel with $2l_x$ = 4 μm and using κ(GaN) at 438 K, we obtain κ = 1.97(300/438)$^{0.48}$ = 1.64. Then the thermal resistance of the GaN layer is R_{th} = 6.1 K/W, and the change across the GaN is $\Delta\theta$ = (6.1) (0.65) = 3.79 K. Using equation (10) with T_o = 437.7 K, θ = 441.67 K, and r = 0.48 yields 441.6 K, or 168.6 °C. So the drop across the GaN layer is just 3.9° as anticipated. This final temperature compares favorably with the average of 180 °C of the measurements.

Table 5 summarizes the estimated temperatures for drain voltages of 4, 8, 12, and 20 V. Figure 14 is reproduced from Kuball's paper and shows the temperature measurements in the access regions about the gate. The circles to the right of the data in the gate – drain access region are the values given in table 5. The asterisks are the values in the channel region obtained by simulation. The uncertainty in Kuball's data was ±5 °C. We conclude that the outlined procedure works very well.

TABLE 5.—COMPARISON BETWEEN AVERAGE MEASURED CHANNEL
TEMPERATURES <T> AND CALCULATED ONES T_{calc} FOR
SINGLE STRIPE HEMT ON SAPPHIRE SUBSTRATE

V_d, V	4	8	12	20
<T>, °C	45	90	129	180
T_{calc}, °C	56	92	125	169
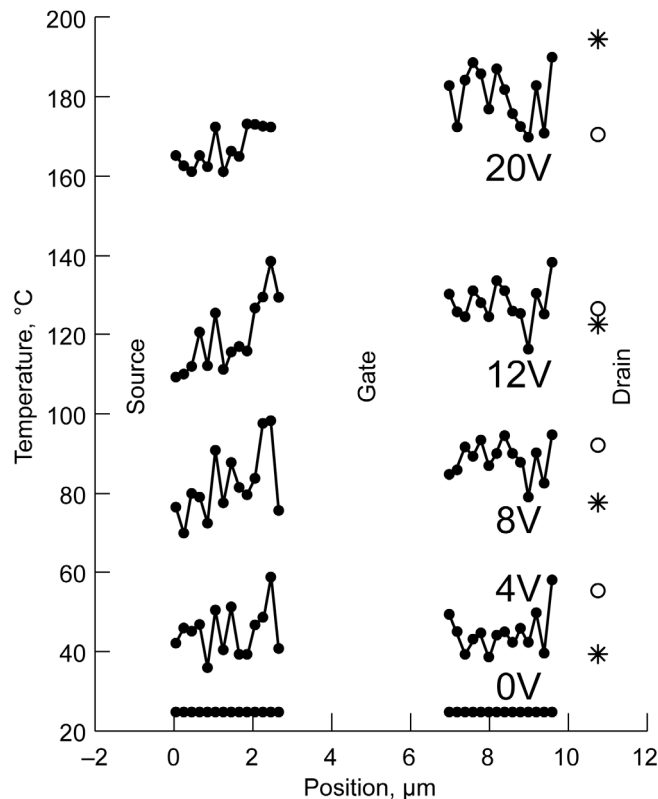
Figure 14.—The measured and calculated temperatures in the S-G and G-D access regions. The simulated values at the AlGaN/GaN junction are shown as asterisks at 4, 8, 12, and 20 V. The calculated values are the circles. The uncertainty of any measured value is 10 °C. (sapphire substrate).

At this point we discuss some of the problems associated with this series of publications. For the results in these papers, the heat sink was not held at room temperature, but allowed to rise as the dissipated power increased. Thus the measured channel temperature value includes the thermal rises across the layers along with the unknown reference temperature of the sink. For the sapphire case the edge went up about 20 °C. Kuball states we can assume the sink rose by that amount. Our calculated temperature is about 12° low, which we can surmise is due to the fact that we assumed the sink to remain at room temperature (27 °C). The data in (ref. 18) suggest that the sink rose to 40 °C, which would boost our values approximately 13°! Then we would agree to within 1°, which of course is beyond our anticipated accuracy. Nevertheless, we can apparently get rather good results with judicious approximations. Kuball states his system accuracy to be within 10 °C.

Now κ_{AlN} is temperature independent and we assume its value to be 0.1. This is about 1/10th of its bulk value, but typical for thin films grown on sapphire or SiC. As a matter of fact, the authors in (ref. 66) have reported measurements that show the thermal conductivity may be two orders of magnitude below the bulk value, when grown on Silicon. Kuzmik et al. (ref. 67) have used different values for κ_{AlN} in simulations, depending on the layer upon which it was grown. Since we do not know the specifics of their AlN layer, some small error exists. However, the thermal resistance formula is insensitive to ρ_s, so the error should be very small. Assuming a parallel isotherm flow pattern in the AlN, (and the thickness to be 0.015 μm) we obtain R_{th} (AlN) = 0.75 K/W, with a corresponding thermal drop of 0.49°; which we have neglected.

While we have been able to get results that agree with Kuball's data, we still have some reservations. The first issue is the reliability of the measurements. In a recent paper (ref. 68) concerning the measurement of temperature in AlGaN/GaN devices using Raman scattering, it was shown that very different results are obtained when different phonon lines are observed. Specifically, the UV line recorded temperatures which were consistently higher by as much as 70 °C as that found using a line in the visible. The reason is the depth of penetration of the light into the sample. For a device similar to the one investigated here, the difference in measured temperature was about 70 °C for the dissipated power of 0.65 W. Kuball's group used the line in the visible, which averages the temperature in the GaN.

Table 6 compares the thermal resistances calculated by the equations of Masana along with the corresponding channel temperatures. In these calculations we used the following approach. First start with the actual gate length and calculate the thermal resistance using the room temperature value for thermal conductivity. Use the calculated spreading angles to determine the footprint. Calculate the substrate thermal resistance. Then calculate the temperature rise across both layers using the dissipated power. Next recalculate R_{th} using the values of κ corresponding to the average of its values at the new temperature and room temperature. Then calculate the channel temperature.

TABLE 6.—THERMAL RESISTANCES AND RESULTING CHANNEL
TEMPERATURES USING THE EQUATIONS OF MASANA

V_d, V	P_{diss}, W	R_{th} (GaN), K/W	R_{th} (sapp), K/W	T_{ch}, °C
4	0.156	5.37	165.4	53.6
8	0.34	5.62	172.3	87.5
12	0.474	5.81	176.8	113.6
20	0.65	6.06	182.6	149.6

Table 7 shows the results of a similar calculation, this time using the equations of Cooke. In this case we assume the spreading angles are 45°, since the edges are sufficiently far away. The final footprints in the two calculations are 4.064×203.15 versus 6.4×202.4 μm². The final channel temperatures are 149.6 and 93.4 °C, a difference of 56.2°, which we consider significant. Observe they differ from that in table 5 by unacceptable amounts.

TABLE 7.—THERMAL RESISTANCES AND RESULTING CHANNEL
TEMPERATURES USING THE EQUATIONS OF COOKE

V_d, V	P_{diss}, W	R_{th} (GaN), K/W	R_{th} (sapp), K/W	T_{ch}, °C
4	0.156	3.47	92.5	42
8	0.34	3.56	94.6	60.4
12	0.474	3.63	96.5	74.8
20	0.65	3.72	98.4	93.4

VI. Comparison Between Darwish et al., and the GRC-1 Model

The previous section compared the predictions of Masana and Cooke for the thermal resistance of a single gate. Masana's equations are only valid for a single gate, whereas those for Cooke are valid for either single or multiple gates. The formulas by Darwish, et al. (ref. 45) are only valid for the multiple gate case, and should be accurate for about five or more gates. The multi-conductor method of section IV should be applicable to either single or multiple gate cases. For brevity we will call the analysis method and final equation by Darwish, the one-shot result. The iterative approach, which uses Masana's equations for the single gate where appropriate (in the GaN layer), and Cooke's equation for the multiple gate case (in the substrate) will be labeled the GRC-1 method. The results from the multi-conductor equations will just be called the multi-conductor results.

As stated previously the models are complementary, but they can be compared in their regions of overlap. We will determine a value for R_{th} for the following data set:

$$L_g = 2l_x = 0.25 \ \mu m$$

$$W_g = 2l_y = 250 \ \mu m$$

$$t_{GaN} = 1 \ \mu m$$

$$t_{SiC} = 100 \ \mu m$$

$$S = 40 \ \mu m$$

$$\kappa_{SiC} = 3.3 \ W/(cm \cdot K)$$

$$\kappa_{GaN} = 1.5 \ W/(cm \cdot K).$$

which is that given in (ref. 45) as an example, and plotted in their figure 4. The one-shot method finds the thermal resistance of the GaN layer (region 1) to be $\Theta_f=13.82$ K/W, and that for the two portions of region 2 to be 19.37 and 19.95 K/W. The total resistance is 53.1 K/W, which agrees exactly with the plotted curve in their figure 4, which is reproduced here as figure 15(a). The figure shows nearly perfect correlation between the analytical calculation and the finite element results. The GRC-1 method obtains R_{th} in the GaN to be 30 K/W. This is assumed to be valid as the gates are separated by 40 μm, and will not interact in the 1 μm GaN layer. We have some leeway on the calculation of the thermal resistance of the SiC layer. Since the thickness is 100 μm and the spacing between fingers is 40 μm, and if we assume spreading is at 45°, then each finger interacts with four of its neighbors (two on each side). Using Cooke's formula, the resistance of the SiC layer changes from $R_{th}=21$ to 28.7 K/W, as the number of fingers varies from 1 to 20. Then the total resistance is 30 +(21 thru 28.7) = 51 thru 58.7 K/W. If we use Masana's equation for a single finger, we obtain $R_{th}=24$ K/W. The total resistance is now 30 + 24 = 54 K/W, see figure 15(b), which agrees closely with the previously found value from Darwish (53.1 K/W). While we hope for agreement, this result is surprising, and we are not sure if this is just a coincidence for this particular case. The fact that they give different values for the GaN and SiC layers, yet the total is the same, is unclear. The determination of the channel temperature is different for the one-shot versus the other two methods. For example; the temperature change for the one-shot case is $(R_{th})(P_{diss})(n)$ where P_{diss} is the power dissipated per gate, and n is the number of gates. For n varying from 5 to 15 with P_{diss} assumed to be 1.0 W, the channel temperature is shown in figure 15(c). The temperature varies from 286 to 817 °C.
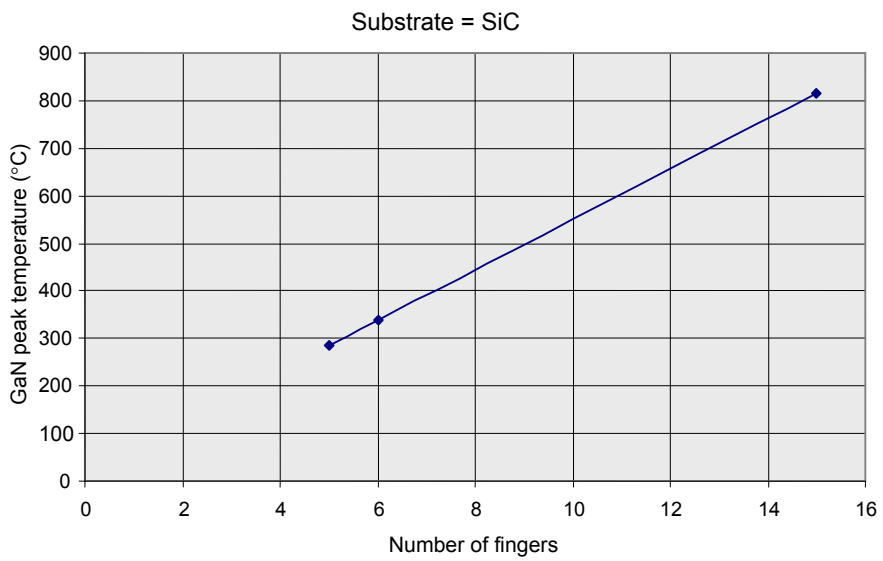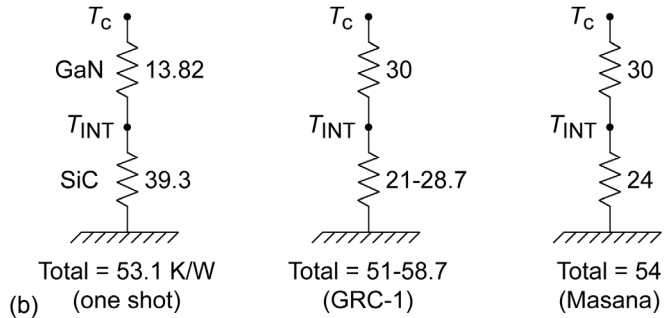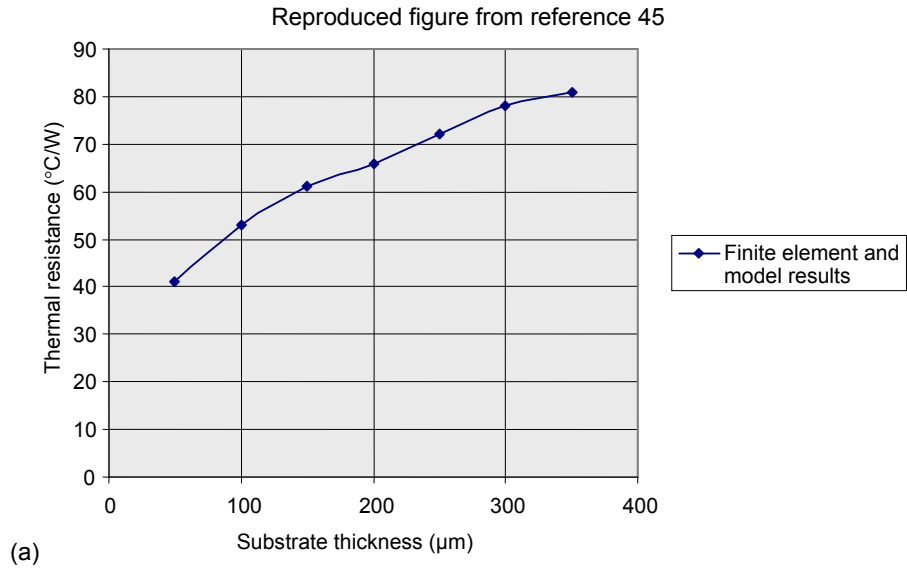
Figure 15.—(a) Reproduced figure from reference 45; showing the excellent agreement between the finite element code and their model's results. (b) Observe that all three models give the same net thermal resistance; however, the distribution over the GaN and SiC layers in the one-shot case is very different. (c) The channel temperature from the one-shot calculation.

The GRC-1 and Mansana (only) method calculates the channel temperatures as follows. Assume the dissipated power is 4 W/mm, and each finger is 0.25 mm wide; thus the power dissipated per finger is 1.0 W. The temperature change across the channel $\Delta T_{ch} = R_{th}(\text{GaN})(1.0 \text{ W})$, and that across the substrate is $R_{th}(\text{SiC})(P_{diss})(n)$. The final channel temperature T_{ch} is the sum of the changes across the substrate and channel +20 °C. Figure 16 gives the interface temperature as the number of fingers varies from 1 to 16, while figure 17 gives the corresponding channel temperature. The upper curve, (one-shot), is derived from the one-shot calculation, while the lower two curves are for Masana's equations in the GaN and Cooke's in the SiC, or Masana's in both layers (neglecting any crosstalk in the SiC layer) respectively. Observe that this channel temperature calculation procedure gives the range of 270 to 663 °C as the number of fingers varies from 6 to 16 for the one-shot case. The upper temperature is around 150 °C lower for this case than the previous method. Table 8 summarizes the temperatures at the GaN/SiC interface and the channel, which are shown in figures 16 and 17.
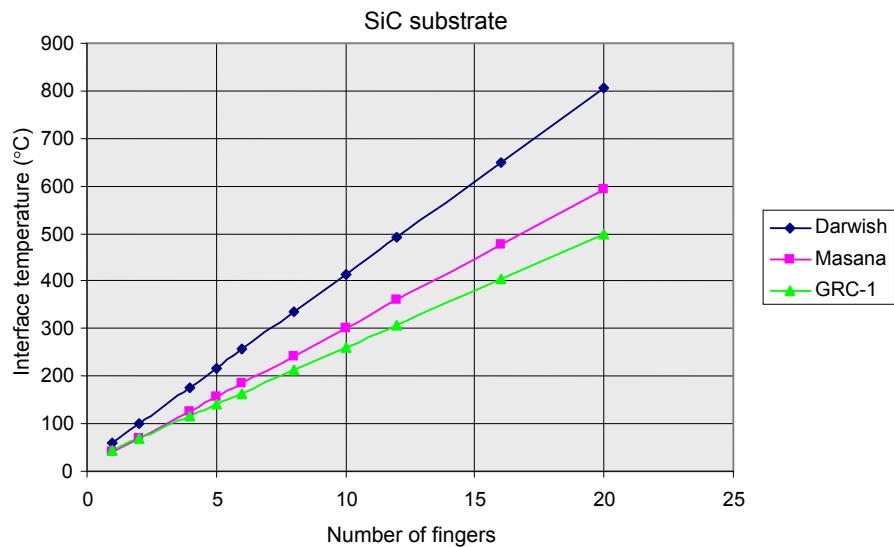
Figure 16.—Interface temperature rise as the number of fingers increases. The base is held at 20 °C.
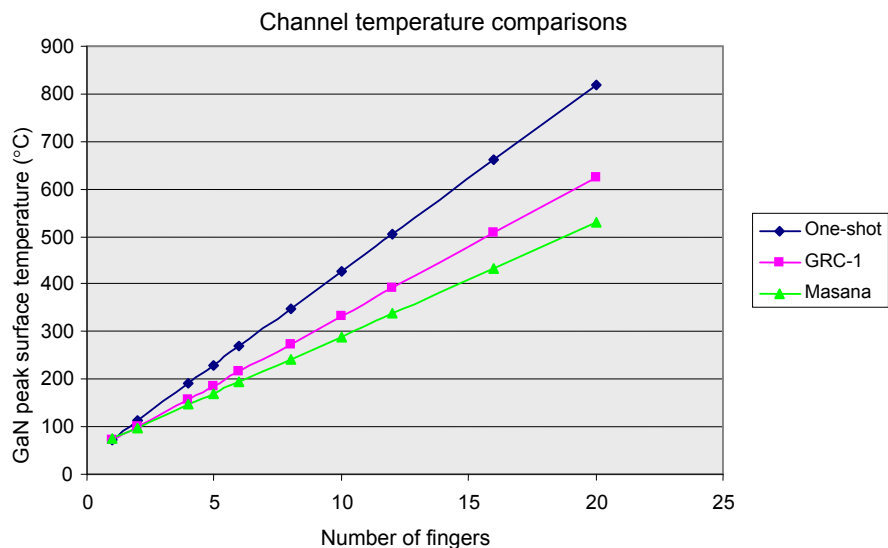
Figure 17.—Corresponding increase in channel temperature with change in the number of fingers.

TABLE 8.—INTERFACE AND CHANNEL TEMPERATURES (°C) FOR A GIVEN
DATA SET AS COMPUTED BY THREE DIFFERENT METHODS. THEY ARE:
MASANA ONLY (M), GRC-1, AND ONE-SHOT RESPECTIVELY

n	T_{int}	T_{int}	T_{int}	T_{ch}	T_{ch}	T_{ch}
	M	GRC-1	One-shot	M	GRC-1	One-shot
1	44	41	59	74	71	73
2	68	69	99	98	99	112
4	116	127	177	146	157	191
5	140	156	216	170	186	230
6	164	185	256	194	215	270
8	212	243	334	242	273	348
10	260	302	413	290	332	427
12	308	361	492	338	391	505
16	404	478	649	434	508	663
20	500	594	806	530	624	820

Before considering more comparisons with published results, we discuss the various functional dependencies upon which the thermal resistance depends. One may write the thermal resistance as follows.

$$R_{th} = f(t_{GaN}, t_{sub}, \kappa^{GaN}(T), \kappa^{sub}(T), W_g, l_x, n, S)$$

The eight parameters are the GaN and substrate thicknesses, their thermal conductivities, the gate width (per finger), the gate length, the number of fingers, and their separation. In general, R_{th} decreases with increasing W_g, increasing S, and increasing l_x. It increases with increasing substrate thickness, and with the number of fingers, n. The strength of the variations depends on the geometry and the heat generation function $g(x,y,z)$.

The paper by Bertilsson et al. (ref. 8) concerning lattice heating in SiC MESFETs is illuminating for our purposes. Their figure 4 gives normalized thermal resistance versus finger width W_g, n, and S. The reference values are 200, 10, and 100 μm respectively. Figure 18 gives R_{th} (normalized to the gate width) as a function of the number of fingers, with the gate length ($2l_x$) as a parameter. The physical gate length was 0.5 μm, and the active layers constituted 1.38 μm. Using the footprint method, we determine the effective gate length on the SiC substrate to be 3.26 μm. The curve labeled reference 8 is extracted from figure 4 of the paper. The curve below it is that derived using the GRC-1 method, with gate length = 3.26 μm. We consider the agreement to be excellent. The two upper curves show the result if the actual gate length, or the gate-drain spacing is used. This reveals the sensitivity to gate length as well as the agreement obtained using the actual length and determining its footprint. For the given gate length of 0.5 μm, the one-shot methods gives the value of 9.6 K-mm/W. The agreement of both methods with the reference 8 results is aided in part by the thermal conductivity being the same in all regions; the 1.38 μm epitaxial layer and the 330 μm substrate. Figure 19 gives the variation of the thermal resistance with gate pitch S; the diamonds are from reference 8, and the squares are the GRC-1 results. Some values obtained with the one-shot method are stated in the caption. Figure 20 depicts the dependence on gate width; the triangles show the GRC-1 result, and one-shot values are stated in the caption. The denormalized thermal resistance curve shows the true decrease with gate width. The one-shot results match the normalized curve closely, but the GRC-1 curve is too flat.
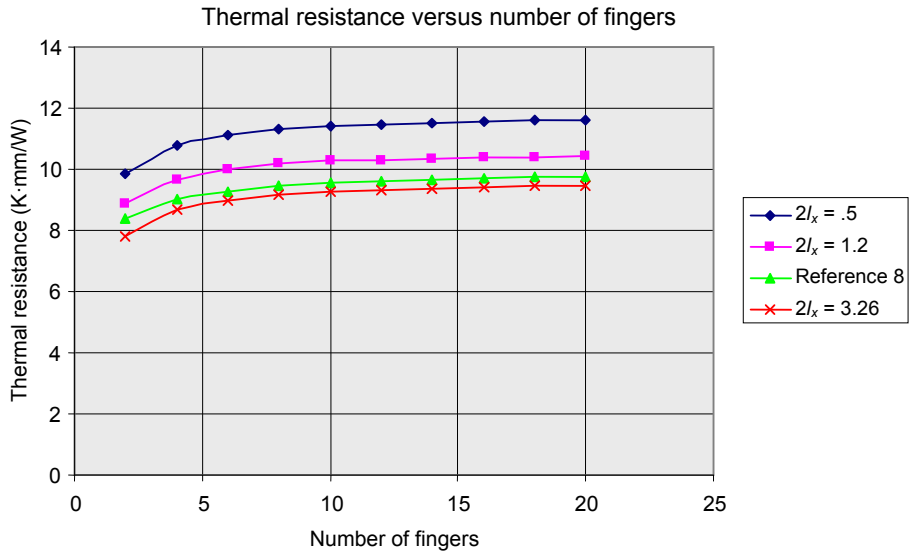
Figure 18.—R_{th} versus the number of gate fingers for different gate lengths ($2l_x$), based on simulations by Bertilsson (ref. 8). The value predicted by Darwish is 9.6 K·mm/W (independent of the number of fingers).
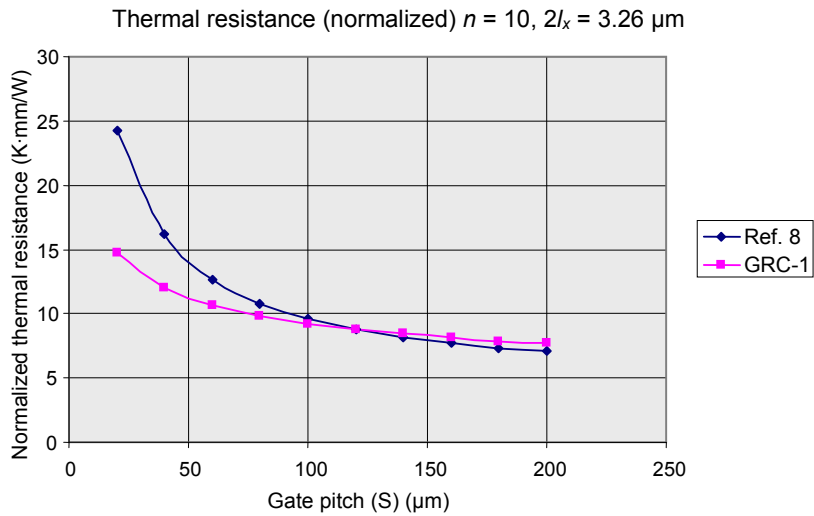

Figure 19.—Variation of R_{th} (normalized) with gate pitch. The values by Darwish are 28.1, 9.6, and 7.7 at S = 20, 100, and 200 µm, respectively.

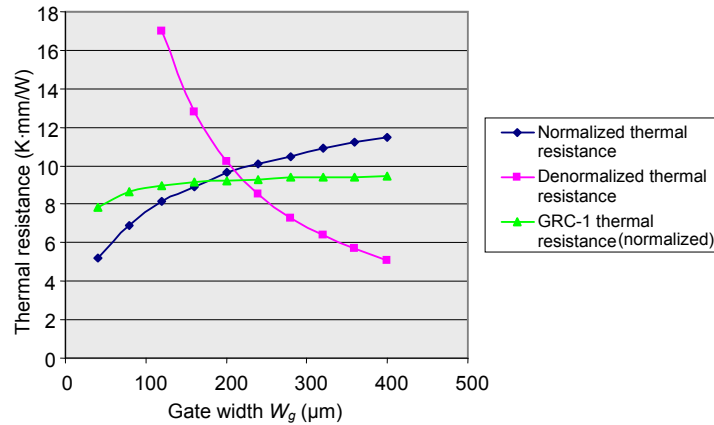Normalized and denormalized thermal resistance versus gate width

Figure 20.—Change in R_{th} (normalized) (diamonds), and denormalized
(squares) with gate width W_g. Here n = 10 and $2l_x$ = 3.26 μm. The
values from Darwish are 6.3, 9.6, and 11.4 at W_g = 40, 200, and
400 μm, respectively.

The next comparison considers the work from Nuttinck et al. (ref. 19). This is one of the few papers wherein the variation with the number of fingers has been shown. The results are those from a simulation, thus we must proceed with some caution. First of all, some of the dimensions, values used for thermal conductivity, etc., were not given, but from study of other publications by the authors, we have been able to develop a reasonable interpretation of their results. In figure 21 the dimensions of the device are shown schematically. The configuration is highly asymmetrical as the source-gate separation is only 0.1 μm, whereas the gate-drain spacing is 3 μm. The thermal conductivity for SiC at 300 K was assumed to be 3.9 (from one of their other publications). The remaining ones were chosen to be typical values. The simulated channel temperature versus the number of fingers is given in figure 22. Notice the temperature increases linearly as n varies from 1 to 8. However, the value at n=16 falls well below an extrapolated value from the line developed for small n. Apparently the temperature given is that of the center finger, and the authors state that above 10 to 12 fingers, additional fingers do not lead to a significant modification of the horizontal heat flow. After 14 fingers, a plateau is reached. Apparently this plateau is the value that the one-shot calculation should produce. We choose n=6 for the one-shot calculation. At that point the channel temperature is 435 K and the thermal conductivity of GaN is calculated to be 1.65. The thermal resistance for the GaN layer is found to be 41.3 K/W. For the SiC layer we find it to be 100.6 K/W. The ratio of thermal resistances is then 0.41. From the transient simulation reported in (ref. 69), that ratio was 0.6. Using the total thermal resistance of 141.9 K/W, and the dissipated power of 0.625 W/finger, the calculated channel temperature is (lower value method) 41.3 × 0.625 + 100.6 × 6 × 0.625 + 20 = 423 °C. Then for n=12 we have 800 °C. These are very high compared with the simulations. The GRC-1 method gives thermal resistances of 66.6 for GaN and 34 to 72 for SiC as n varies from 1 to 16. Figure 23 summarizes these calculations. The prediction of the channel temperature for the GRC-1 method is also shown as the line in figure 22. Both calculations do not correlate well with the simulated curve. However, we can get complete correlation with the GRC-1 method in the following way. Starting with the single finger case we obtain the footprint at the GaN/SiC interface to be 8.35×127 μm². Then with the data set obtained from their publications, we calculate R_{th} for the SiC as follows:

$$2l_x = 8.35 \text{ μm}$$

$$2l_y = 127 \ \mu\text{m}$$

$$2L_x = 590 \ \mu\text{m}$$

$$2L_y = 278 \ \mu\text{m}$$

$$W = 330 \ \mu\text{m}$$

$$\rho_s = 3.9/2.4 = 1.625$$

$$\gamma_e = 15.2$$

$$\gamma_s = 0.47.$$
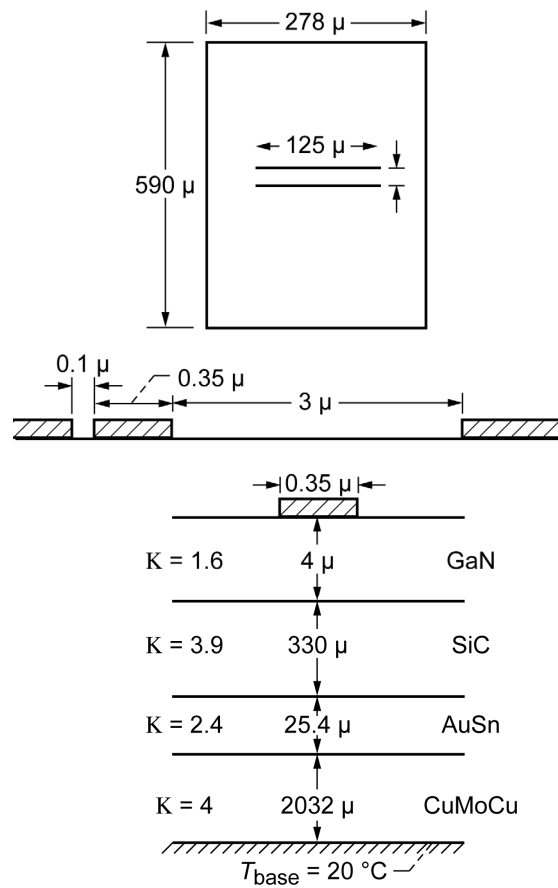
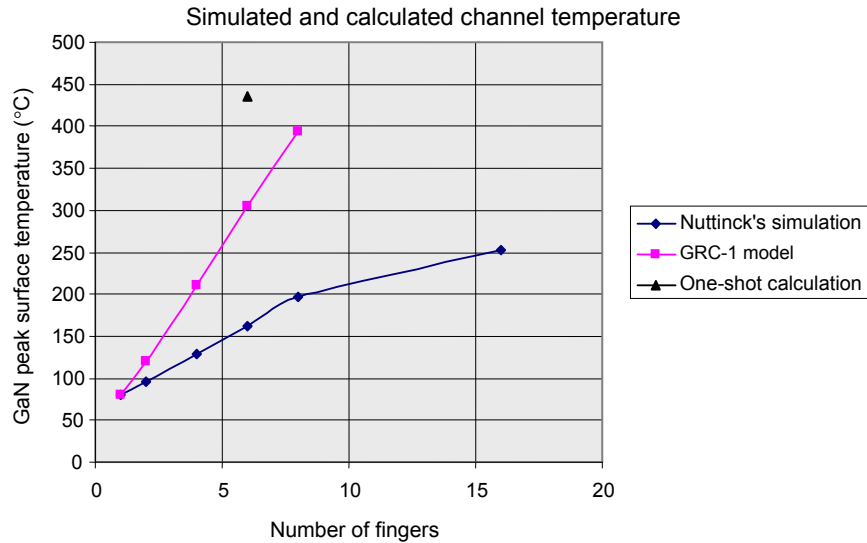Figure 21.—Top and cross-sectional views of device simulated by Nuttinck et al. (ref. 19).

Figure 22.—Channel temperature of simulated device. The lower curve is derived from Nuttinck's simulation. The straight line is the GRC-1 prediction, while the single point ($n = 6$, $T = 435$) is the one-shot prediction.
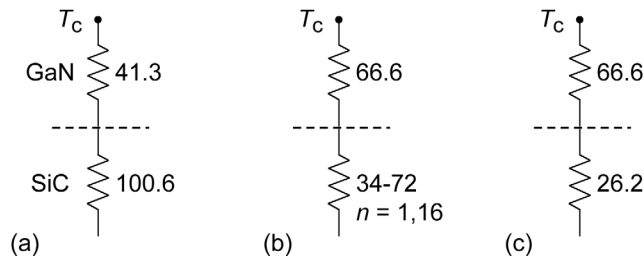

Figure 23.—(a) Is the resistance stack calculation by the one-shot procedure. (b) Is that for the GRC-1 method. (c) Masana's method, neglecting cross-talk in SiC.

We obtain the thermal resistance for SiC to be 26.2 °C/W. The temperature determined by the simulator was 78 °C, and subtracting the base plate value of 20 °C, yields a net drop across both the GaN and SiC layers to be 58 °C. The drop across the SiC is calculated to be $26.2 \times 0.625 = 16.4$ °C. Therefore the drop across the GaN is 41.6 °C. This gives the thermal resistance across the GaN the value 66.56 °C/W, with corresponding thermal conductivity 1.8 W/(cm·K). This value is well within the range for GaN. Now assuming the change in temperature drop across the GaN is constant as the number of fingers increases (since the fingers are sufficiently separated to eliminate any cross-talk in the GaN). We obtain the following equation for the channel temperature:

$$T_{ch} = R_{th}(n)\,(0.625)n + 20 + 41.6.$$

Using the simulated temperatures with n, we obtain $R_{th}(n)$ in the SiC. From these we calculate the required values of thermal conductivity as a function of temperature. The values needed are shown on the solid curve (squares) in figure 24. This curve is reasonably close to the average one shown. The four values at 300 K obtained in the literature show the large dispersion one may expect. Comparison with figure 22, where constant κ_{SiC} was used, shows how critical the correct value for $\kappa(T)$ for any layer must be in order to match measured or simulated results. As stated earlier, this data on the thermal conductivities is not known precisely, which hampers any analytical scheme.

Approximations for SiC thermal conductivity
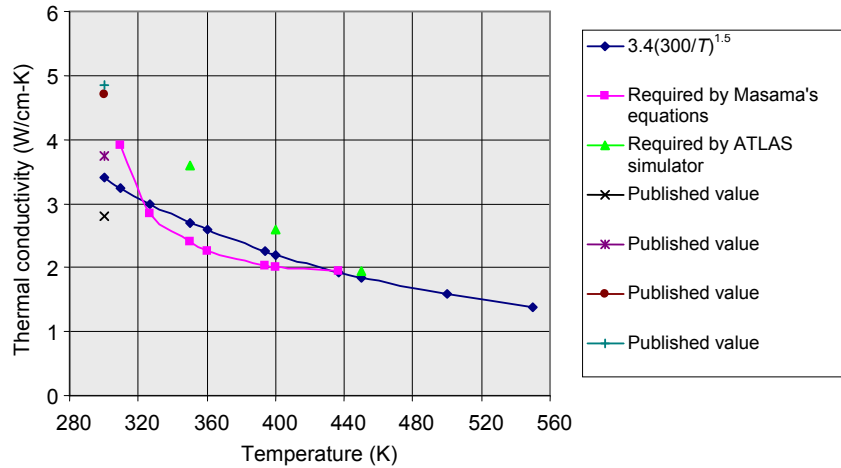
Figure 24.—Composite of thermal conductivity of SiC. The multiple values at
300 K are 2.8, 3.75, 4.7, and 4.85 are those found in the literature.

VII. 2–D Silvaco—Atlas Simulations (Basic Information)

This section encompasses the material parameter sets and computational models used in the 2–D simulations. The version of ATLAS used was 5.8.3.R. The flags set were Fermi-Dirac statistics, bandgap narrowing, field dependent mobility, SRH generation/recombination, and lattice temperature. Impact ionization and tunneling were not allowed, the drift-diffusion option was used, and the baseplate temperature was 300 K. No traps were included. At the present time, the information on traps is not precise, and a wide range of parameters describing them exists. The physical location, capture cross-sections, energy levels, and densities are widely dispersed; and the trap signatures depend on many process steps, as well as the growth mechanism, and the substrate. Therefore, we felt including them into the model at this time would overly complicate an already very complex model. In most cases, the electric field strength was below the critical field for ionization, so we don't think turning off that option caused significant errors. The boundary conditions were the default provided by ATLAS, the Fermi level was not pinned, as no surface charges, or traps were included. For any parameter not mentioned in the text, the default was used.

The model was developed with internal self-consistency as a primary goal. We attempted to stay within the ranges found in the literature whenever possible. However, the ranges are wide, due to the large number of parameters available for the devices. We chose values specifically for comparison with the experimental results of Kuball et al. (refs. 15 to 18), wherein both measured I–V characteristics and channel temperatures for several drain bias voltages were given. Their work was unique in that both accurate self-consistent electrical and thermal information was provided. On the other hand, many of the key parameters needed to start a simulation were not given. The chip dimensions, 2DEG sheet density, and low field mobilities were given. The mobilities were 1560 and 1900 cm^2/V-sec for sapphire and SiC respectively. A common electron sheet density of 7.5×10^{12} cm^{-2} was specified. The doping levels were not specified, so we adjusted them in the simulation to permit best fitting of both current and temperature data.

The device cross-section is shown in figure 25. Starting at the top, it consists of two $Al_{.2}Ga_{.8}N$ layers; the upper and lower ones are 230 and 50 Å thick respectively. Their doping is 2×10^{18} and 1×10^{15} donors per cm^3, respectively. The highly doped layer serves as the carrier supply source. The field at the AlGaN/GaN interface due to both the spontaneous and piezoelectric polarization is modeled by a positive sheet charge $\sigma_s = 1\times10^{13}$ and 0.7×10^{13} charges per cm^2 for GaN grown on sapphire or SiC respectively. These values were chosen by trial and error. Observe the magnitude value for SiC is very close to the

S   G   D

μ = 600   230 Å   Al$_{0.2}$ Ga$_{0.8}$ N

50 Å   Al$_{0.2}$ Ga$_{0.8}$ N
σ$_s$ + + + + + + + + +   + + + + +
2 deg channel   20 Å   GaN
Transition   10 Å
Smoothing   2 Å
μ = 900 bulk GaN

μ = 1560 sapphire   μ = 2000 SiC
     1500   1900
1 Å 1440   1800
     1380   1700
     1320   1600
     1260   Transition   1500
     1200   1400
     1140   1300
     1080   1200
     1020   1100
      960   1000

2 Å   900   900
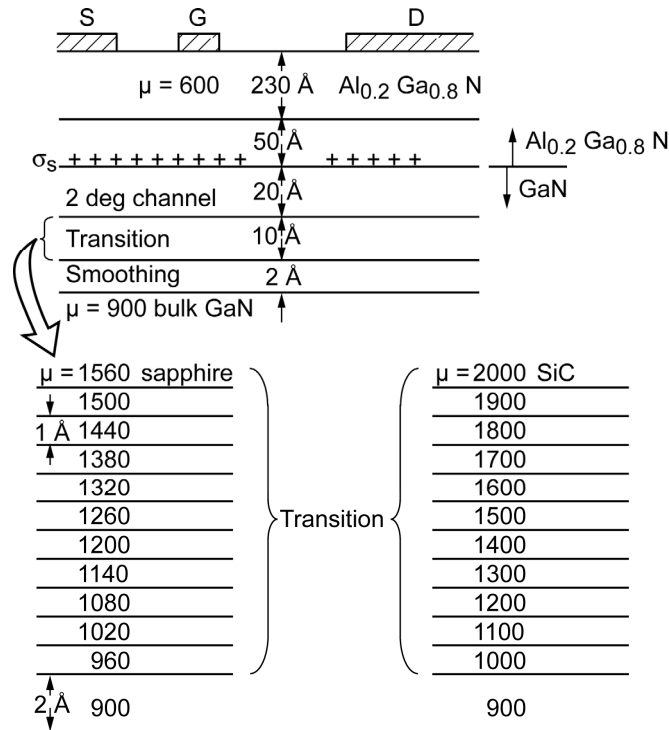
Figure 25.—Schematic (not to scale) of simulated devices.
Figure 26 gives additional information.

value for the sheet density given by Kuball. This approximation has been used by several authors in the literature (see for example (ref. 31)) with apparent success. In principle, the bound charge due to the polarization is a distributed effect; but incorporating this with the available options in the code is not straightforward. Due to excellent agreement with published data, we think the single sheet model is adequate for our purposes. The strain state of the GaN is different, depending on the substrate, thus the different sheet values. When GaN is grown by MOCVD it is in compression/tension depending on the substrate being either sapphire/SiC respectively. This difference may cause the polarization effects, and traps, to be different. Due in part to these differences, our discussion is separated into two parts; one for sapphire and one for SiC.

The sheet charge values were assumed constant with position along the channel for all gate and drain voltages and temperatures. Experimentally, n_s the negative charge density existing in the channel, that partially shields the fixed positive sheet charge density, decreases with increasing temperature. This may or may not reflect changes in the sheet charge value. We have neglected this effect. The simulated saturated drain current reduced by ~10 and 11 percent as the sheet charge was reduced by factors of 5 and 50 respectively. The sheet charge and the alignment parameter for conduction band edges provided a reasonable band shape near the AlGaN/GaN heterojunction. We assume any excess charge, or interface dipoles that may be present in the actual device; are adequately modeled by the alignment parameter and sheet charge. The position of this charge sheet is important; and we get best results when it is directly at the physical heterojunction. In actual devices, the surface passivation is a critical process; as much of the dispersive behavior is dependent on the charge state in and around the passivation layer. We have omitted any charge build-up on the surface, or in the AlGaN. We have also neglected possible conduction paths near the GaN/AlN interface. However, we have assumed the AlN to have a doping level the same as the bulk GaN layer. The underlying sapphire or SiC substrates have been assumed completely insulating.

The 2DEG channel (defined by high mobility and specific variation with temperature) was modeled as a layer 20 Å thick. Below the channel is a 10 Å transition layer. This layer is further partitioned into ten 1 Å layers; wherein the mobilities transition from the channel to the bulk values. Finally, a 2 Å smoothing layer with the bulk mobility is below the transition layer. Originally this layer was just a

placeholder. The mobility values used in the transition layer are listed in the expanded portion of the figure. Below this layer is the large bulk GaN layer. Table 9 provides the dimensions for the source, gate, and drain pads and their separations.

TABLE 9.—DIMENSIONS OF SOURCE, GATE, AND DRAIN PADS FOR THE BASIC DEVICE

Element dimensions, μm	Sapphire substrate	SiC substrate
Source pad	50	50
Gate length	4	1
Drain pad	50	50
S-G spacing	3	1
G-D spacing	3	2
Overhang (semiconductor) beyond drain edge	10	10

The simulated device of figure 25 is 1 μm deep (into the page), and the results are scaled to the full width of 200 μm (done internally in ATLAS). The minimum grid spacing in the x and y-directions was 0.1 μm and 1.0 Å, respectively. The fine mesh in the y-direction was in and about the channel layer. The number of grid points for the sapphire and SiC substrate cases were 19,968 and 15,808. The maximum number allowed was 20,000. For our simulations the density of points was the same; the larger number in the sapphire case was due to the device just being larger. Some parameter values used are listed in table 10.

TABLE 10.—PARAMETERS FOR THE PRIMARY LAYERS OF THE HEMTS

Parameter	Al_2Ga_8N	GaN	AlN	SiC
E_g, eV	3.96	3.4	6.14	3.34
N_c, cm^{-3}	2.07×10^{18}	1.07×10^{18}		
N_v, cm^{-3}	1.16×10^{19}	1.16×10^{19}		
E_d, eV	0.044	0.044		0.0518
E_a, eV	0.045	0.045		0.195
ε_r	9.5	9.5	10.4	9.66
N_d, cm^{-3}	2×10^{18} upper 1×10^{15} lower	1.0×10^{15}	1.0×10^{15}	0.0
V_{sat}, cm/s	1.12×10^7	2×10^7		

The Schottky barrier height was 4.5 eV for all cases, on both substrates. We swept its value from 4 to 5, and settled on 4.5. The corresponding surface densities n_s were 7.4, 7.9, and 8.13×10^{12} cm^{-2} respectively. This was performed at the gate center.

As noted in previous sections, the thermal conductivity values are critical, as the developed temperature due to self-heating is very sensitive to the value for $\kappa(T)$. Table 11 gives the information concerning the $\kappa(T)$ specifications. The thermal conductivities for air above the device, the contact pads, and the AlGaN were $2.7 \cdot 10^{-4}$, 2.4, and 0.13 W/(cm-K), respectively. For the materials with temperature dependent κ, we used the format, $\kappa = 1/(aT^2 + bT + c)$, and chose 3 points to determine the values for a, b, and c. For sapphire the points (κ,T) chosen were (0.486, 363 K), (0.416, 403 K), and (0.40, 445 K). For SiC, (3.6, 350 K), (2.6, 400 K), and (1.95, 450 K). Notice these points are plotted in figure 24, and show good correspondence with the average curve developed from data in the literature. For the GaN layer, the points were derived from the analytical formula 1.6 $(300/T)^{1.4}$. In all cases the sapphire and SiC were assumed undoped. In one run we assumed the SiC was doped at 10^{15} cm^{-3}, and the drain current at $V_D =$ 20 V increased by 3.75 and 5 mA, over baseline values of 27.5 and 57 mA, respectively. These were for the gate at –4 and –2 V, respectively.

The specific contact resistivities to the GaN layer on the sapphire and SiC substrate cases were $5.0 \cdot 10^{-4}$ and $1.0 \cdot 10^{-4}$ Ω-cm^2, respectively. Variation of these numbers caused a strong effect. The values seem to control the linear slope for low drain voltages to a large degree.

TABLE 11.—THERMAL CONDUCTIVITIES (W/CM-K) FOR THE PRIMARY LAYERS IN THE STRUCTURE

	AlGaN	GaN	AlN	Sapphire (see text)	SiC (see text)
κ	0.13	$1.6(300/T)^{1.4}$	0.1	$1/(aT^2 + bT + c)$	$1/(aT^2 + bT + c)$

The carrier mobilities were chosen as follows. In both the AlGaN and GaN layers the dependence on the electric field was

$$\mu(E) = \mu_\circ \left\{ 1 + \left(\frac{\mu_\circ E}{\upsilon_{sat}} \right)^2 \right\}^{-\frac{1}{2}}. \tag{49}$$

In the AlGaN the coefficient μ_o has the form

$$\mu_\circ(T) = \mu_\circ(300K) \left(\frac{300}{T} \right)^{TMUN}, \tag{50}$$

where the value at 300 K was assumed to be 600 cm^2/V-sec, and TMUN = 1.5. In all subsequent discussion, the units of the mobility will be omitted for brevity. In the GaN channel and transition layers, TMUN was 3.1 and 1.0, respectively. These values were assumed for both substrate cases. The dependence on doping and temperature in the GaN bulk was modeled using the Albrecht et al. (ref. 70) approach. The equation is

$$\frac{1}{\mu_\circ(T)} = \frac{a}{100} \ell n\left(1 + \beta_{cw}^2\right) \left(\frac{T}{300} \right)^{-1.5} + b\left(\frac{T}{300} \right)^{1.5} + \frac{c}{\exp\left(\frac{1065}{T} \right) - 1}, \tag{51}$$

$$\beta_{cw}^2 = 64.6 \left(\frac{T}{300} \right)^2.$$

The value for $\mu_o(T)$ is a fitting parameter, and μ_o (300 K) = 900 gives an excellent fit for sapphire. The fitting coefficients (a, b, and c in the above equation) were determined for our assumed doping of 10^{15}/cm^3. The values used were $a = -2.71 \cdot 10^{-2}$, $b = 2.64 \cdot 10^{-3}$, $c = -1.34 \cdot 10^{-2}$. The room temperature bulk and 2DEG channel mobility values on sapphire and SiC substrates were 900, 1560 and 900, 2000 cm^2/V respectively. These values correspond to many theoretical predictions and several measured values (refs. 71 and 72). Figure 26 takes a more expanded view of the device, and in particular showing the contact depths from the heterojunction plane.

The band diagrams for both substrates are depicted in figures 27 and 28.
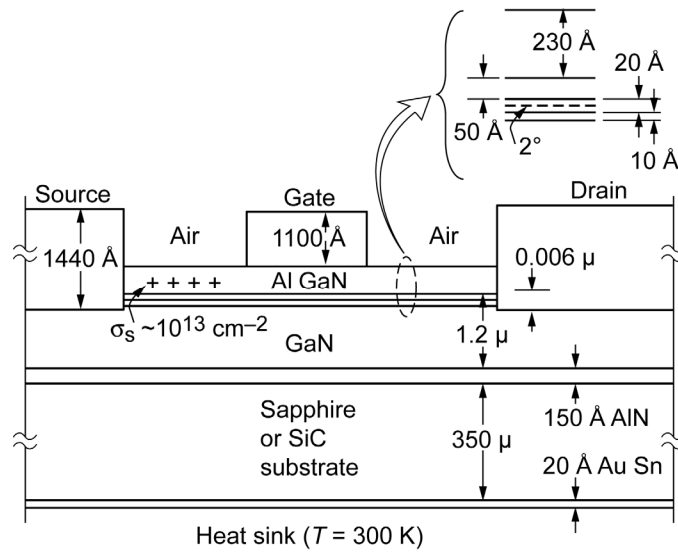
Figure 26.—Detail of basic device used in simulations.
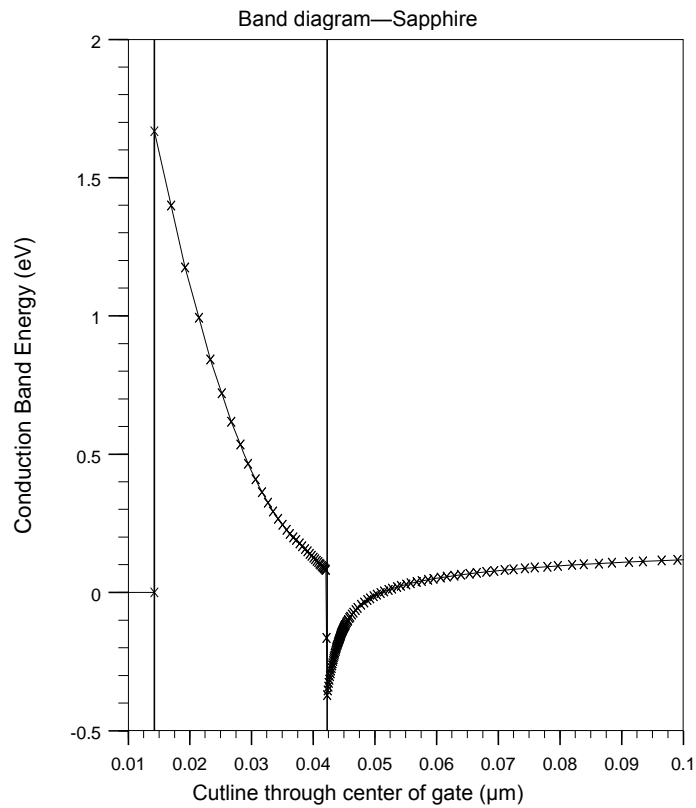
Figure 27.—Energy band diagram for sapphire substrate case.

Band diagram—SiC
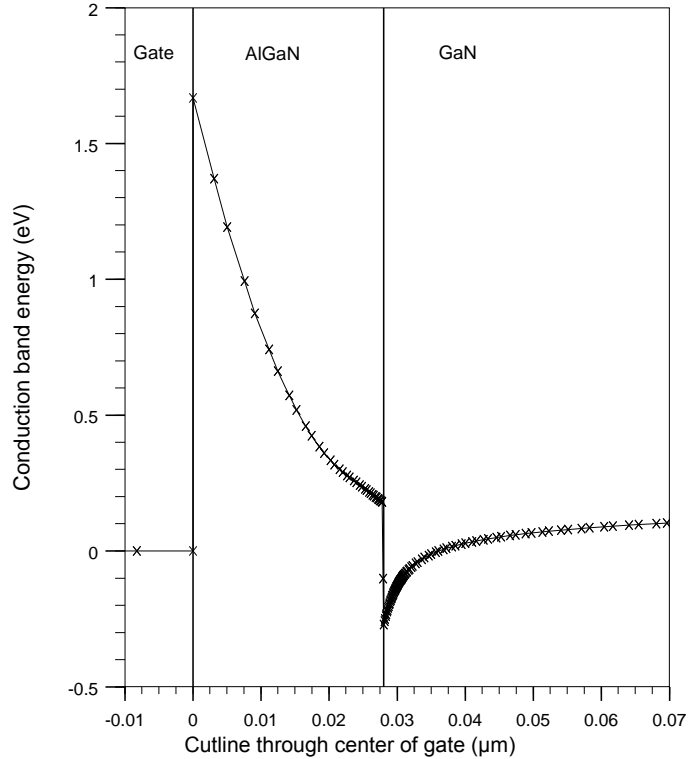
Figure 28.—Energy band diagram for the SiC substrate case.

In theory the conduction band energy is composed of many parts. For our purposes in this section, we will decompose the total band edge energy into two parts; one due to the electric potential, and the second due to "other" terms. The "other" terms will be treated in detail in the Discussion section. By definition, the electric potential is a continuous function at all points; including interfaces. Thus the potential energy associated with the electric potential is continuous everywhere. At a heterojunction, a large change in the "other" part occurs over a very small region (say 5 Å), which is modeled as a jump in the band edge. ATLAS uses the following method to incorporate the energy jump. The magnitude of the jump (the step height) is the product of the difference in band gaps of the AlGaN and GaN, and the align parameter. We chose the parameter to be 0.8, which gives a step of 0.45 eV. We specified the electron affinity of the AlGaN to be 3.82 eV, but after adjustment in the program, its effective value was changed to 2.83 eV. The adjusted electron affinity for the GaN was 3.28 eV. The energy band diagram is then constructed as follows. The electrostatic potential is determined throughout the structure; then the step of 0.45 V is added at the plane of the heterojunction. This step exists over 3 mesh points; one point is at the edge of the AlGaN, one in the interface, and one at the edge of the GaN. The function is then multiplied by –1 and given the units of electron-volts. Notice the "other" parts are incorporated solely at the interface, and the remainder follows the shape (negated) of the electric potential.

The sheet charge is placed at the interface, and perturbs the potential in this region. This causes the resulting notch depth to be near 0.38 and 0.28 eV below the Fermi level for the sapphire and SiC cases, respectively. The size of the step is held constant by the program. From experiments, the measured step for our case should be near 0.45 eV. No fixed charge is associated (in Poisson's equation) with the step, as its origin is due to "other" parts. Recall the electric potential in Poisson's equation is associated with both free and bound charge densities, and the charges that produce the step are not included. The effect of these unspecified charges is incorporated in the align parameter. Actually the step is due to the differences in the bandgaps between AlGaN and GaN. The bandgaps are due to the corresponding lattice constants and periodic crystal potentials in the two materials. The sheet charge causes a step in the normal component of the electric displacement as expected. The sheet charge is not visible in plots due to either it

not being included as an option to be plotted, (since it only exists along a single mesh line) or hidden by the line defining the interface. However, its effects are seen in the potential shape and all other applicable parameters. When the charge sheet was placed at various planes in the AlGaN, small notches appeared about them; which we considered to be unsatisfactory. This is apparently due to the software initially placing neutralizing free charge at adjacent mesh points to keep the entire system charge neutral. When this charge is placed in the notch, most of it apparently stays there or in nearby regions. When the sheet was moved to different locations, most of the free charge moved away from the plane, and left some residual near the plane. That residual along with the sheet charge caused a small well about the plane of the sheet. This is also problematic when a negative sheet charge is placed on the top surface of the AlGaN; holes are immediately inserted and must be dealt with. There is no easy way of handling the holes since they should not be present in the material. The bandgap is too large for thermal generation. So once placed in the system, they cannot combine, so what should one do to address their artificial presence? One might place some (always ionized) compensating acceptors on the surface to hold them. However, many numerical simulations we reviewed in the literature did not place any charge on the top surface; and apparently achieved good results. Therefore, we chose not to use more than one charge sheet.

VIII. Sapphire Substrate Results

The simulated (solid) and measured (dotted) I–V characteristics for a HEMT on a sapphire substrate are shown in figure 29. These data were measured by Kuball et al. (ref. 15), and we assume no trapping effects were present. Thus the I–V should be reasonably independent of sweep rate, direction of gate step voltage, and we assume the curves were developed in the thermal steady-state. The droop is assumed to be solely due to self-heating. In most practical devices the droop can be due to both self-heating and trapped charge in various regions of the device. We have neglected charge trapping, and apparently these devices have minimal trapping effects. When the lattice temperature flag was turned off, the curves did not droop.

The $V_g = 0$ curve is the primary one we will focus upon, as the measured temperatures were determined for this gate voltage. In general, the match between simulation and measurement is excellent. When approaching pinch-off, we see the conduction in the bulk is slightly too high. There are many
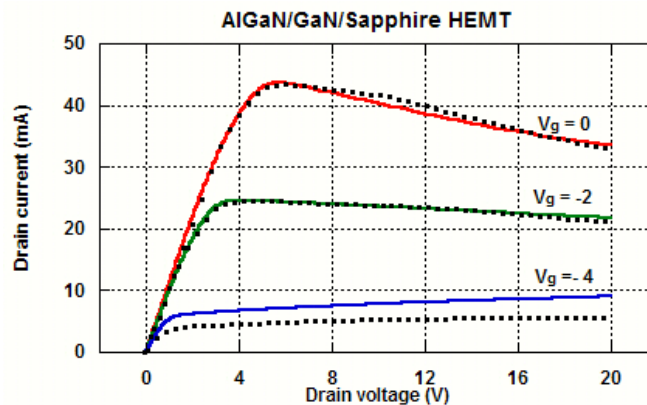
Figure 29.—Simulated (solid) and measured (dotted) I–V characteristics for an AlGaN/GaN HEMT on a sapphire substrate for gate voltages of 0, –2, and –4 V.
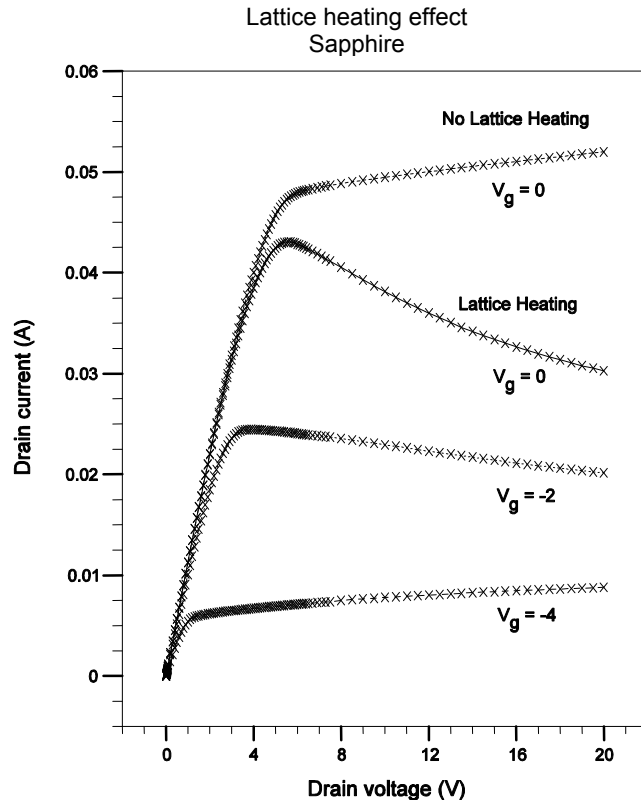
Figure 30.—The change in drain current when lattice heating
was turned off or on (for the V_g = 0 case only).

changes we can put forth to remedy this; we could reduce the mobility and/or saturation velocity and/or the doping in the lower region of the GaN where the major portion of the current exists near pinch-off. Figure 30 shows the changes in the I–V curves (only the effect on the V_g = 0 curve) for lattice heating turned off or on.

When the lattice heating was turned off and zero contact resistance was also in effect, the V_g = 0 curve reaches slightly above 100 mA at 20 V. Figure 31 gives the comparison between the simulation and measured temperatures. The comparisons are made at drain voltages of 4, 8, 12, and 20 V. The vertical lines with dots are just to aid the eye. The simulated temperatures at the gate edge are below the curve, and the ranges of temperatures from Kuball's paper are given above. The simulated values tend to the low sides of the ranges at low drain voltages, and then to the high side near 20 V. Only at 12 V is the simulation comfortably in the range. The measured data ranges are the same as those given in table 2 in section V. Observe the ranges are not precise, and only a visual judgment of the measured points was used.

Figures 32 and 33 give the temperature variation (drain at 20 V, gate at 0 V) along a cutline through the middle of the gate to the bottom heat sink.

The contour plot in figure 32 shows that the isotherms become horizontal near a depth of 50 μm. The peak temperature is 197 °C, and that at 50 μm is 137 °C. The right panel shows the nearly linear drop in temperature through the sapphire. Figure 33 gives the detail near the surface. The drops across the GaN and AlN regions are about 2.1° and 0.3° respectively. Figure 34 shows the drop across the device for increasing drain voltage (unless stated otherwise, the gate was always at zero). We can generalize; a nearly exponential drop occurs for the first 50 μm, with the remainder being linear. The linear drop occurs when the isotherms are horizontal (as expected). Figure 35 shows the peaking behavior at the gate edge (on the drain side) as one moves horizontally from source to drain. The spike occurs at the gate edge in all cases. Kuball's laser spot size was about 1 μm², and his longitudinal steps were between 0.2 and 2 μm, so his measurements should capture the correct average temperature.

Lattice temperature (°C)
Sapphire
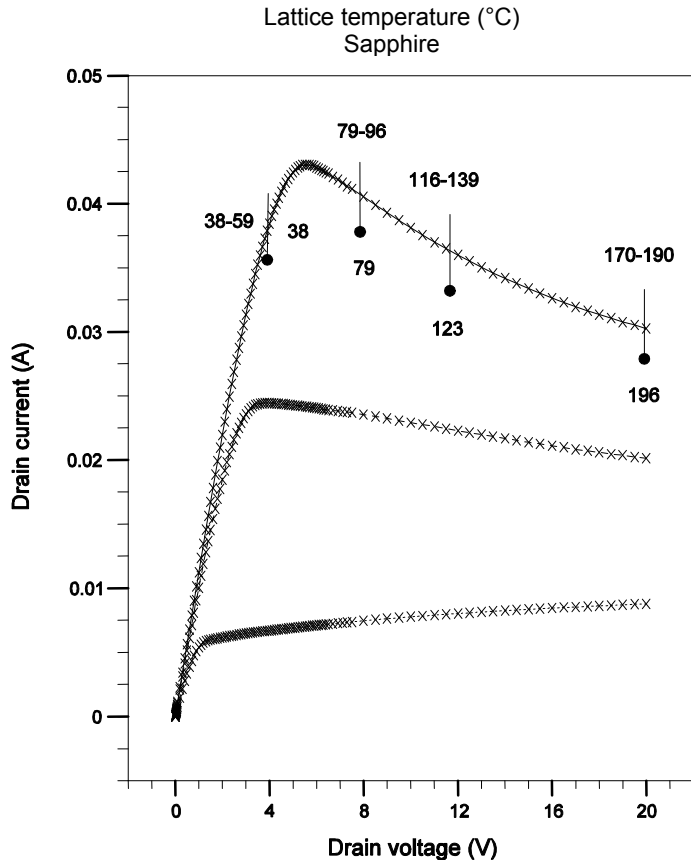
Figure 31.—The measured range of channel temperature (above curve) and the simulated values (below) at drain voltages of 4, 8, 12, and 20 V.

Device temperature
Sapphire (V_d = 20 V)
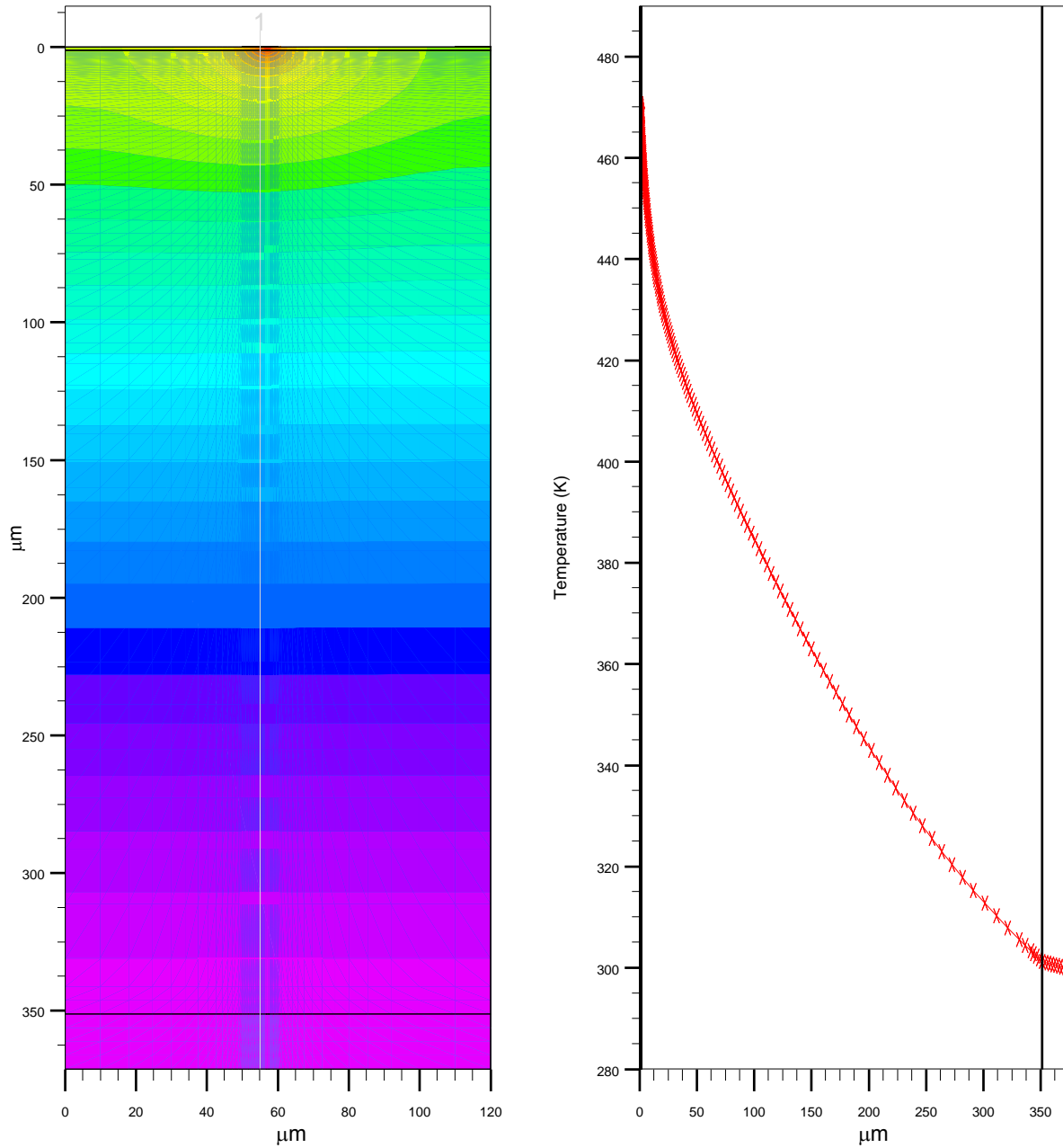
Figure 32.—The temperature contour plot and value along a vertical cutline through the center of the gate for the drain at 20 V.
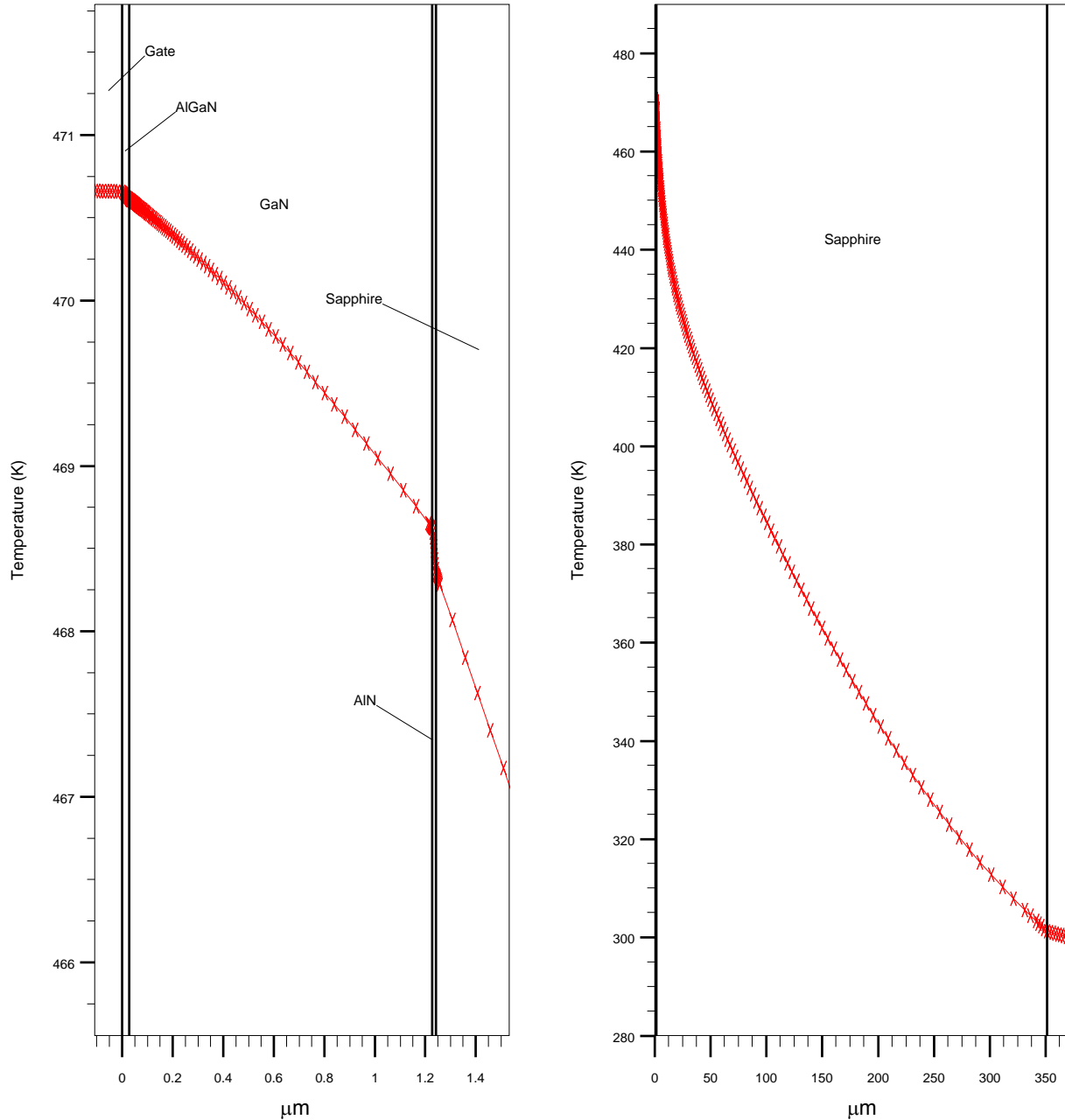
Figure 33.—The detail of the temperature in the AlGaN/GaN and AlN regions (left panel) along with the variation through the sapphire (right panel).

Figure 36 gives temperature changes as one moves from the gate towards the drain. The three curves are values at the channel, middle and bottom of the GaN layer, respectively. At the gate edge the values are 482, 478.5, and 475 K; which is only a difference of 7°. Therefore averaging over the depth should not produce significant error.
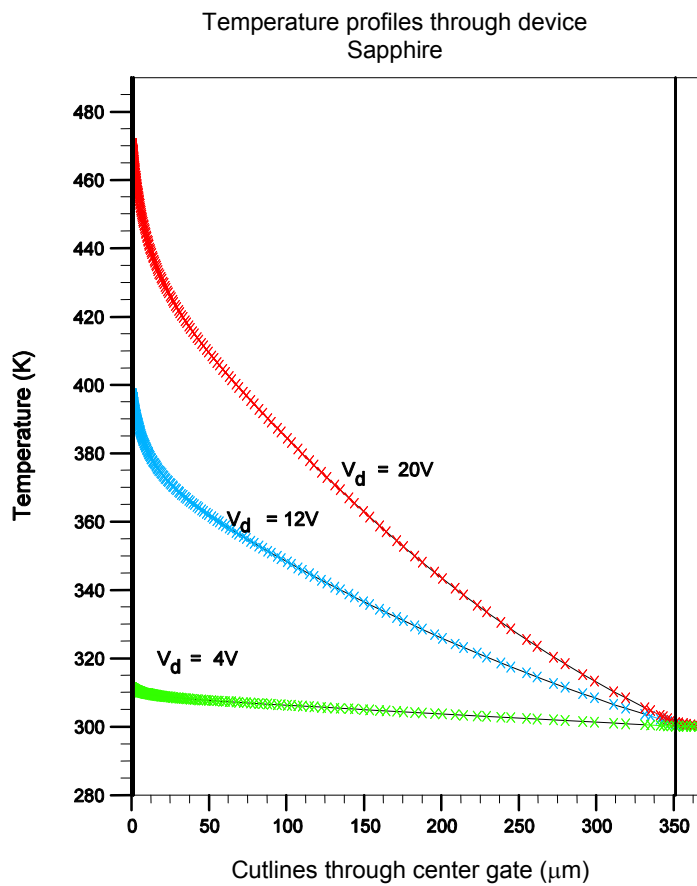
Figure 34.—Temperature drops across the sapphire substrate for drain-source voltages of 4, 12, and 20 V.
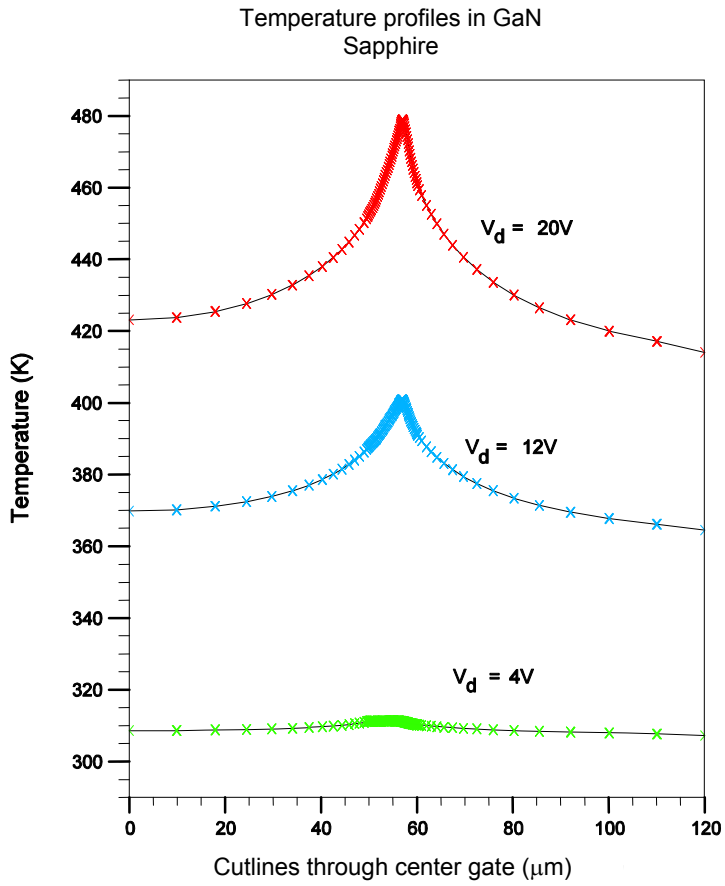
Figure 35.—Variation of temperature as one moves horizontally through the center of the GaN layer.
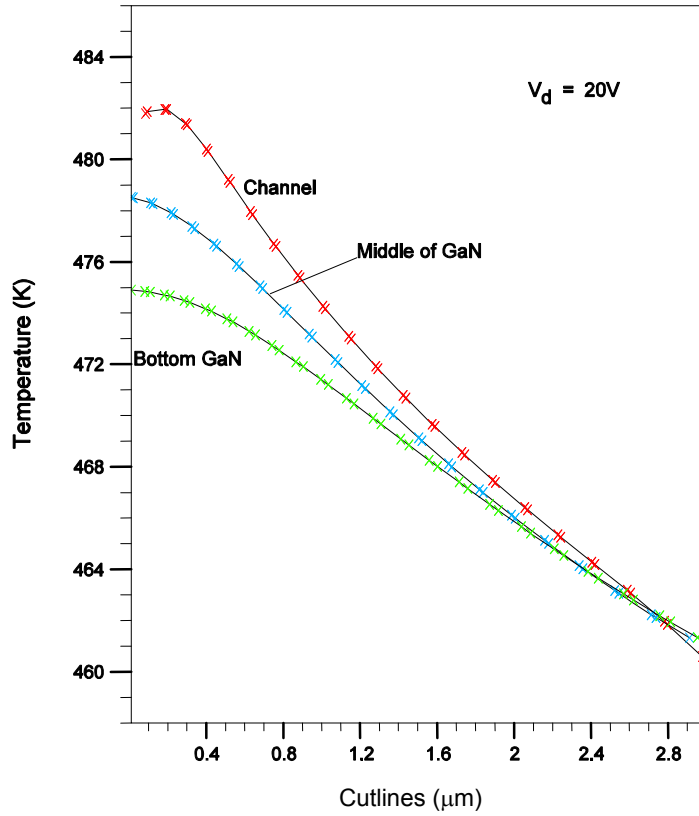
Figure 36.—Temperatures between the gate and drain edges at the top, middle, and bottom of the GaN layer.
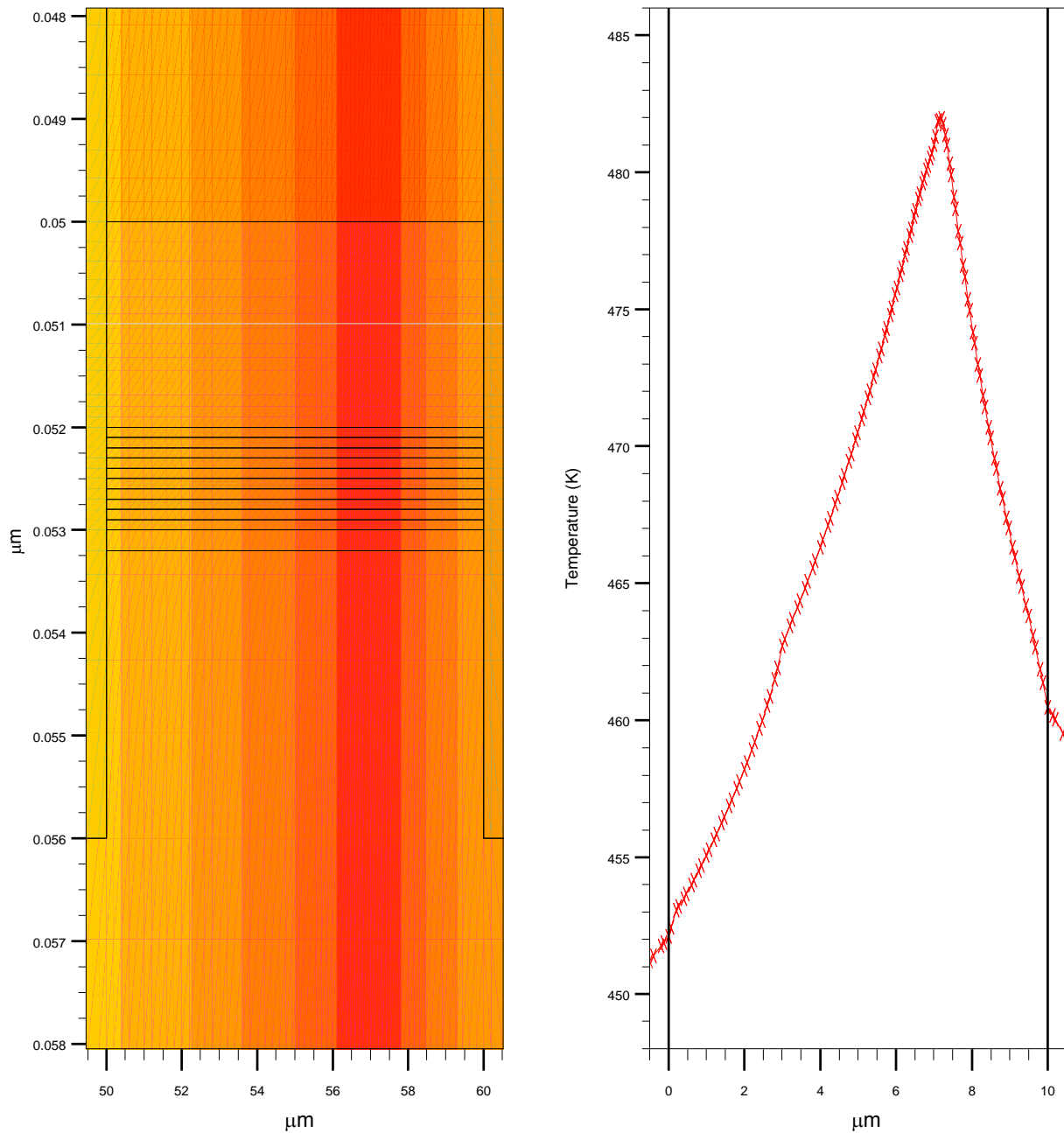
Figure 37.—A thermal contour plot and the temperature from source to drain at the middle of the GaN layer. The 1 Å thick transition layers are shown in the contour plot.

The horizontal cutline in figure 37 is at the center of the channel in the GaN layer, and it reveals the change in temperature from the source to drain contacts. The small kink in the curve in the panel on the right is at the gate edge near the source. The source and drain edges are at 179 and 187 °C, and the edges of the gate are at 190 and 209 °C.

Table 12 shows the drain current at $V_d = 20$ V, at zero gate bias, for two different variations on temperature of the thermal conductivity. Observe the current differs by 3 mA while the temperatures differ by 32°. Smaller differences are seen for the gate at –2 V.

TABLE 12.—CHANGE IN PEAK TEMPERATURE AND DRAIN
CURRENT FOR TWO DIFFERENT APPROXIMATIONS FOR
THE THERMAL CONDUCTIVITY FOR SAPPHIRE

$\kappa(T)$	$I_d(20V)$, mA	T, K
$1/T$	31	482
$1/(aT^2 + bT + c)$	34	450

Figure 38 shows the temperatures at the gate edge (at the surface) and at vertical planes in the gate-drain access region of the GaN layer versus the drain voltage.

Figure 39 reveals the source and gate edges track each other with drain voltage. Figure 40 is a potential contour plot; the steps are in 3 V.
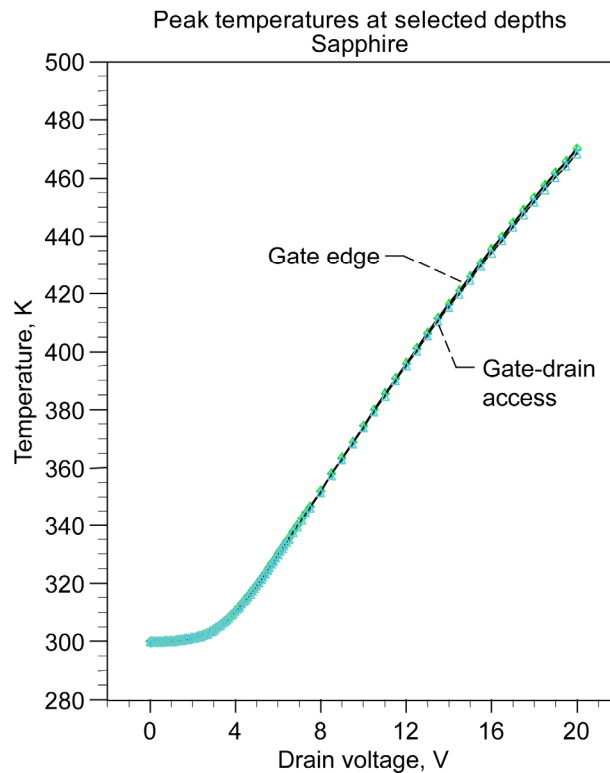
Figure 38.—Gate edge temperatures and that in the gate drain access regions as the drain voltage is increased.
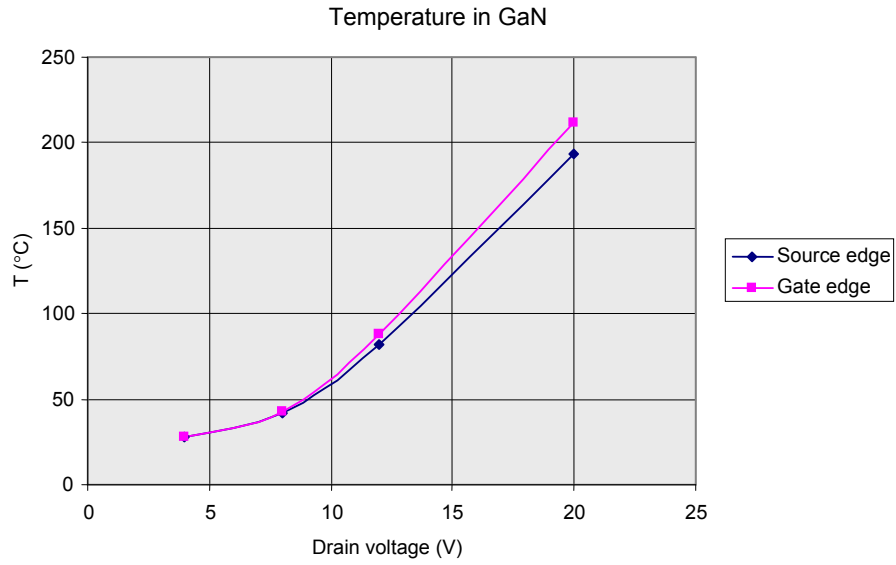
Temperature in GaN

Figure 39.—The temperatures at the gate and source edges with increasing drain voltage.

Potential plot at V_d = 20 V
Sapphire
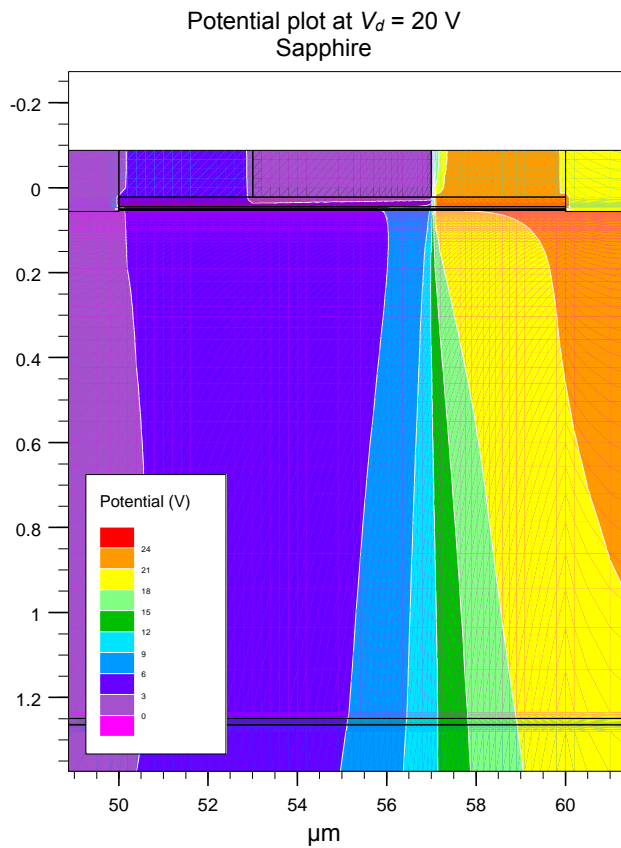
Figure 40.—Constant potential contours (3 V steps), showing the source, gate, and drain pads from left to right. The gate is at 0 V.

Figure 41 shows the potential at a vertical cutline through the gate on the left, and along a horizontal cutline at a depth of 0.0501 μm.

Potential under gate and in channel
Sapphire (V_d = 20 V)
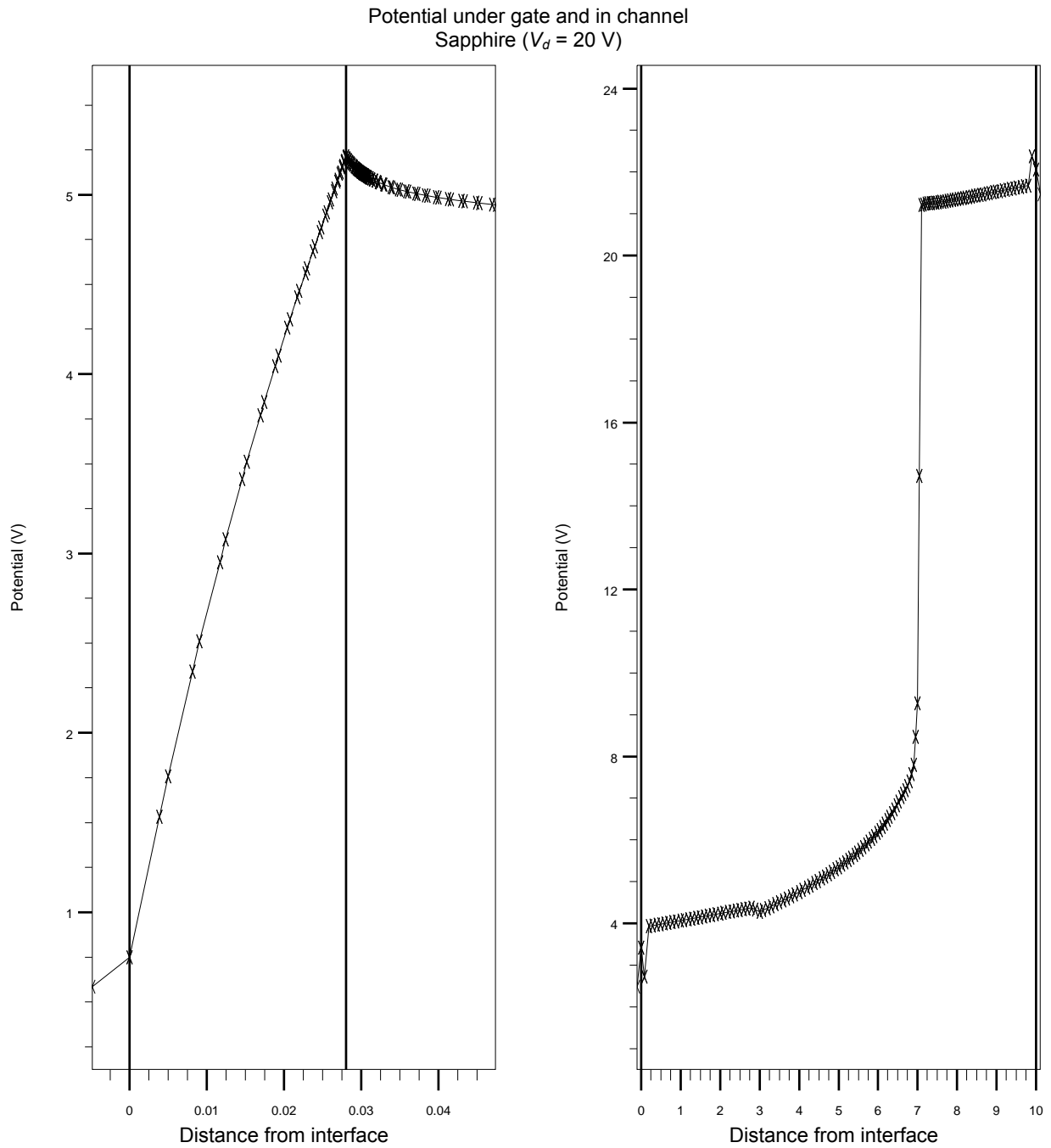
Figure 41.—Variation of potential along a vertical cutline near the gate center (left panel), and along a horizontal cutline along the channel at a depth of 0.0501 μm for drain (right panel) at 20V.
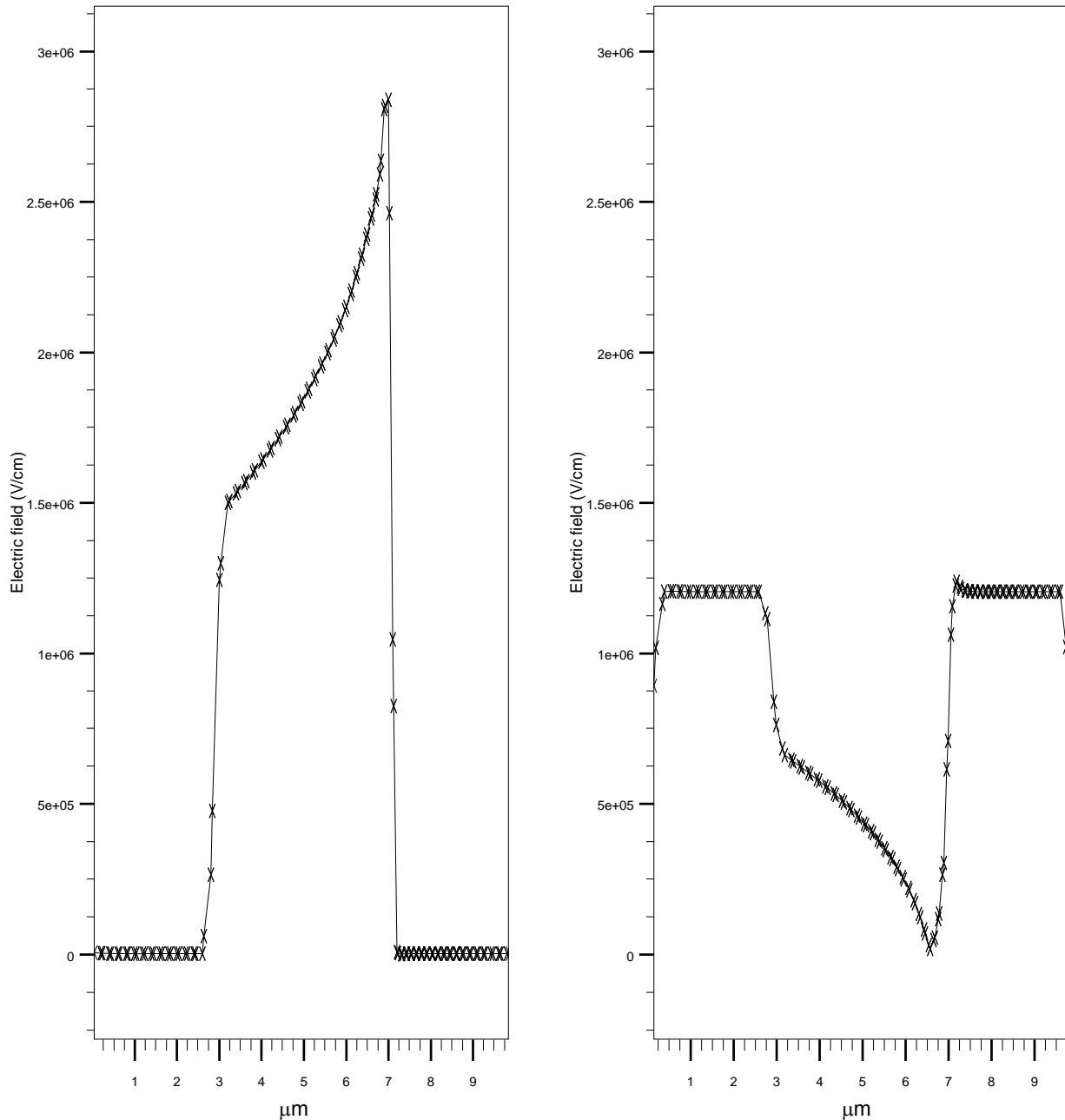
Figure 42.—The electric field in the AlGaN from source to drain (left panel). That in the GaN is shown on the right; Observe the field drops two orders of magnitude at the gate edge.

The electric field magnitude from the source to drain in the AlGaN and GaN layers is depicted in figure 42. The left panel shows the peaking at the gate edge in the AlGaN buffer region. Observe it approaches 3 MV/cm, which is close to the avalanche value. The literature states the avalanche field is somewhere between 3 and 6 MV/cm. The right panel shows the much lower value in the channel. Observe the notch at the gate edge where the field drops to 1.8×10^4 V/cm. Figure 43 shows the magnitude of the electric field near the channel, from source to drain for drain voltages of 20 (left) and 8 (right) V.
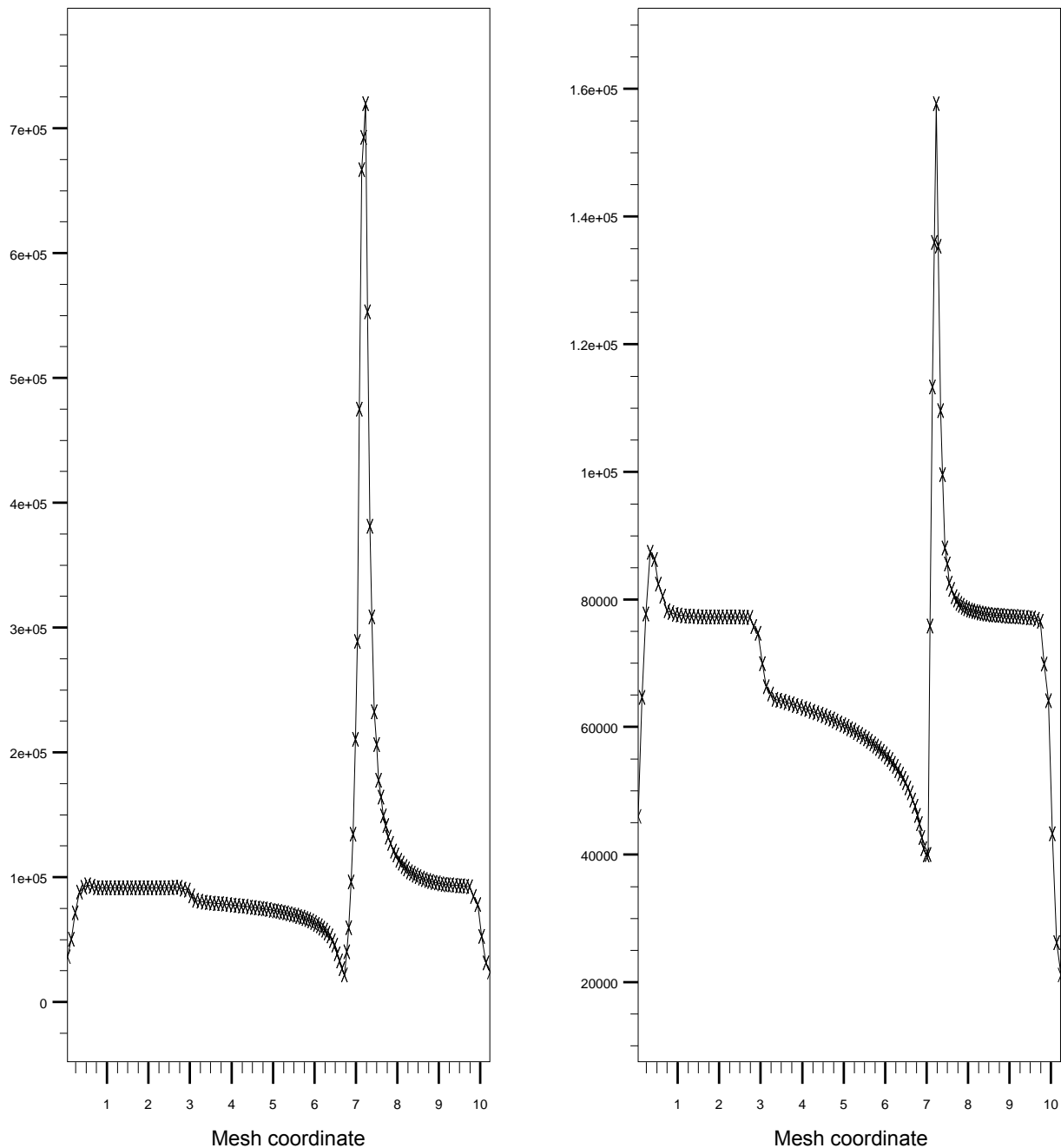
Figure 43.—The variation of the magnitude of the electric field near the channel for 20 V (left panel) and 8 V (right panel) on the drain.

The magnitude of the velocity field at two horizontal cutlines is illustrated in figure 44. The left panel is at a plane below the channel, while that on the right is at a deeper plane.

Figures 45 through 48 demonstrate the carrier concentration variation along specific cutlines.
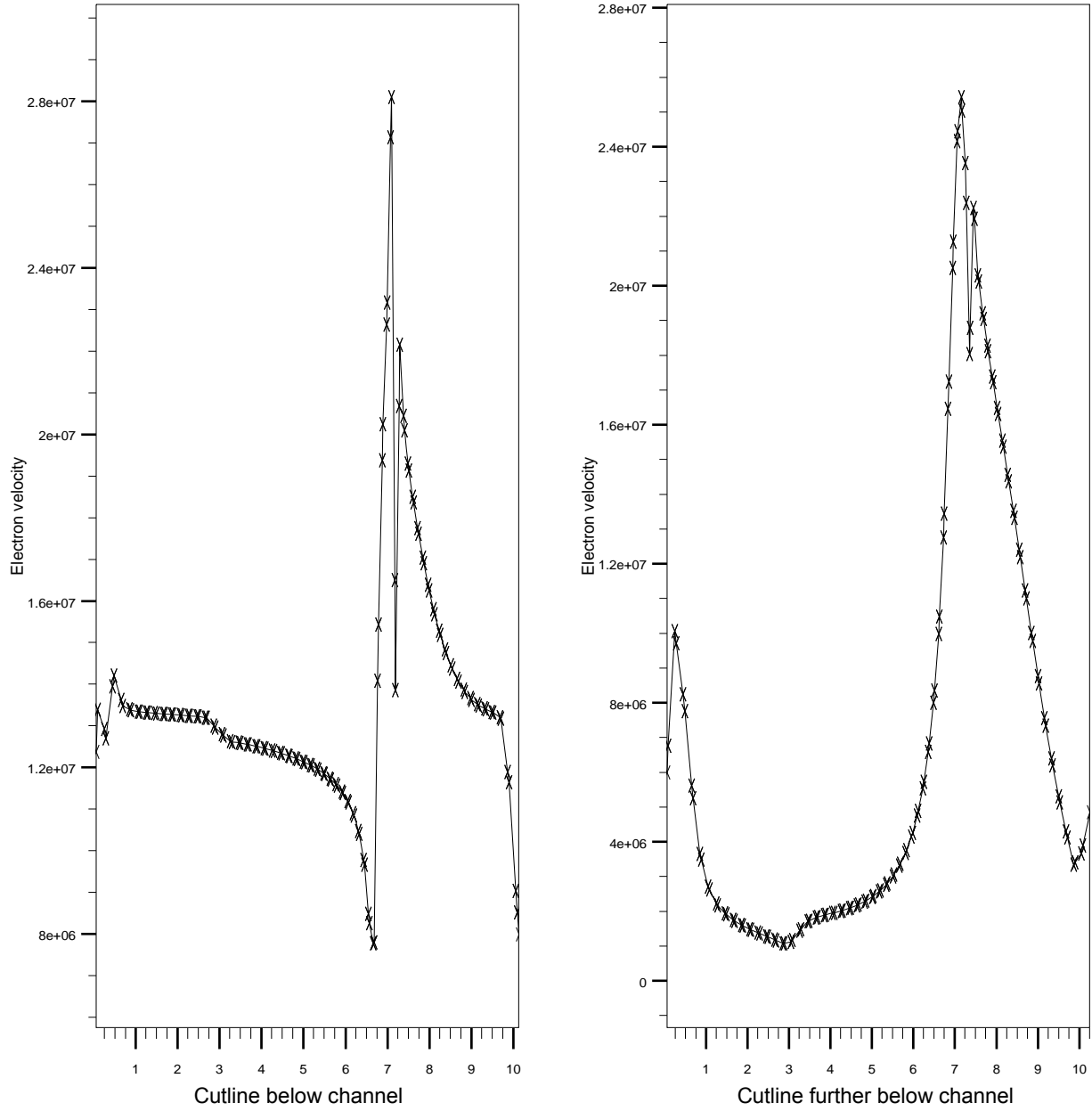
Figure 44.—The velocity field (cm/s) at two depths below the channel.
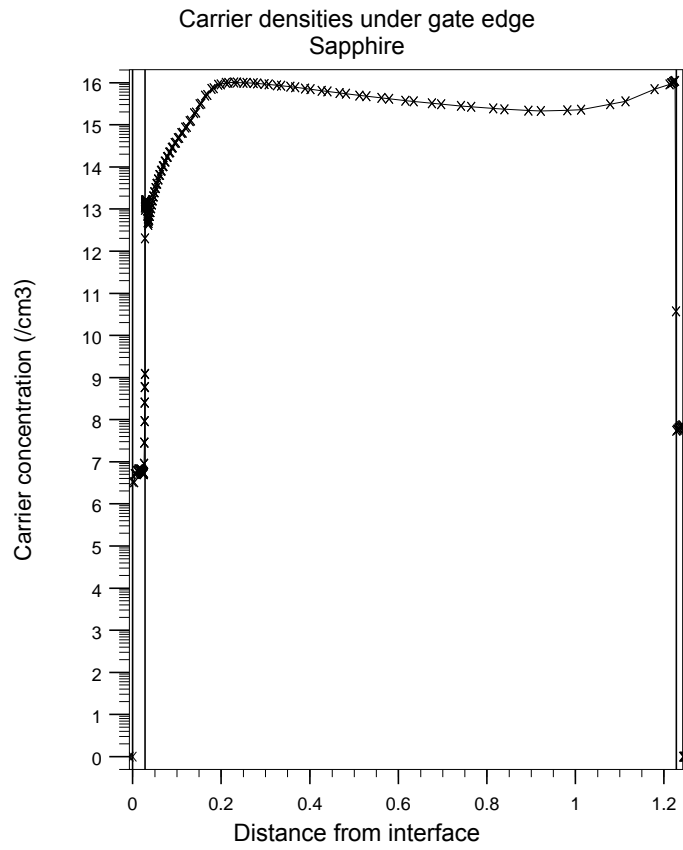
Figure 45.—The distribution of carriers along a vertical cutline at the gate edge through GaN at V_d = 12 V.

Figure 46.—Carrier densities along vertical and horizontal cutlines on the left and right panels respectively. On the left, the cutline starts in the AlGaN and crosses the heterojunction. On the right, observe the depleted notch at the plane of the gate edge.
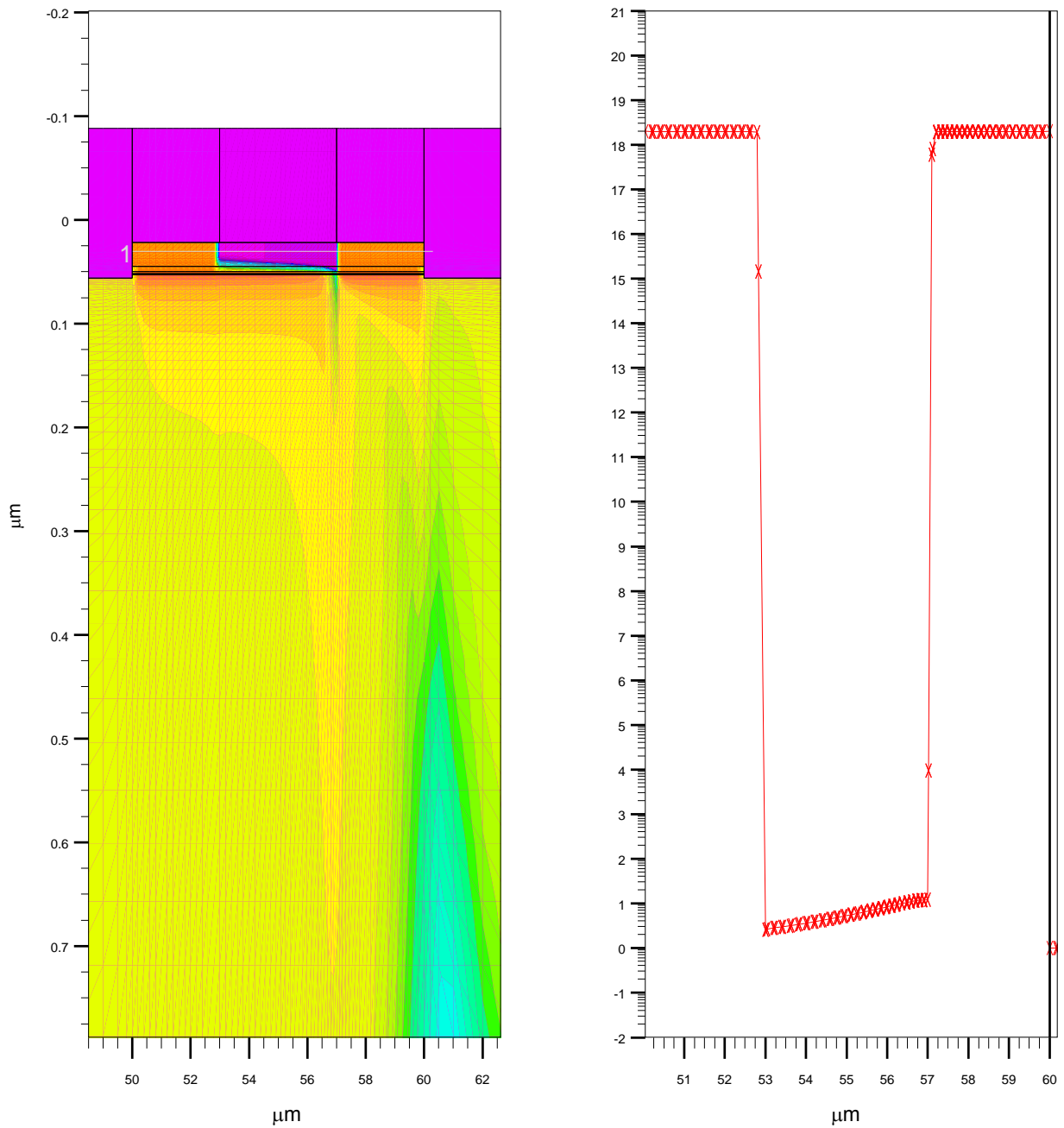
Figure 47.—Contour plot of the carrier density. The right panel shows the concentration along a horizontal cutline through the AlGaN at a depth of 0.030 µm. Notice the region under the gate is completely depleted.

Carrier density under gate
Sapphire
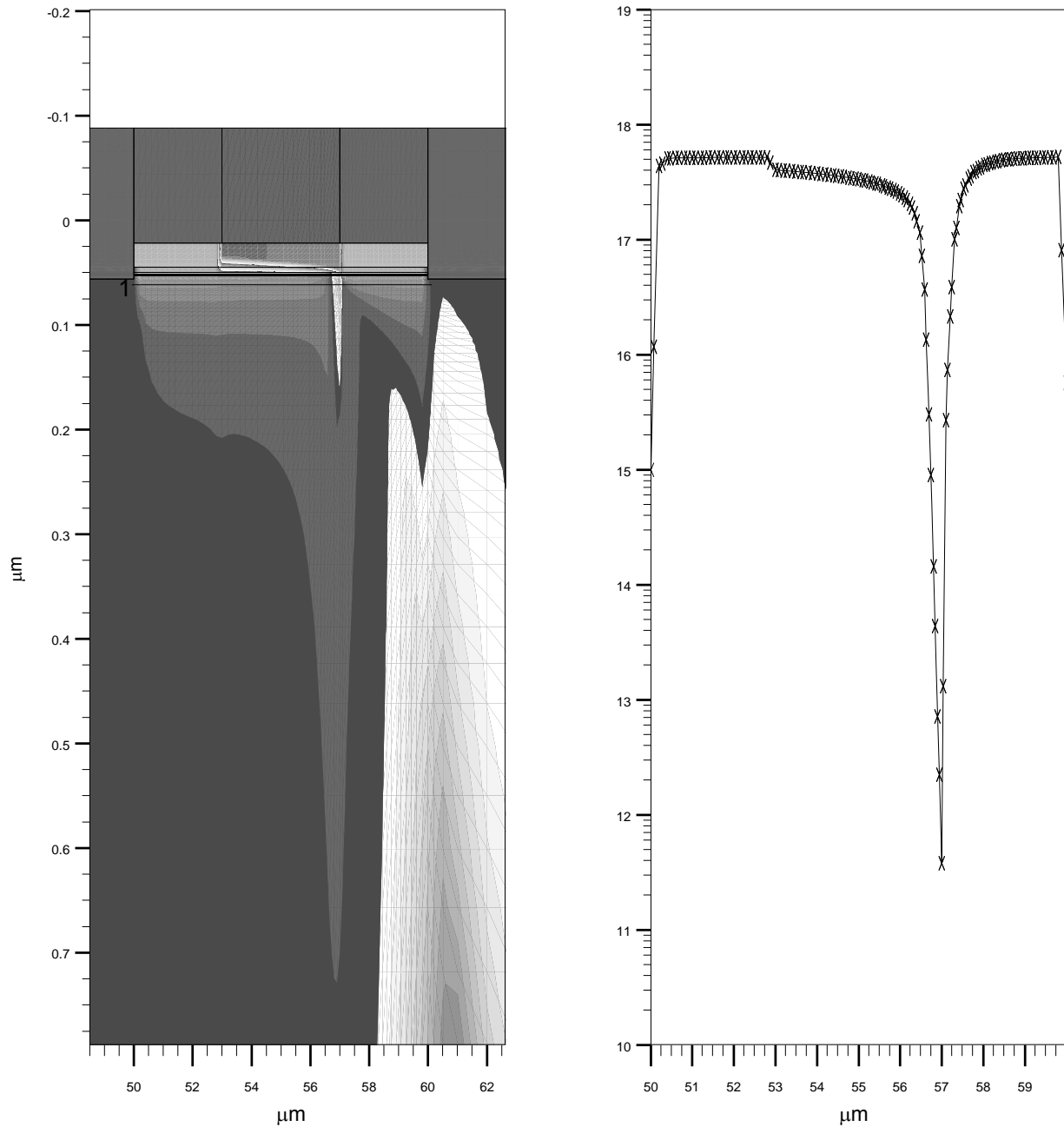
Figure 48.—Contour plot of carrier density; the right panel demonstrates depletion near the gate edge along a plane 0.061 μm below the heterojunction.

Figure 49 is along a horizontal cutline at a depth of 0.035 μm. The current density is seen to be zero in the AlGaN under the gate.
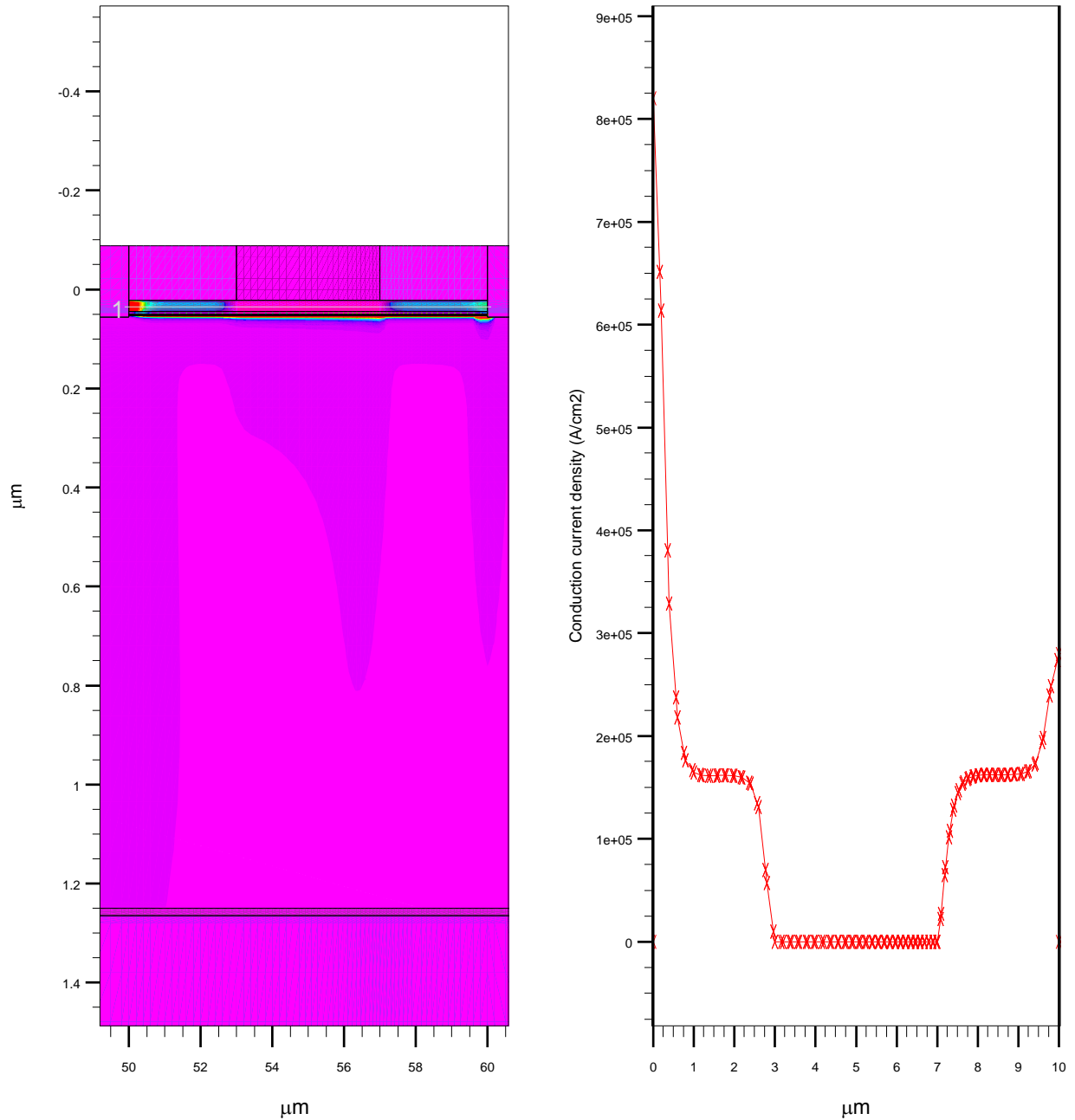
Figure 49.—The current density in the AlGaN layer versus horizontal position. Cutline at 0.035 µm.

Figure 50 demonstrates the interesting behavior of current density variation with depth into the GaN. The current drops in the lower half, but then picks back up near the AlN interface. Notice the absence of current at the heterojunction, which means a portion of the "channel" is completely depleted. Therefore in the saturation region, the current is supported by conduction solely in the GaN layer over horizontal intervals encompassing the gate edge plane. Further down the channel (say midway to the drain) the current in the channel picks back up. A spike of current then exists at the heterojunction.
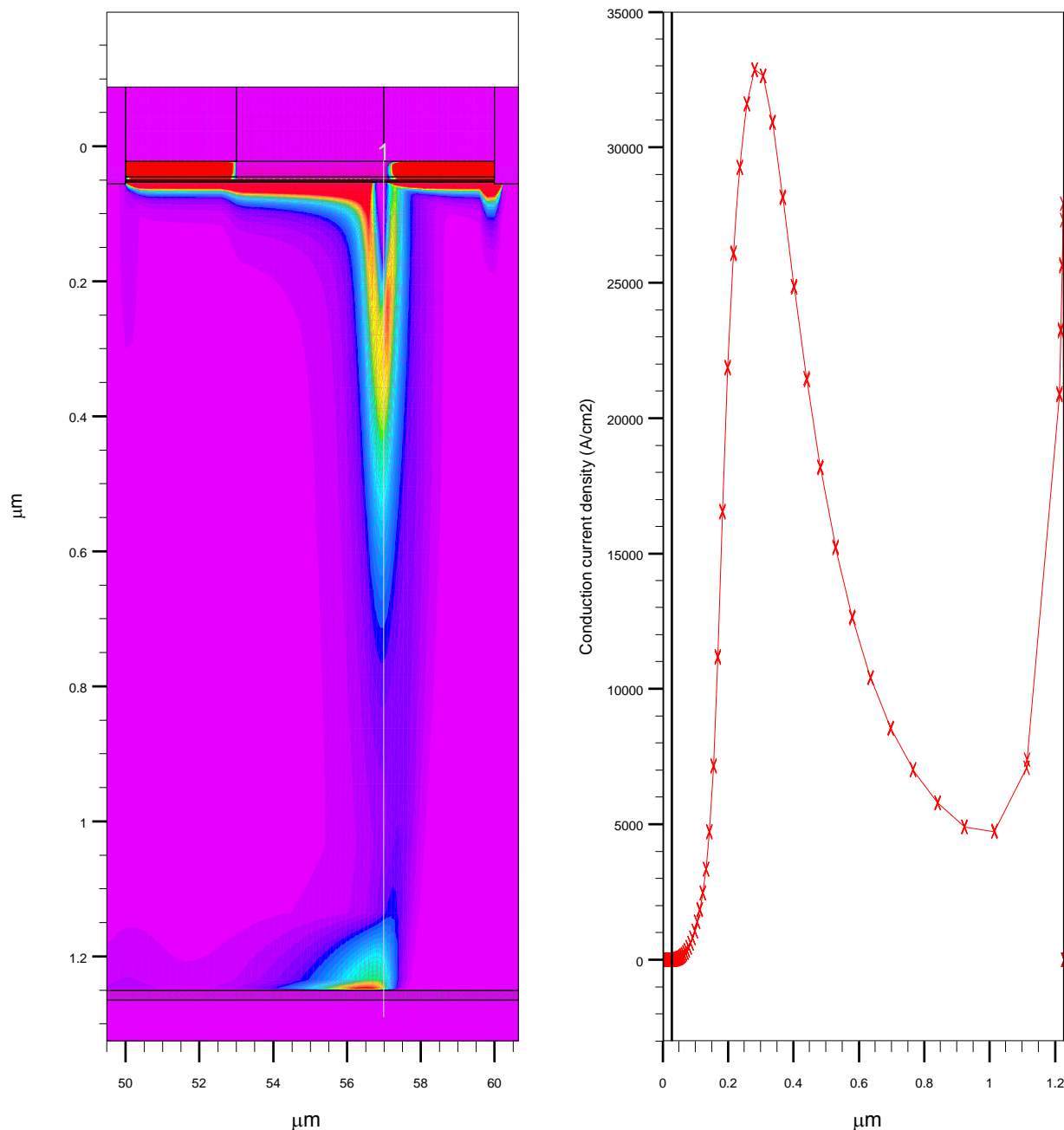
Figure 50.—Contour plot of the current density. The right panel shows the current density along the vertical cutline at the plane of the gate edge

Figure 51 has an interesting contour plot of the current density. The light regions indicate larger values. The plot on the right is along the cutline shown just below the channel. Notice the deep notch at the plane of the gate edge.
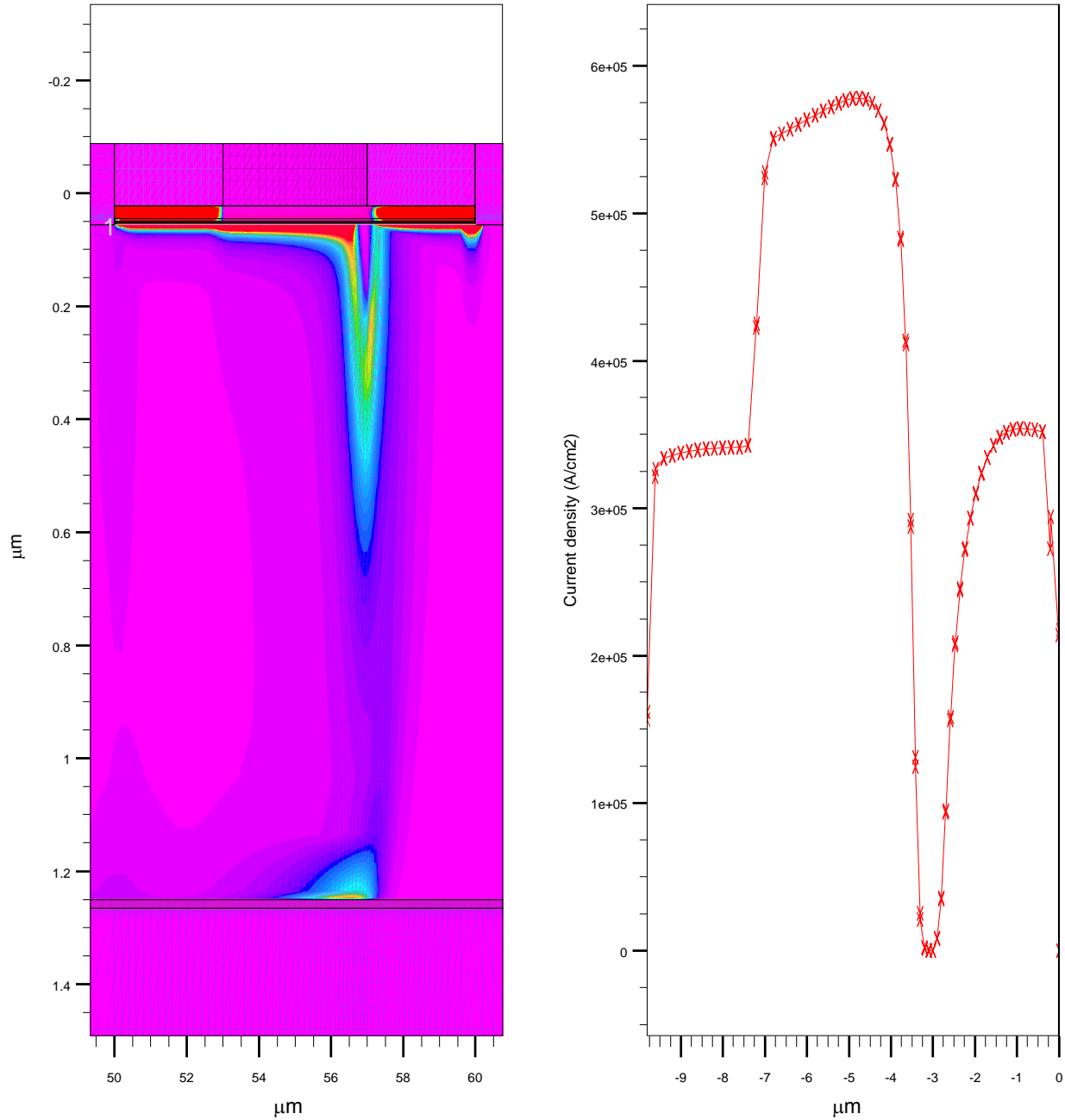
Figure 51.—Current density along a horizontal cutline slightly below the channel. The notch occurs at the gate edge.

Figure 52 demonstrates the heat generation profiles at horizontal cutlines.

Sapphire
Horizontal cutline along channel

Horizontal cutline at depth 0.2 m in GaN
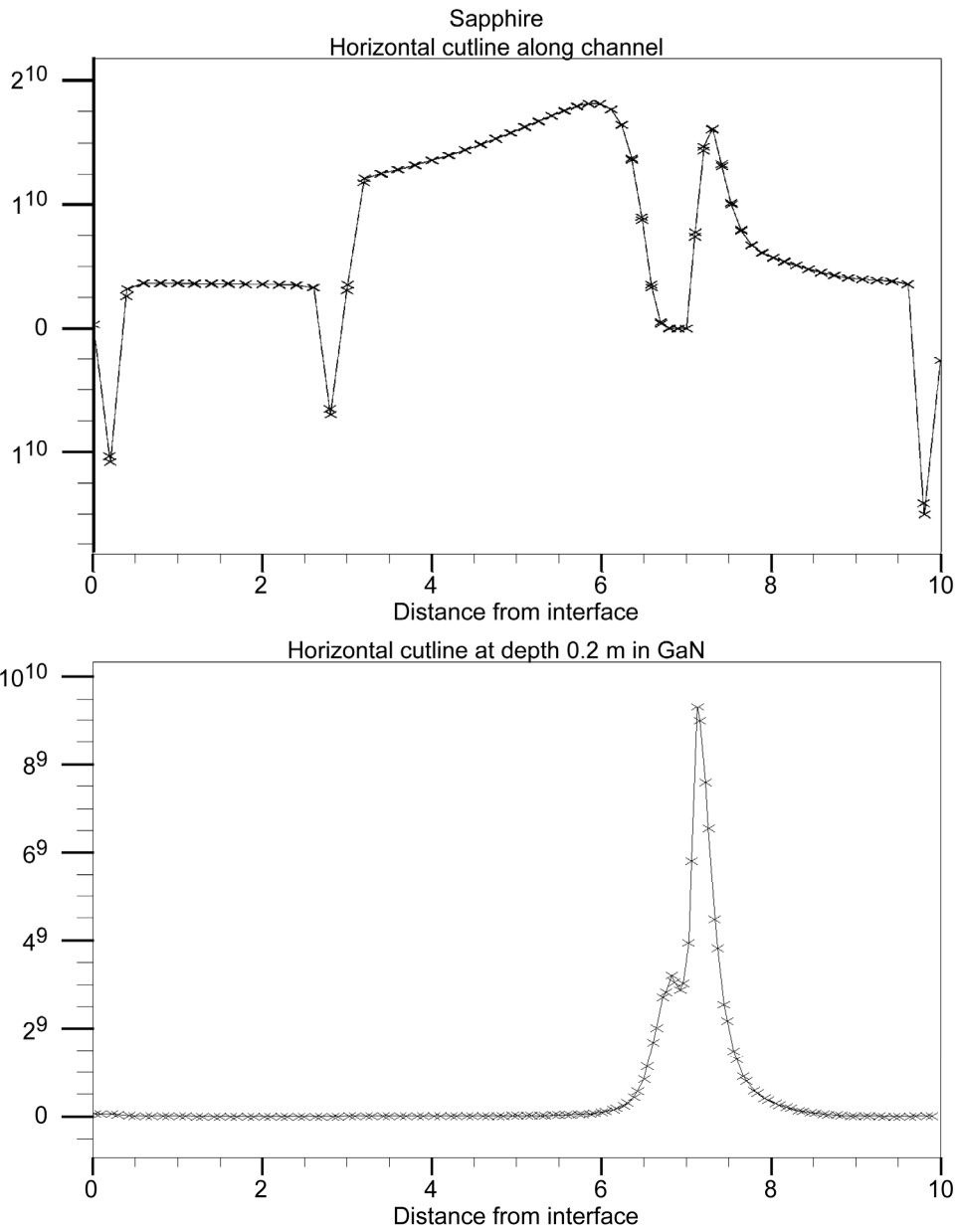
Figure 52.—The heat generation profile at two different horizontal cutlines. The drain is at 20 V.

Figure 53 is a close-up view of the heat generation rate along a horizontal cutline in the channel area. Observe the heat generation at the source and drain contacts. The heat generation is composed of several terms; the dominant one being the dot product between J and E, the other components are assumed small. The notches occur in the portions where the current is very low.
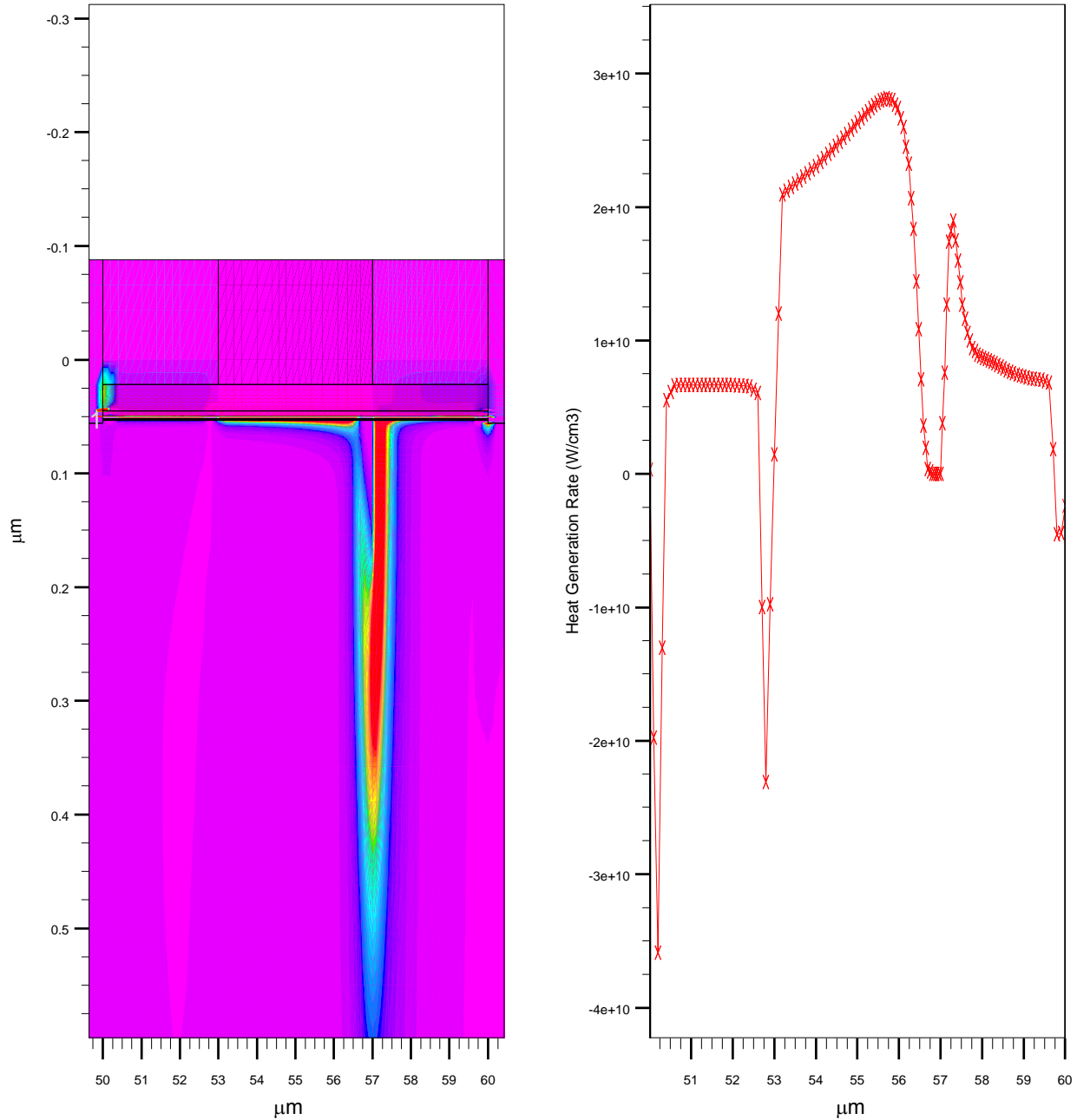
Figure 53.—Contour panel and cutline along the channel of the heat generation rate (W/cm^3) for 20 V on the drain. Notice the heat generated at the ohmic contacts.

Figures 54 through 57 illustrate the heat generation rate as the voltage is increased from 4, 8, 12, and 20 V. The shapes of the plots leads one to speculate that a combination of point sources (for the spikes) along with uniform regions (averages of the remainder), may yield better results in analytical models.

Heat generation rate at V_d = 4 V
Sapphire
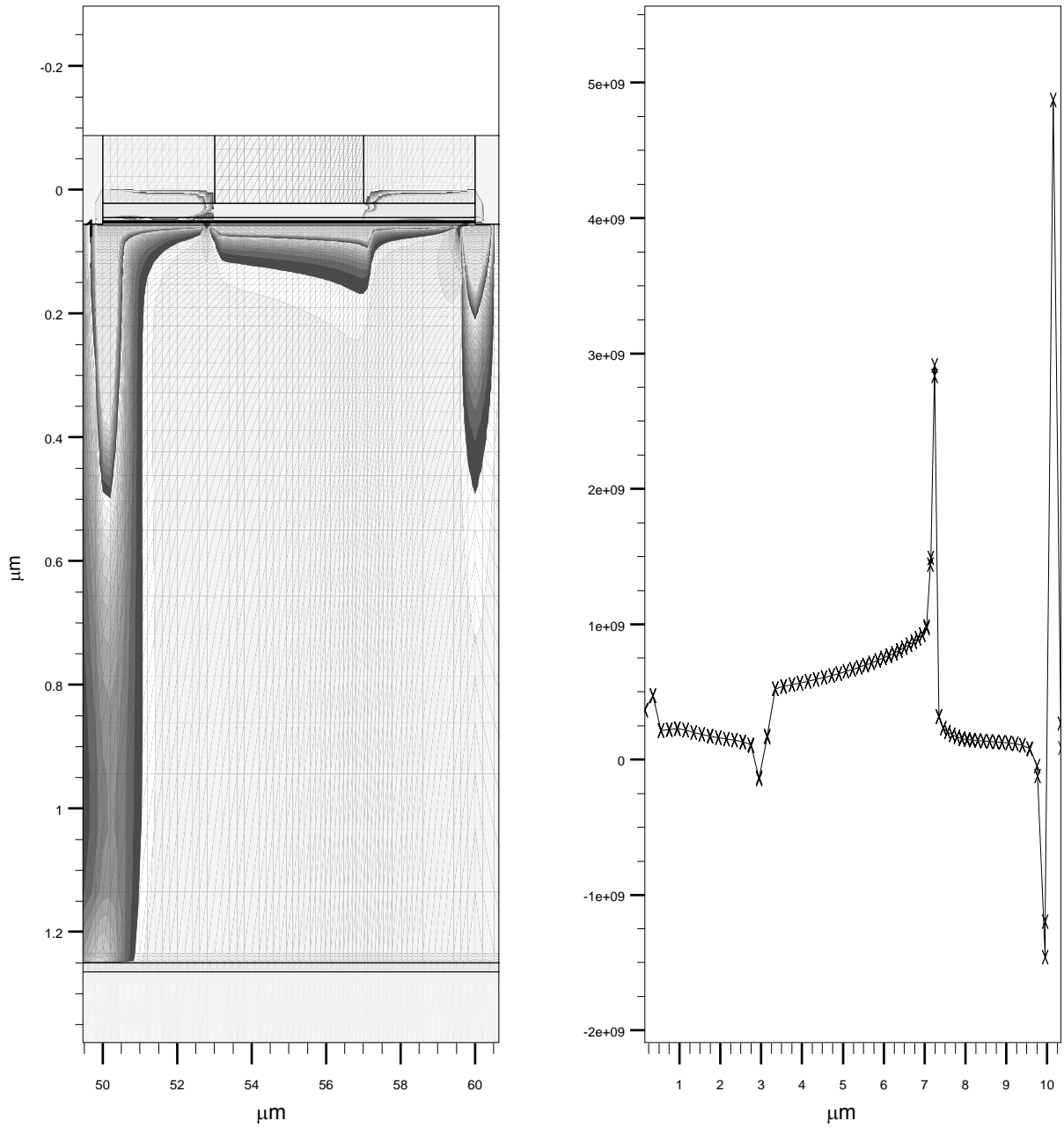
Figure 54.—The heat generation rate along a horizontal cutline at a depth of 0.06 µm for 4 V on the drain.

Heat generation rate at V_d = 8V
Sapphire
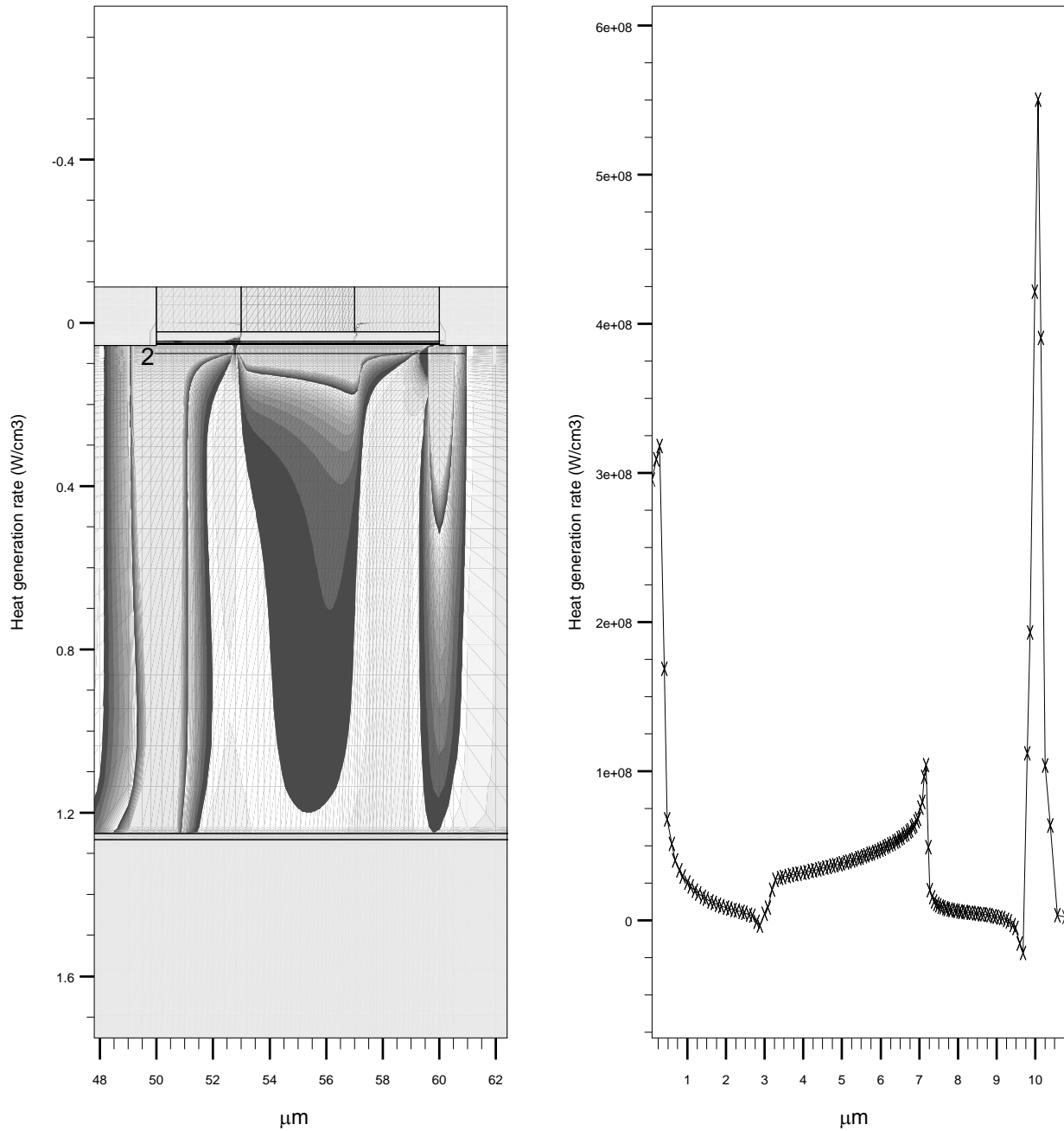
Figure 55.—The hot-spot peak is below the drain pad at 8 V. The lighter portions in the contour plot are the hotter regions and the cutline is at a depth of 0.08 μm.

Heat generation rate at V_d = 12 V
Sapphire
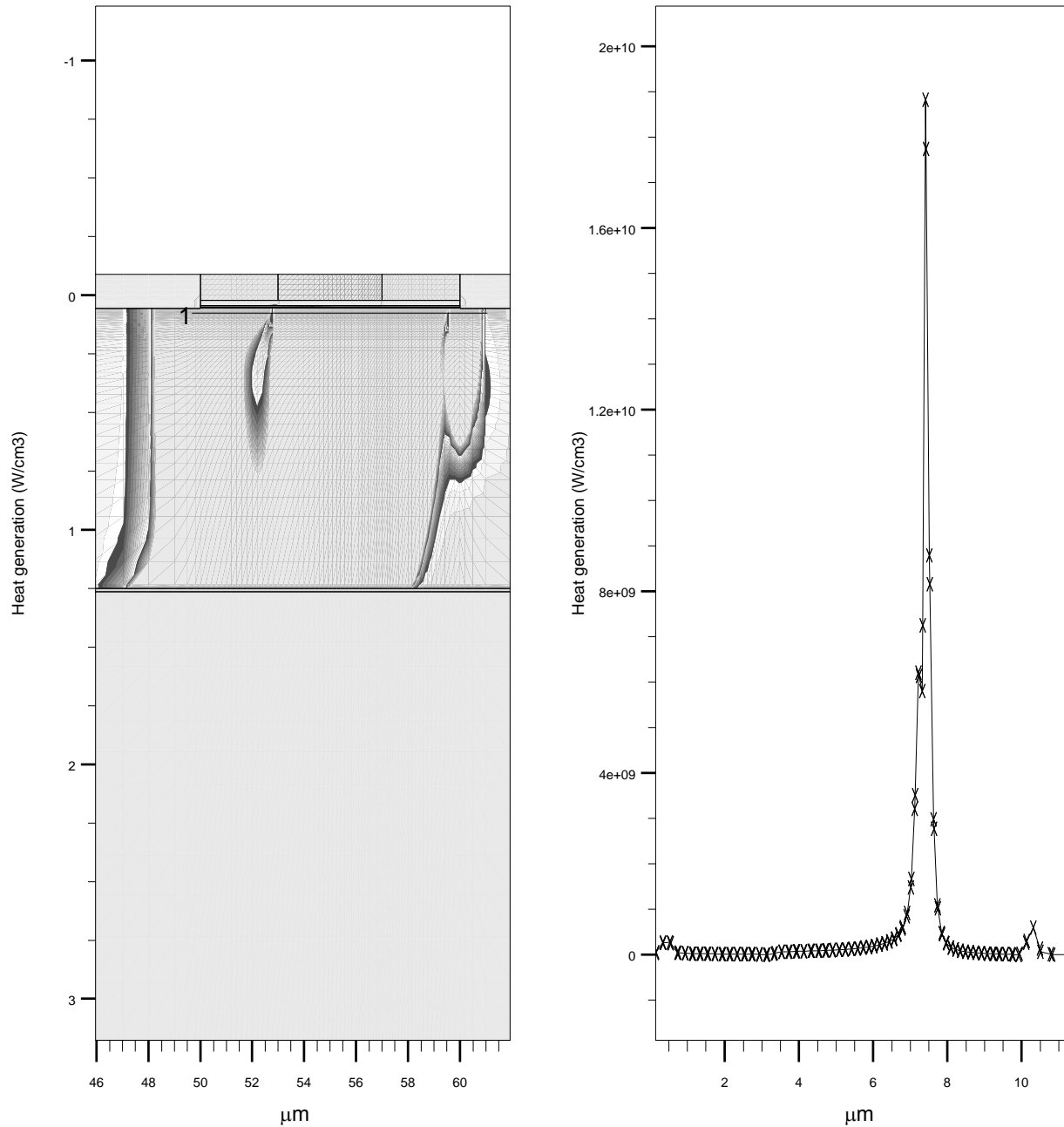
Figure 56.—Heat generation at 12 V with a cutline at a depth of 0.08 µm.

Figure 57 displays the current density and heat generation rate along the same cutline. They track one another for the most part. Near the AlN layer the generation is low due to the reduced electric field there.
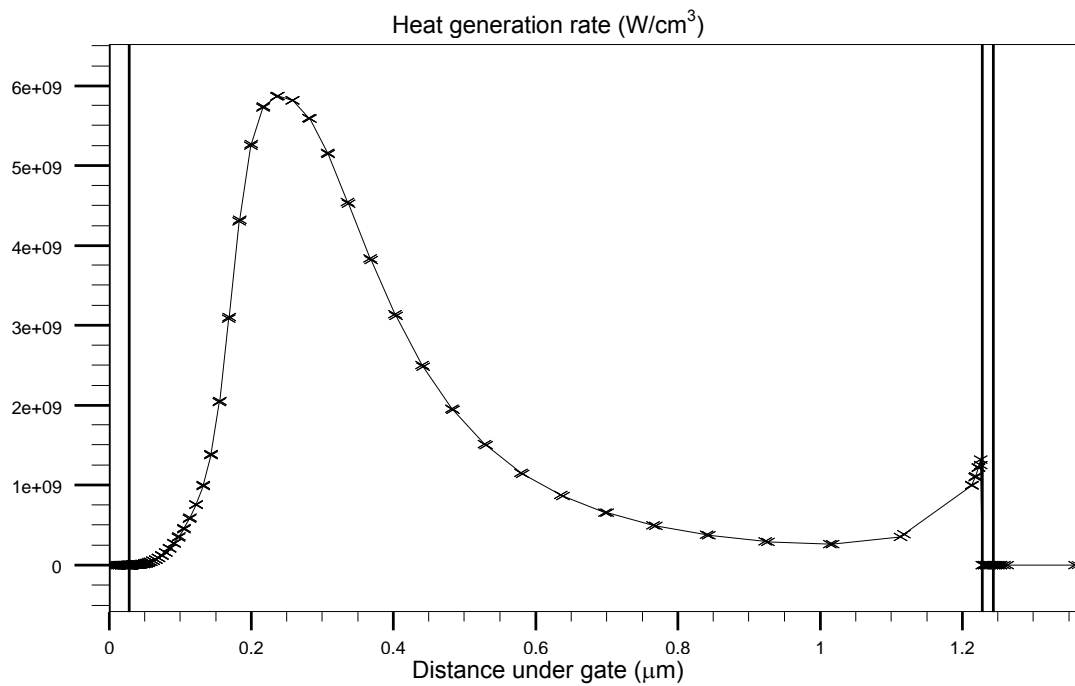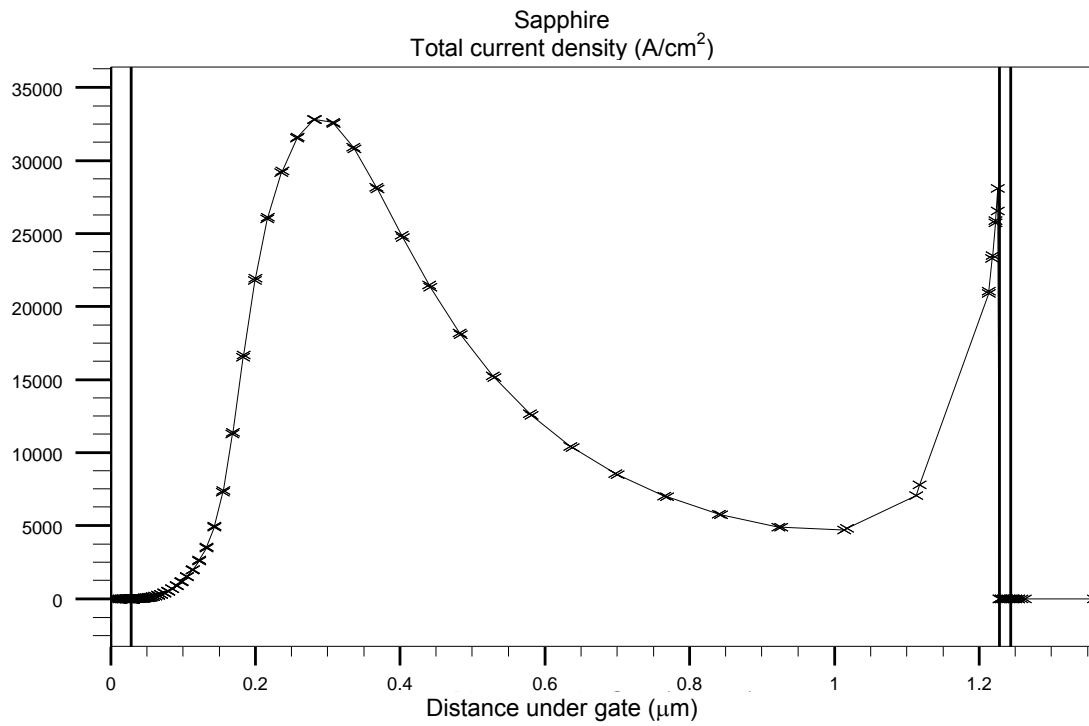
Figure 57.—Vertical cutline showing both the current density and heat generation rate. Drain at 20 V.

In general there are four spikes in $g(x,y)$, the heat generation rate. They are at the contacts and edges of the gate. It is interesting that $g(x,y)$ is near zero at the singularity plane due to the current (the current density is as low as 3 A/cm^2) being near zero there. In spite of this, however; the temperature peaks in this region. We close this section by stating that the channel current is disrupted in an interval about the gate edge. For cutlines not exactly at the heterojunction, the current is nearly zero. Much of the current is carried in the upper portion of the bulk GaN layer in the saturation region. Thus the detailed properties of the channel are not especially important for the device current. The properties of the upper portion of the GaN layer are important for current. It is also interesting that a portion of the current exists near the GaN-AlN plane. This appears to be due to the geometry of the device; that is, a favorable horizontal component of the electric field. In some cases the channel is re-established near the drain pad. If both the gate-drain spacing is small, and the voltage difference is large, then the channel may not re-establish itself.

IX. SiC Results

The measured and simulated I–V characteristics of the SiC substrate device are given in figure 58. The agreement is not as good as that for the sapphire case. The calculated pinch-off currents don't reach the measured values for low drain voltages and the curves keep on rising at the higher voltages. There are several reasons that explain this discrepancy. First of all, the initial SiC device simulation used all of the parameters found earlier for the sapphire case; the only changes incorporated were the source-gate-drain dimensions and the thermal conductivity value. The results were not good. We varied many of the same parameters that we found useful in the sapphire case, but could not get all of the three gate voltage curves to simultaneously match the experimental ones, and agree with temperatures. Only after altering the supply layer density in the AlGaN (something we did not do for the sapphire), did we start to get much better correlation. Unfortunately, time ran out for this project; so figure 58 is given as our best effort. The increase in doping in the supply layer by a factor of two brings the $V_g = -2$ curve up to the measured value. This fact shows the sensitivity of the parameter set needed for good agreement throughout the I–V plane. In particular, the supply layer is critical because electrons cannot come from anyplace else to form the conduction path. Unlike some experimental devices wherein just the unintentional residual doping supplies enough carriers to establish drain current; unless the supply layer density is sufficient, the simulation currents will all be low. Figure 59 shows the sensitivity of the drain current as the supply layer doping is increased by a factor of two. The gate equal to zero and –4 curves were determined for doping of 2×10^{18} cm^{-3}, while the three central curves were for the gate at –2 and the changing doping values. This increase shows the short-fall in the previous plot was due to the lack of carriers available in the low drain voltage regime. In other words, the increased doping prevents the gate potential from pushing too many carriers out of the channel region. We observed, but do not show, that the saturated drain current for two values of channel mobility are rather close, which shows the I–V is more sensitive to the supply doping value than the 2DEG mobility. The maximum temperature in the sapphire case was about 180 °C, and that for the SiC was closer to 120 °C. The current in the SiC case was about twice that of the sapphire case. Thus the SiC case was both cooler and with stronger fields. These factors demonstrate the challenges presented in higher power devices, smaller geometry devices; and the corresponding need for closer scrutiny. We choose, however, to ignore these factors at the present time, and leave them for future investigations. All of these factors must be considered; and the nonlinearities are unfortunately not known precisely, which makes the current very sensitive to parameters. Thus one must have "everything right" for the simulations to agree with experiment. Not to mention the fact that traps may be present, which we have neglected from the outset. Even with these caveats, we think the agreement with measurements is very satisfactory.
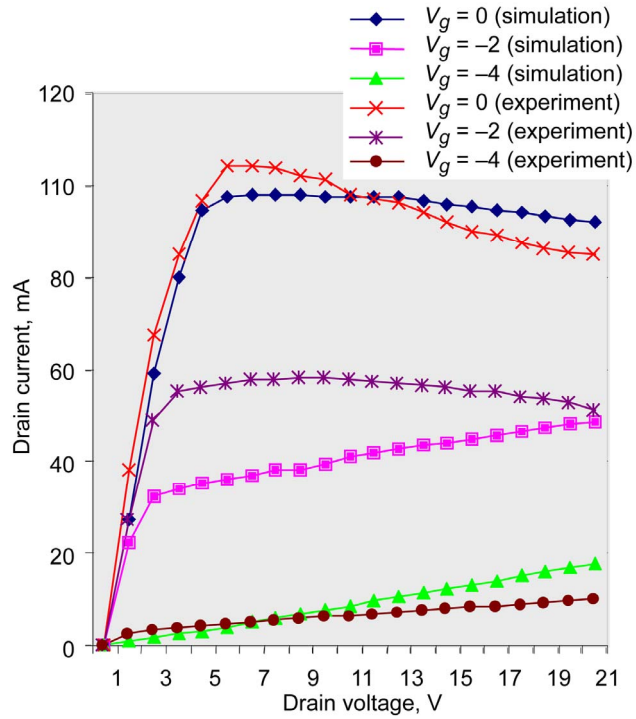
Figure 58.—Static I–V characteristics for SiC substrate HEMT. The legend indicates the simulation versus experimental curves.
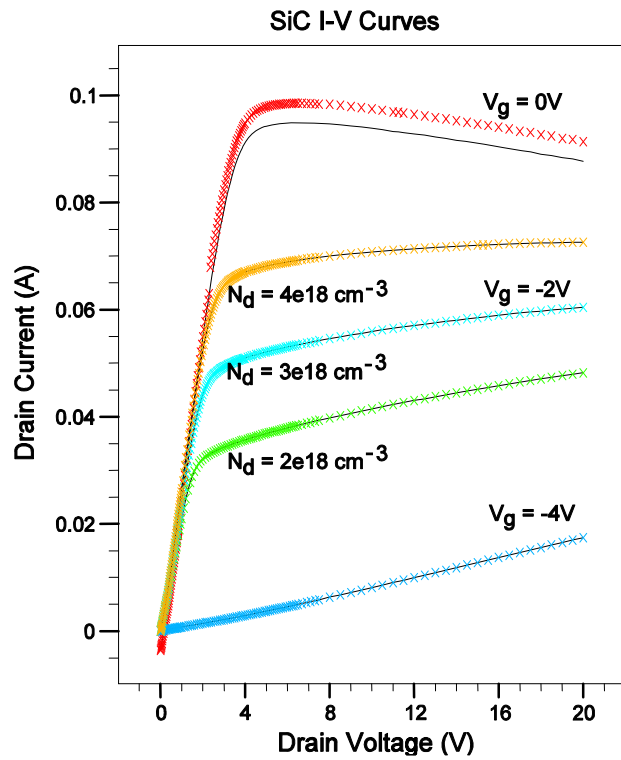

Figure 59.—The increase in the drain current for $V_g=-2$ as the doping density of the supply layer is increased by a factor of two.

Figure 60 gives an expanded view of the temperatures near 20 V. The difference in temperature between the gate edge and the bottom of the GaN layer for this case is about 15°. The results of (ref. 68) show consistently higher temperatures when just the surface temperature is measured. Thus we have some leeway when matching-up simulation and measurement. The average is not well defined, so we need only to be within say 20° to declare a good match. In other words, is the measured temperature the average of the GaN layer, or the peak value on the top surface of the AlGaN? A final remark is that the temperatures in horizontal planes in the GaN show the gate edge and source edge track each other. At low drain values they are nearly the same, and at 20 V the source is about 18° below the gate.

The electron concentration along a vertical cutline through the center of the gate is given in figure 61. Observe it is climbing from essentially 0 to 10^{14} cm^{-3} at the heterojunction. It peaks near 8×10^{18} cm^{-3} in the notch. Figure 62 depicts the temperature drop across the AlGaN, GaN, and AlN layers. In most cases the drop across the GaN layer is around 22°, while that across the AlN is near 3°. The AlGaN is only a fraction of a degree hotter than the GaN. Figure 63 gives the thermal profile through the entire device. Similar to the sapphire case, an almost linear drop occurs from around 50 μm depth down to the heat sink.
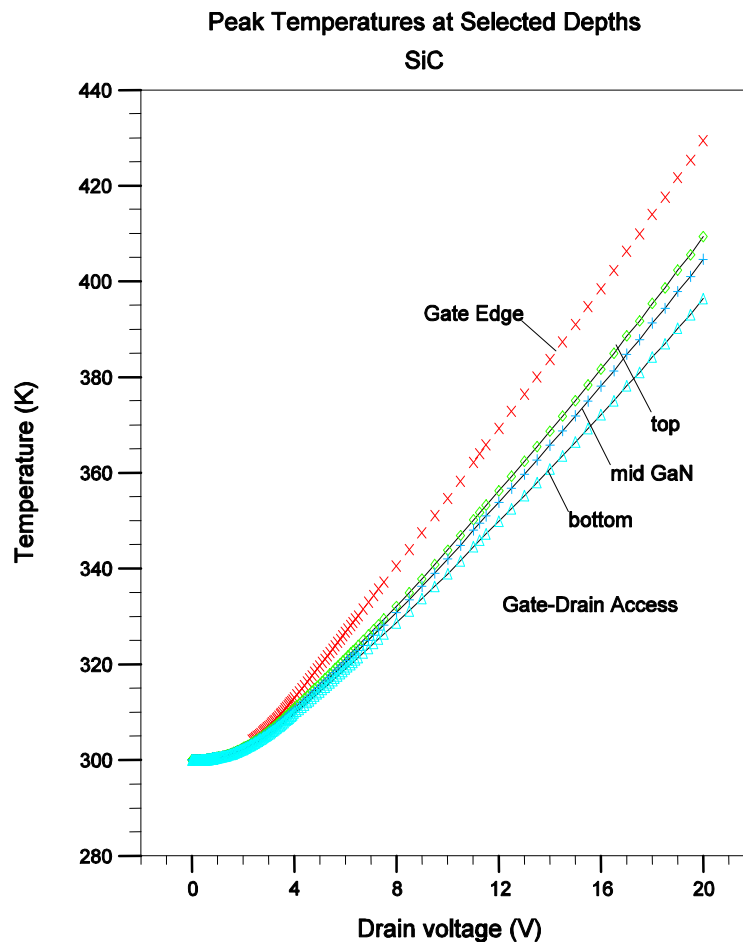

Figure 60.—Temperatures at the gate edge and in the gate-drain access region as the drain voltage increases.
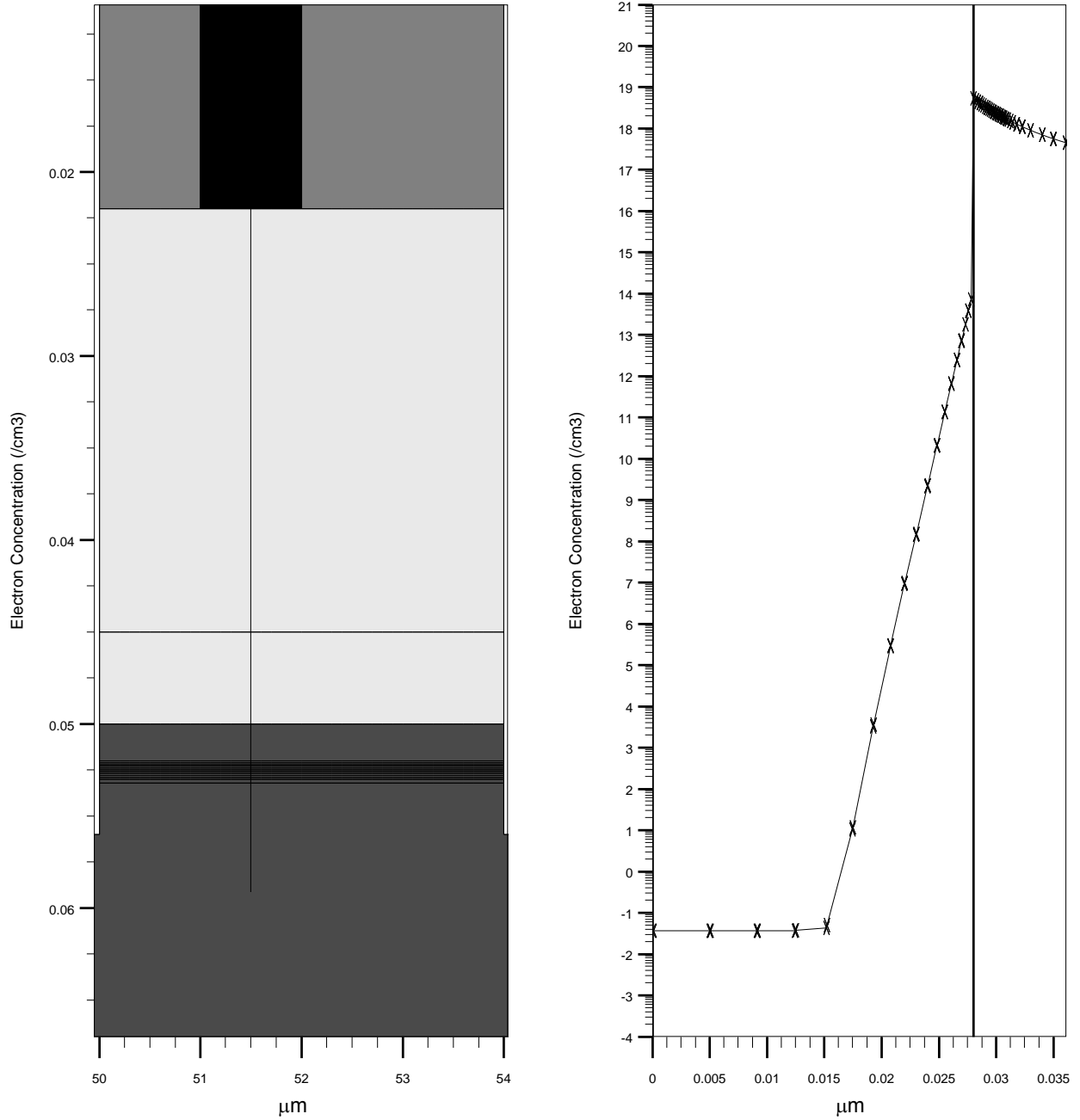
Figure 61.—The electron concentration variation with depth starting at the gate contact and traversing the heterojunction.
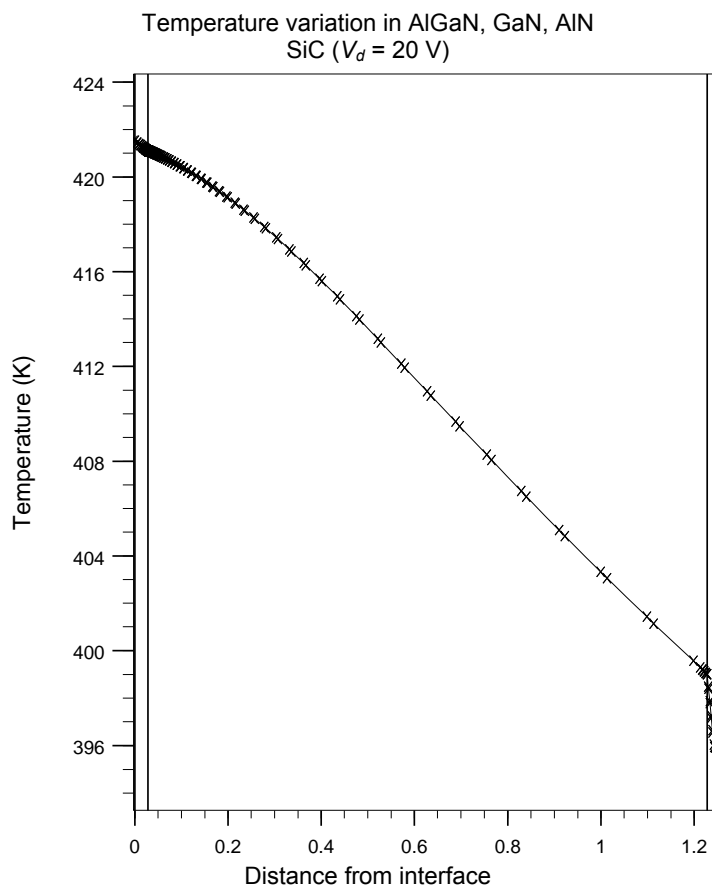
Figure 62.—Temperature profile in the AlGaN, GaN, and AlN regions. The drop across the GaN is typically in the 21° to 24° range for most conditions, such as mobility variations and doping levels.

The two line plots in figure 67 are horizontal cuts slightly below the channel for 4 V on the drain. Both show heat generation, and that on the right is at a slightly lower depth. Observe the two spikes that exist near the gate edges in the access regions. The drain access region is hotter by nearly an order of magnitude. Figure 68 gives vertical cuts at $x=52$ and 54 μm, respectively. On the left the cutline is defined by $0.476<y<0.094$, while on the right it is $0.046<y<0.131$. At $x = 52$ (gate edge), $g(x,y)$ extends 0.01 μm into the material. At $x = 54$ (drain edge) we have the ohmic spike, a drop in the AlGaN region, then the spike at the heterojunction.

Device temperature
SiC (V_d = 20 V)
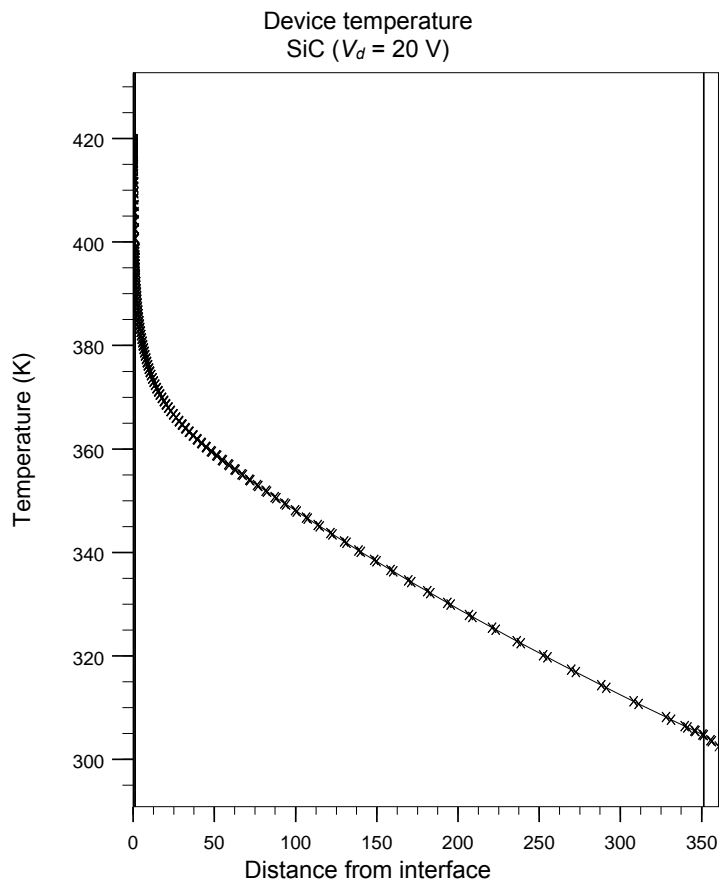
Figure 63.—The temperature profile through the entire device; from
gate to heatsink. The drop in the SiC is essentially linear for the
lower 300 μm of the substrate.

Thermal contours at 4 V on the drain (V_g = 0 V) are illustrated in figure 64. The steps in shading are only a few degrees apart as most of the device is near room temperature. Table 13 demonstrates the temperature variation at arbitrary points along the upper portion of the device.

TABLE 13.—SIMULATED TEMPERATURES AT VARIOUS
POINTS IN THE UPPER REGION OF THE HEMT

x	y	Temperature, K
0.84	3.6	307
29.9	3.64	307
51	2.8	309
76	2.8	307
100.5	3.6	307
113.4	2.8	307

The coordinates correspond to the contour plot in figure 64. Notice the GaN layer extends down to 1.2 µm, with the remainder below being SiC. All of the sampled points were chosen in the SiC. The first and last entries (not shown in fig. 64) are at the extreme left and right sides of the unit. The baseplate is kept at 300 K.

The heat generation contour plots are exhibited in figures 65 and 66. The drain is at 4 V, and notice the heat generated at the ohmic contacts is comparable to that generated in the channel. The small bump at the AlN interface is due to a non-negligible amount of current existing there. A closer view of the channel region is shown in figure 66; the behavior at the source pad is interesting.
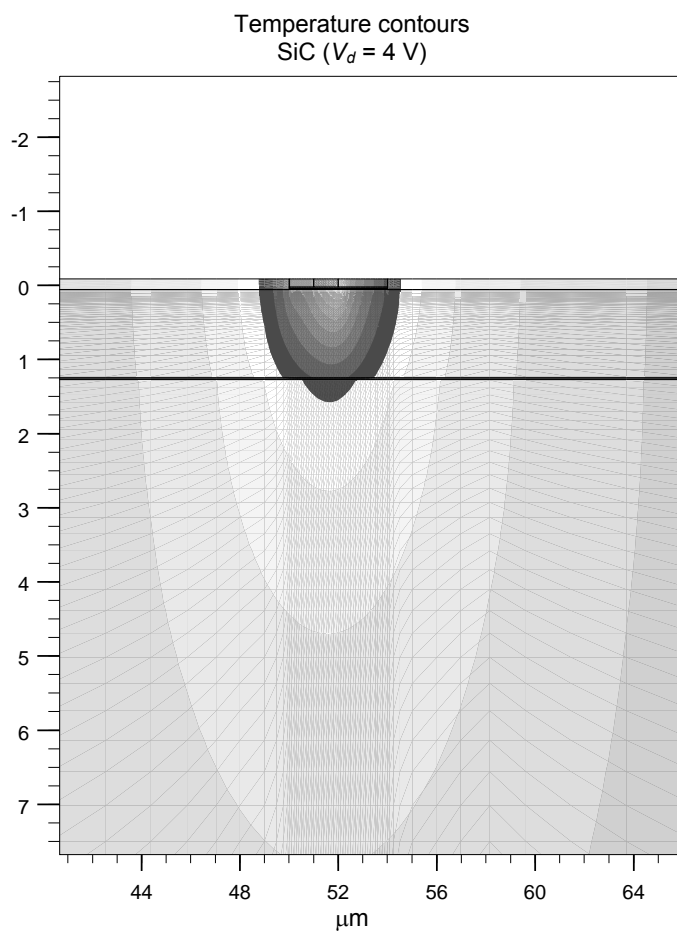
Figure 64.—Constant temperature contours centered on the gate edge for bias (V_g = 0 V, V_d = 4 V). Observe the interesting focusing effect of the low conductivity AlN layer.
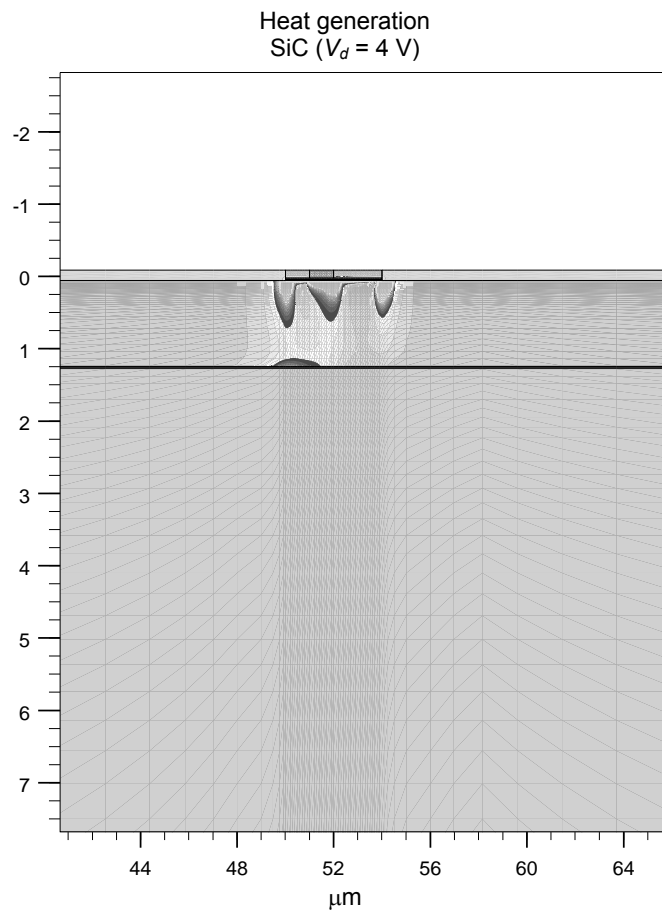
Figure 65.—Heat generation at 4 V on the drain. The heat
generated at the contacts is comparable to that developed in
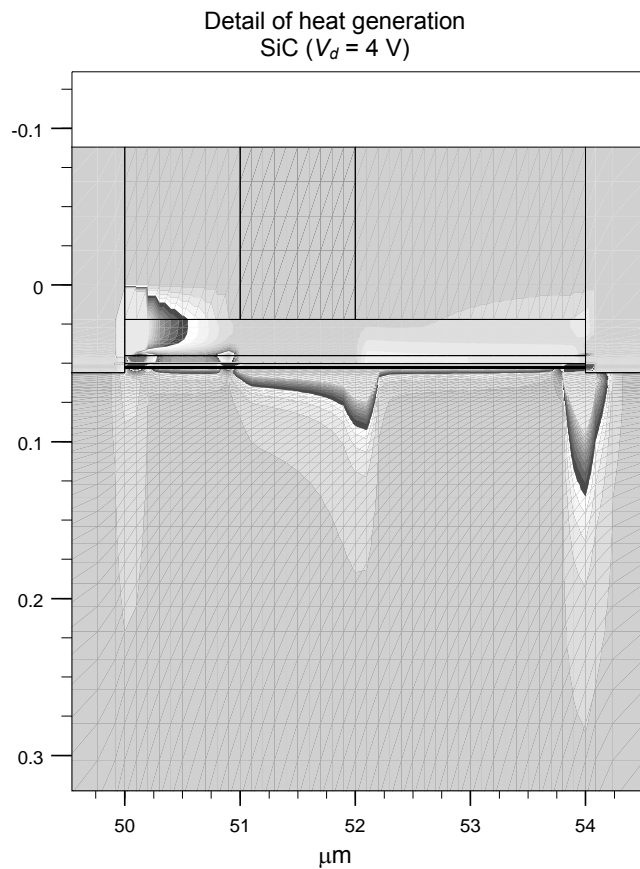the channel.

Figure 66.—Tighter view of the heat generation function
    $g(x,y)$. The behavior near the source pad is interesting;
    the temperature distribution of the air between the
    source and gate metal pads is similar to that in the
    solid AlGaN.
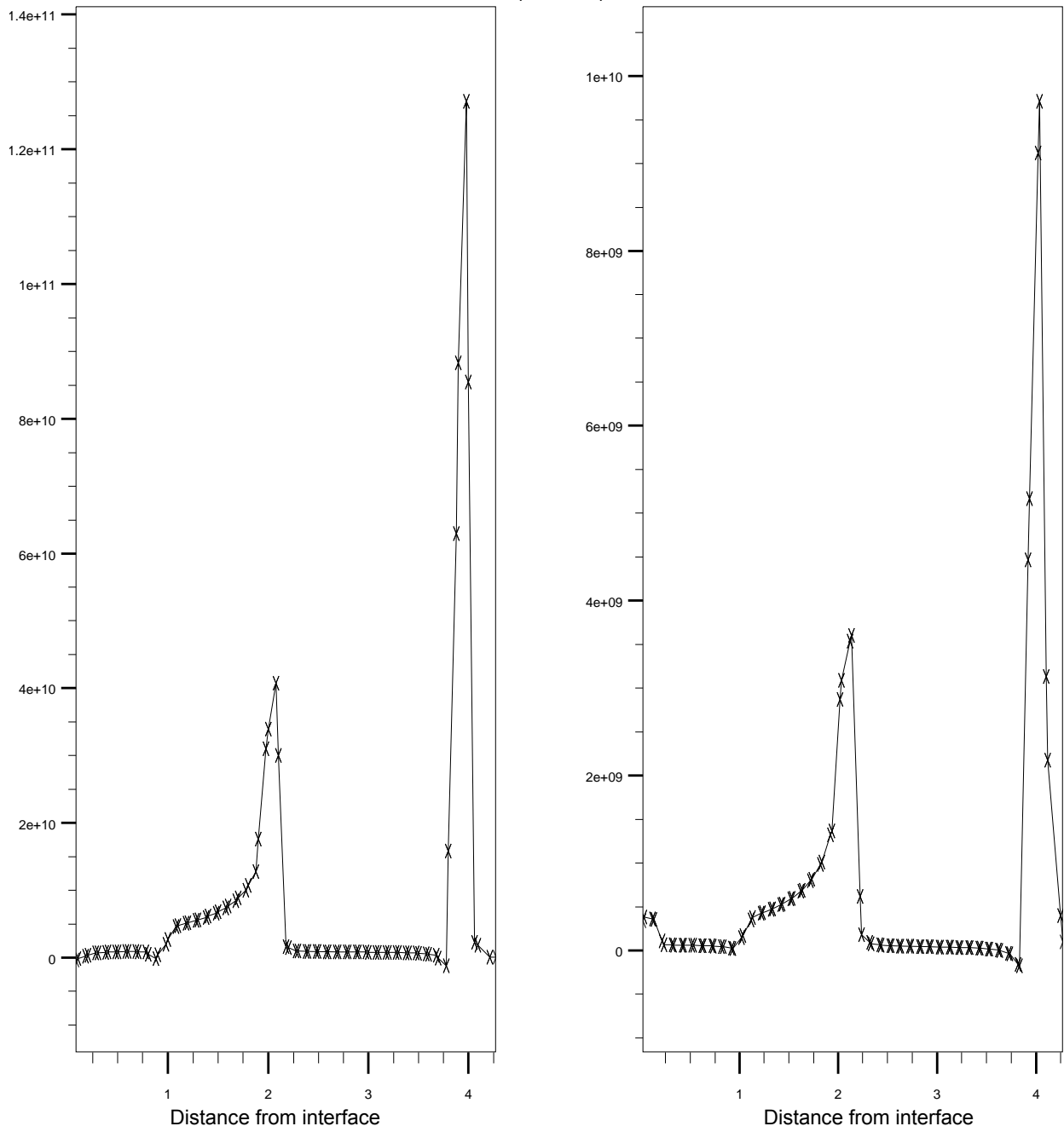
Figure 67.—Horizontal cutlines showing the heat generation at two depths below the channel. The spikes occur in the access regions about the 1 μm gate.
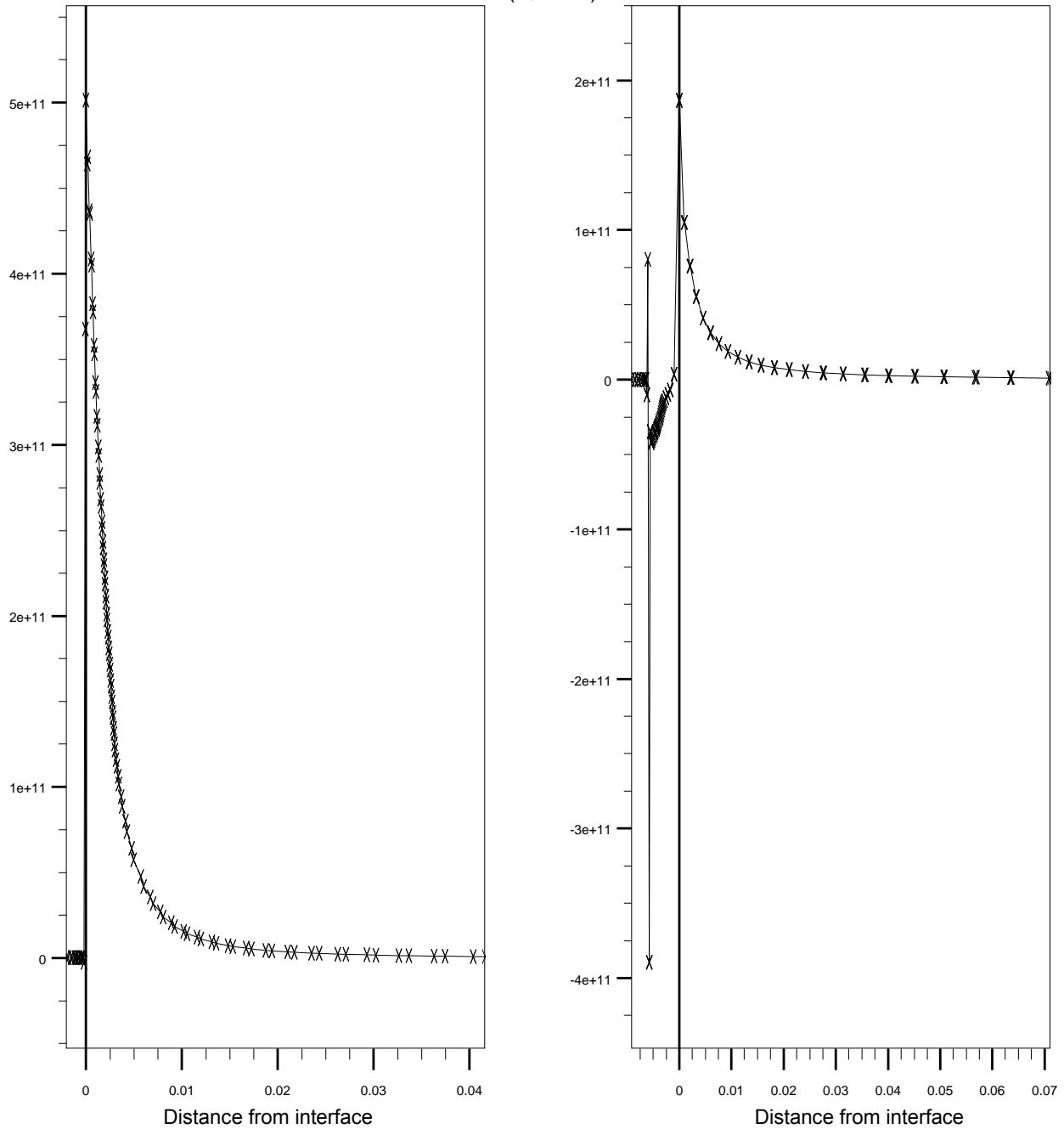
Figure 68.—Vertical cuts showing $g(x,y)$ versus y at planes corresponding to the gate and drain edges (left and right panels, respectively). On the drain edge the first spike is due to the ohmic contact.

Figure 69 demonstrates the mobility and electric field magnitude for 5 V on the drain. The horizontal cutline is at $y = 0.076$ μm. The field peaks at the source, gate, and drain edges respectively. Figure 70 shows the entire simulation area and elucidates the temperatures at selected points in the structure for the bias point ($V_g = 0$ V, $V_d = 5$ V). The chip edges on the top surface are at 310 K and the base is at 300 K. This is in contrast to Kuball's assumption that the baseplate rises to nearly the value found at the chip edges.
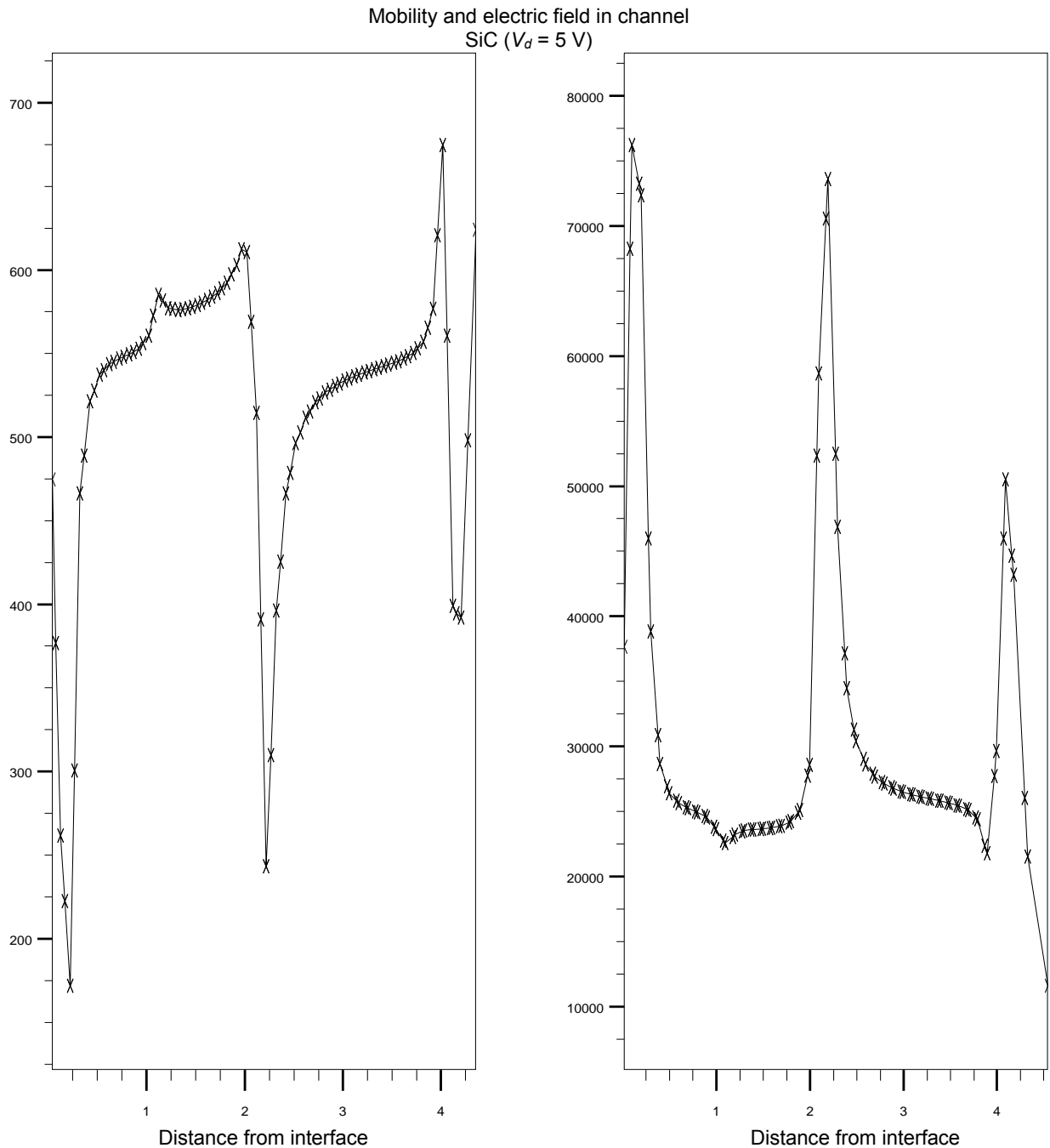
Figure 69.—The mobility and absolute value of the electric field along a horizontal cutline near the channel.

Figure 71 is a contour plot (V_d = 5 V) with nearly the same scale for both axes. Therefore, the isotherms have nearly their true shape. The drop is only about 4° from the point in the light region about the gate and the lowest contour. Again the isotherms are nearly horizontal at the depth of 50 μm. Figure 72 is a similar plot for the drain increased to 8 V.

Figure 73 shows the magnitude of the current density in the AlGaN/GaN regions. Table 14 gives the values at the specified points.

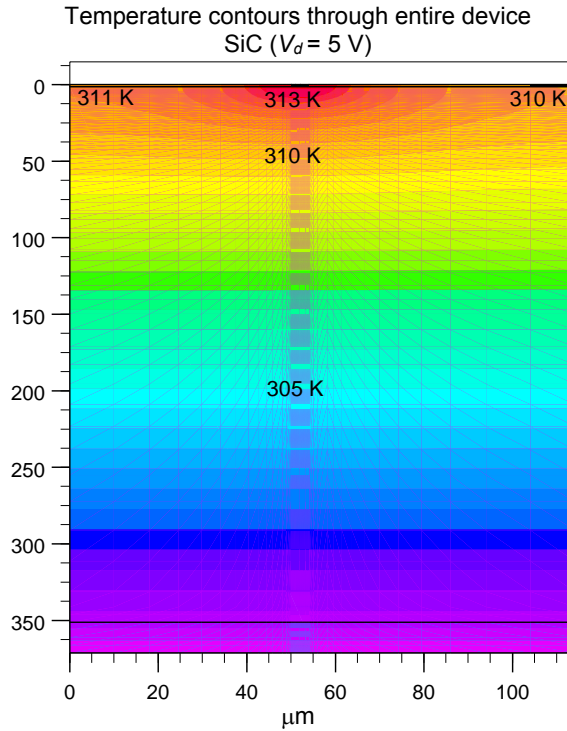Temperature contours through entire device
SiC (V_d = 5 V)

Figure 70.—View of the entire device showing the temperatures at specific points. The gate is at 0 and the drain is at 5 V. The drain current is about 98 mA.

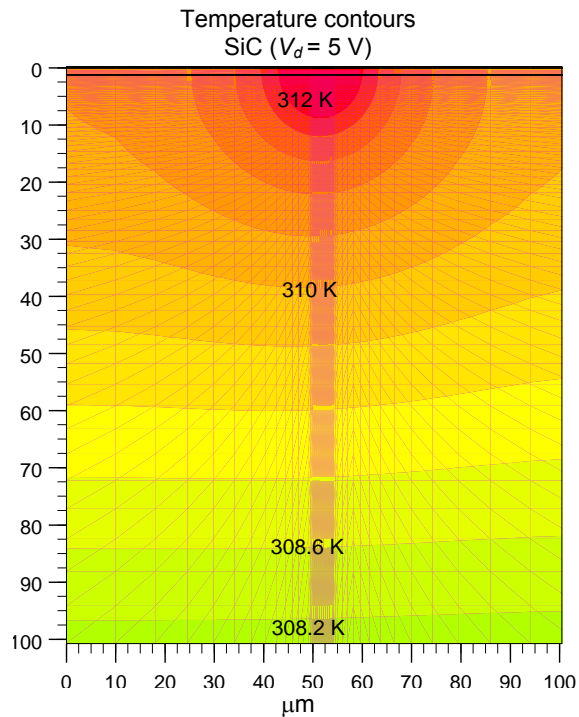Temperature contours
SiC (V_d = 5 V)

Figure 71.—Contour plot at 5 V with nearly identical scales for vertical and horizontal axes. The true shapes of the isotherms are seen clearly. Observe that the temperature drops about 4° from top to bottom.
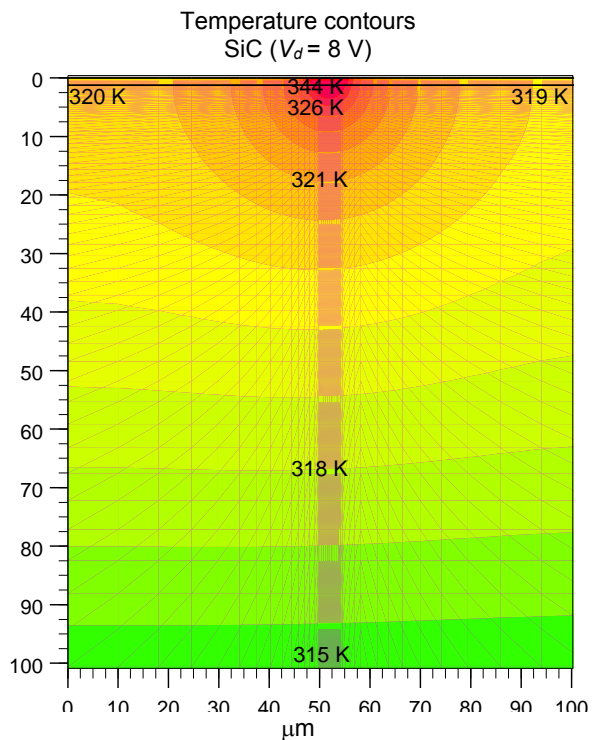
Figure 72.—True shape of contours for 8 V on the drain.
Here, about 15° is dropped from channel to bottom
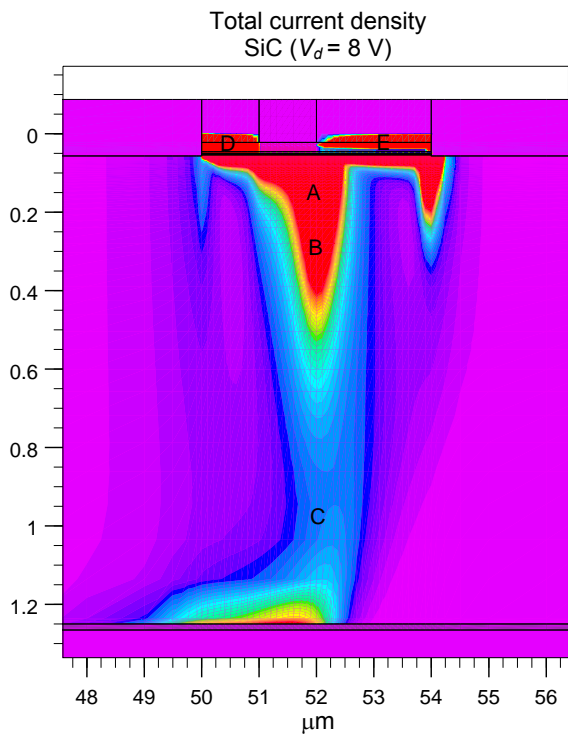(about 106 μm away).

Figure 73.—Current density contours for V_d = 8 V. The
geometry of the device causes the small portion at the
GaN/AlN interface.

TABLE 14.—THE MAGNITUDE OF THE CURRENT DENSITY IN
THE ACTIVE DEVICE REGION FOR 8 V ON THE DRAIN

Point	x, µm	y, µm	$\|J(x,y)\|$, A/cm^2
A	52.0	0.122	148,702
B	52.0	0.283	23,624
C	52.0	0.979	2,774
D	50.4	0.034	5,222,558
E	53.2	0.052	7,949,000

Figure 74 is the x-component of the current density, for the same bias point ($V_g = 0$ V, $V_d = 8$ V). Table 15 gives the values at points A, B, and C.

Figure 75 accompanies the two previous figures, as it displays the y-component of the current density.

Figure 76 is a horizontal cutline plot showing J_y for $V_d = 8$ V. The two spikes occur at the gate edge and the drain contact. The small dip at 1 µm is on the source-side gate edge.

TABLE 15.—THE x-COMPONENT OF THE CURRENT DENSITY
J IN THE ACTIVE REGION AT 8 V ON THE DRAIN

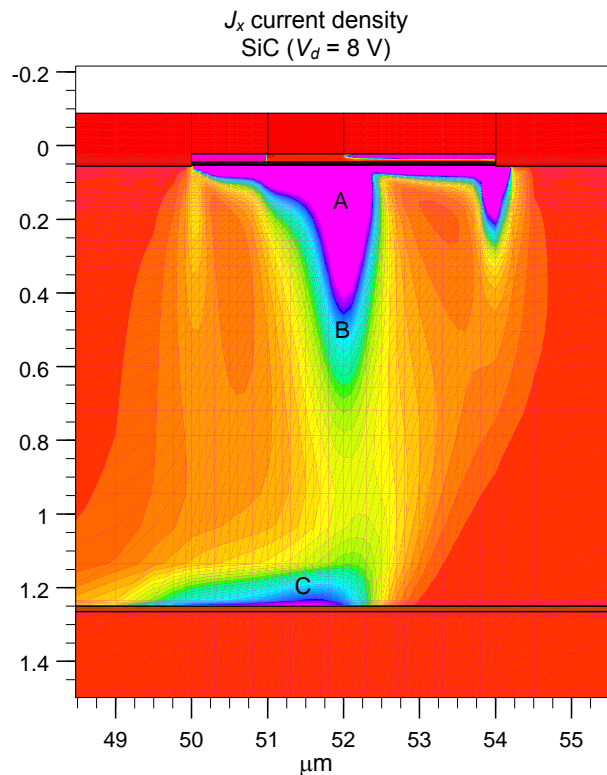| Point	x, µm	y, µm	$J(x,y)$, A/cm^2
A	52.0	0.204	50,608
B	52.0	0.531	6,279
C	51.7	1.23	8,079

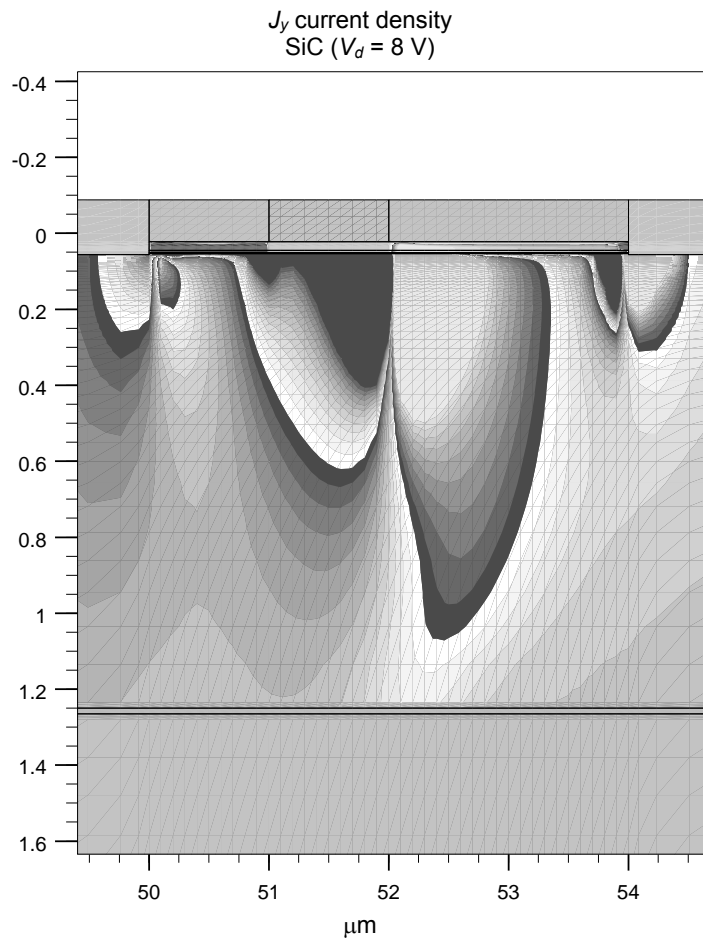Figure 74.—Contour plot of J_x at $V_d = 8$ V.

Figure 75.—Contour plot of J_y at V_d = 8 V. Notice the absence (or change in opposite direction) at the gate edge. The current is pushed down into the GaN layer at the gate edge.
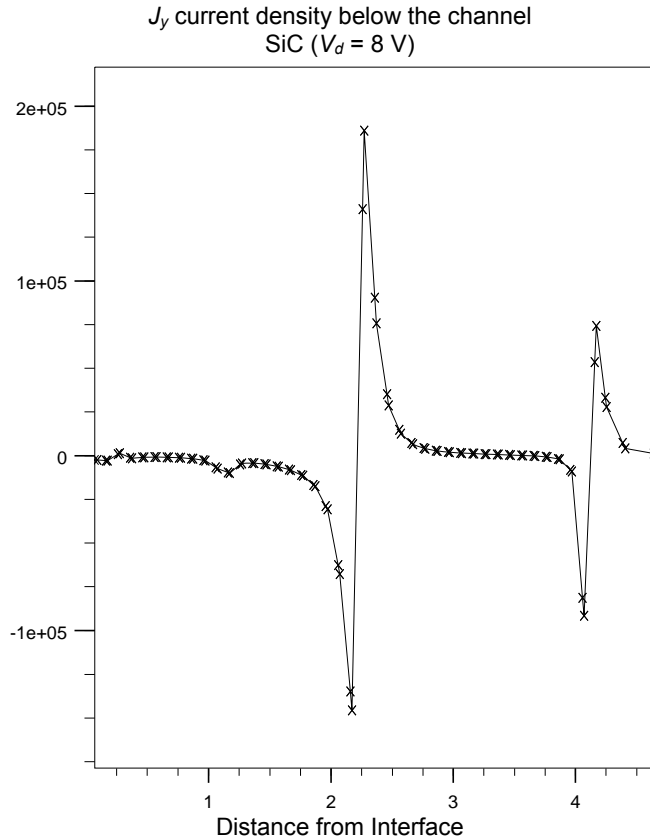
Figure 76.—Horizontal cutline demonstrating the behavior of J_y slightly below the channel.

The contour panel in figure 77 is that of J_x, while the cutline plot on the right encompasses the heterojunction (see cutline 1 in the left panel). Table 16 gives the values at the indicated points. Point A in the AlGaN has considerable current, while point B (in the undoped region of the AlGaN) has almost none. Point C is at the heterojunction and the current density peaks there. Point D is just below the transition layers, and is the start of the bulk GaN region. Finally point E is deep into the GaN layer.

TABLE 16—THE x-COMPONENT OF THE CURRENT
DENSITY J FOR THE FIVE POINTS IN FIGURE 77
UNDER THE CENTER OF THE GATE ($V_d = 8$ V).

Point	J_x Current Density (A/cm²)
A	-2.6×10^5
B	-238
C	-1.75×10^7
D	-1.24×10^6
E	-2106

The conduction band edge at three vertical planes is illustrated in figure 78. The drain is at 8 V. The coordinates of the planes and ends of the cutlines are: $x = 50.5$, $-0.009 < y < -0.095$ (midway between source and gate); $x = 51.5$, $-0.024 < y < -0.1$ (mid-gate); $x = 53$, $-0.009 < y < -0.093$ (midway between gate and drain). The notch remains all along the channel for this bias point ($V_g = 0$ V, $V_d = 8$ V).
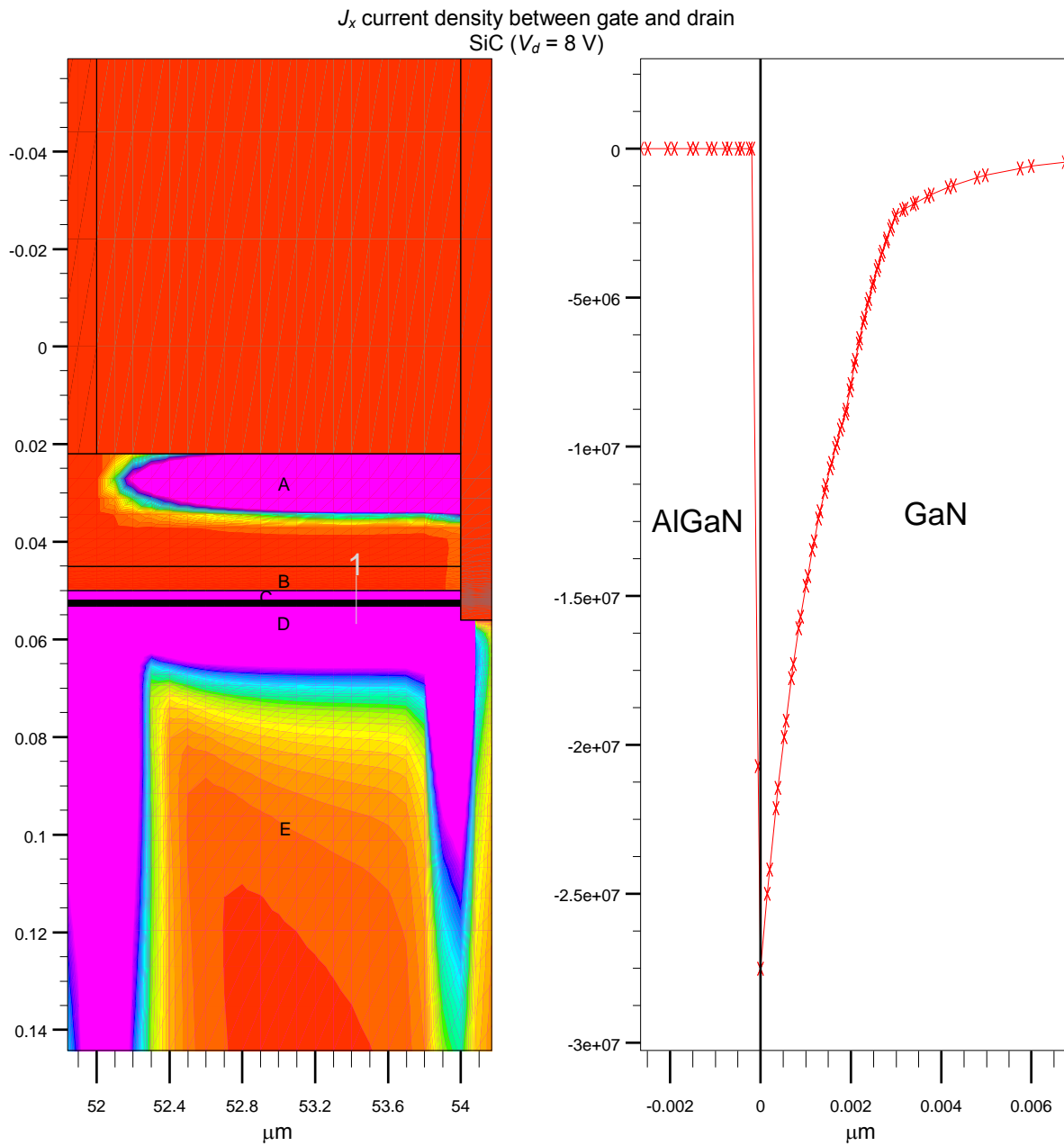
Figure 77.—Conduction current contours (J_x), and its values along cutline 1. Observe the current is contained in the channel region (the plane of the heterojunction and about 0.003 μm (30 Å).
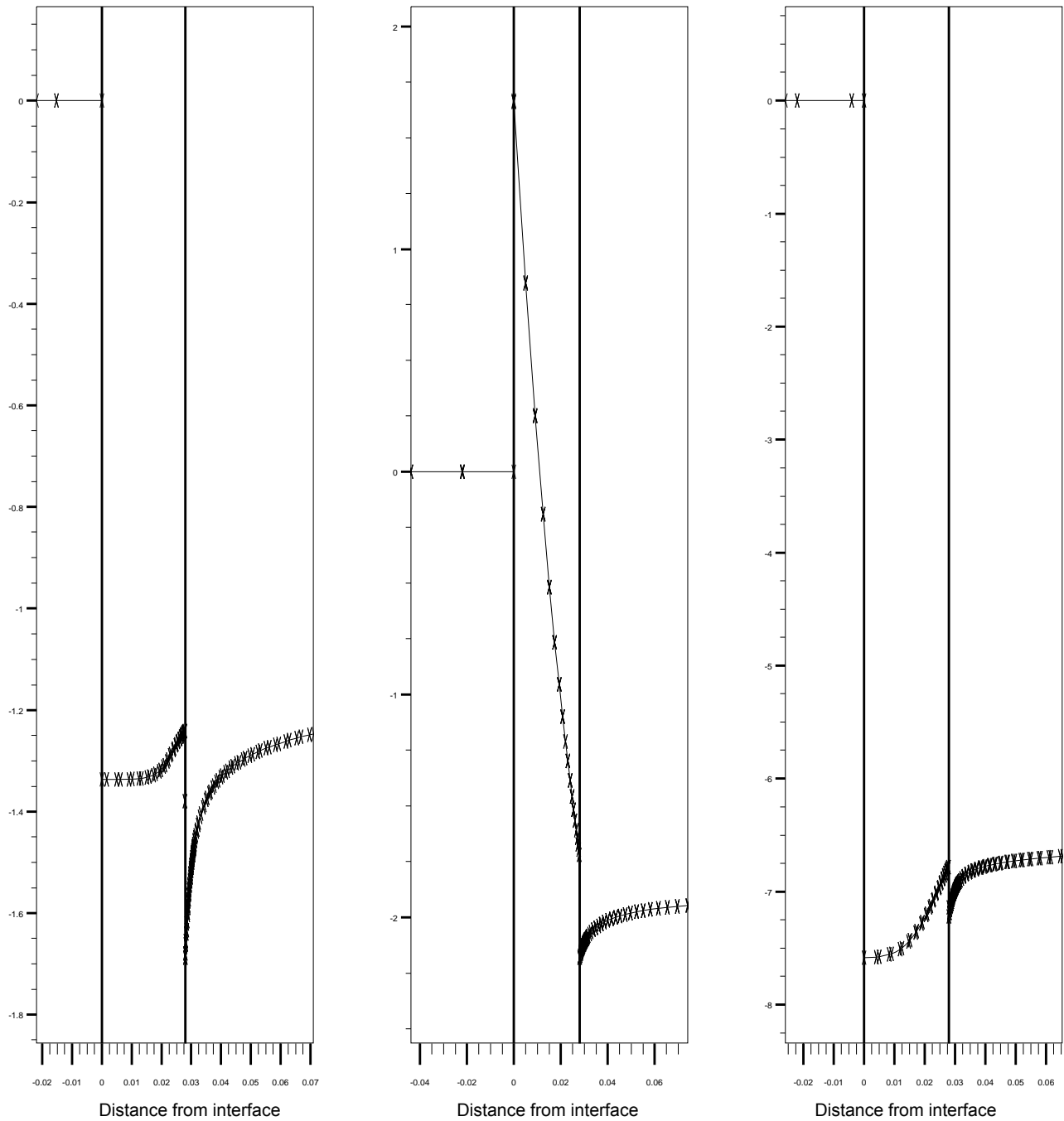
Figure 78.—Conduction band edge profiles at mid source-gate access, center of gate, and mid gate-drain access region.

The heat generation plot for 8 V on the drain is shown in figure 79. Notice values in contours that contain the points A and B differ by four orders of magnitude. This demonstrates the large heat spike at the gate edge, and why an equivalent heat source close to the S-D distance causes the analytical expression of Masana to agree with simulations and measurements.

Figures 80 and 81 are horizontal cutline plots of $g(x,y)$ at $y = 0.0474$ for 8 and 20 V on the drain. The ranges of x are: $50 < x < 54.2$, and $49.9 < x < 54.2$ respectively. Notice the spike (at 8 V) at the source contact is the largest at this depth with the gate—drain access being the next largest. However, at 20 V the drain spike starts to develop, but is still an order of magnitude below the source's value. The values in the access regions around the gate are nearly the same in both cases; about 4×10^9 W/cm^3.

Figures 82 to 85 are thermal plots for $V_d = 20$ V. The axes are nearly the same in figure 82 to show the true shapes of the isotherms. A closer view is presented in figure 83 to demonstrate the high temperature column beneath the gate edge. Figure 84 displays the entire device; notice the chip edges are about 58° above the heatsink. The heatsink was held at 300 K, and its top surface was determined to be 304 K. Apparently the 25 μm thick copper bottom surface is held at 300 K, and the boundary condition there is considered to be Dirichlet. The area of the copper surface is 113×200 μm^2 and its thickness is 25 μm. Using the general expression for thermal resistance $R_{th} = l/(\kappa A)$, and using $\kappa = 4$ °C/W we obtain $R_{th} = 2.765$ °C/W. For our simulation we obtained about 91 mA at 20 V, so the dissipation was 1.82 W. This yields a temperature drop of 5 °C; which agrees within 1° of the simulation. A cutline through the gate edge down into the SiC is depicted in figure 85. The channel is at 430 K and the GaN/AlN interface is at 400 K. The drop across the AlN is about 3°.

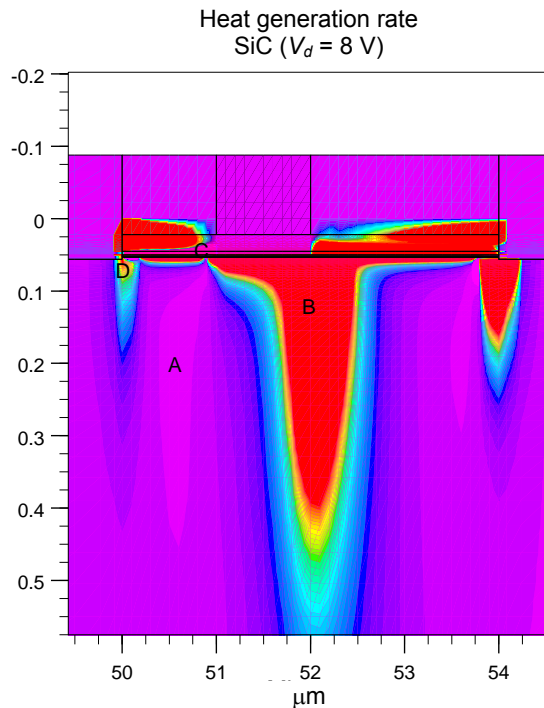Figure 79.—Heat generation around the channel and into the GaN layer.
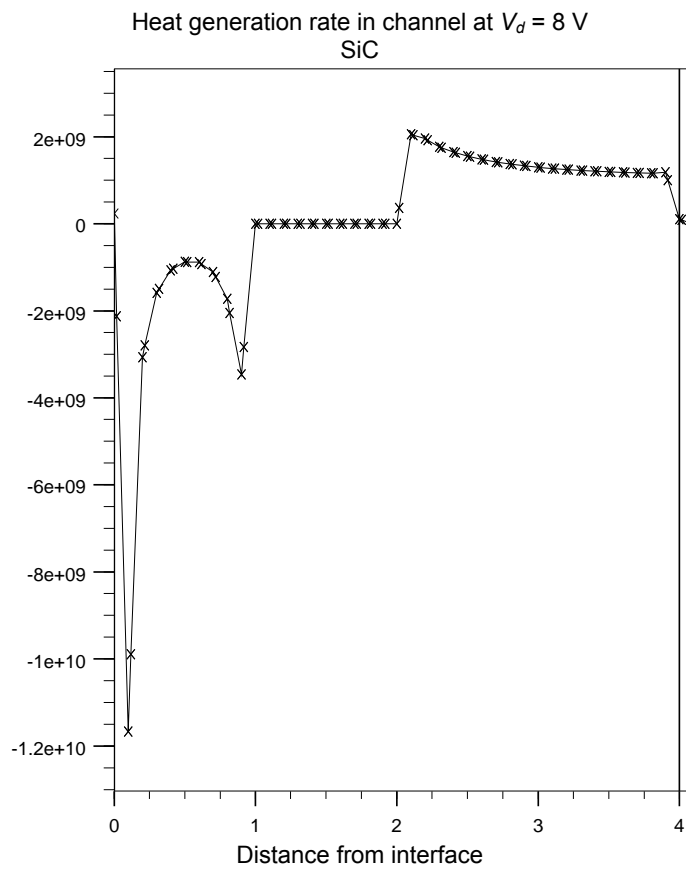
Figure 80.—Heat generation along horizontal cutline in the
channel area at 8 V.

Heat generation rate in channel at V_d = 20 V
SiC

Distance from interface
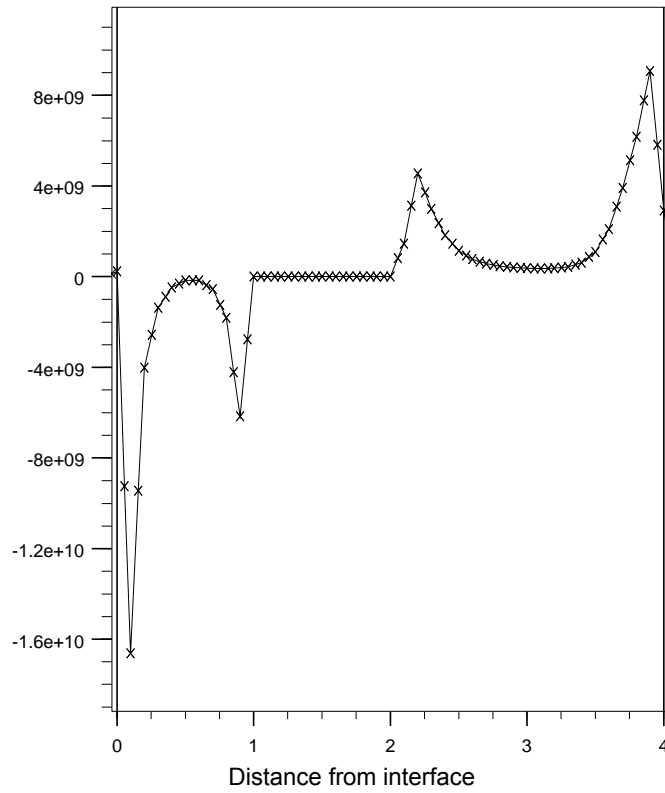
Figure 81.—Heat generation along same cutline as figure 80, but now at 20 V.

True shape of temperature contours
SiC (V_d = 20 V)

μm
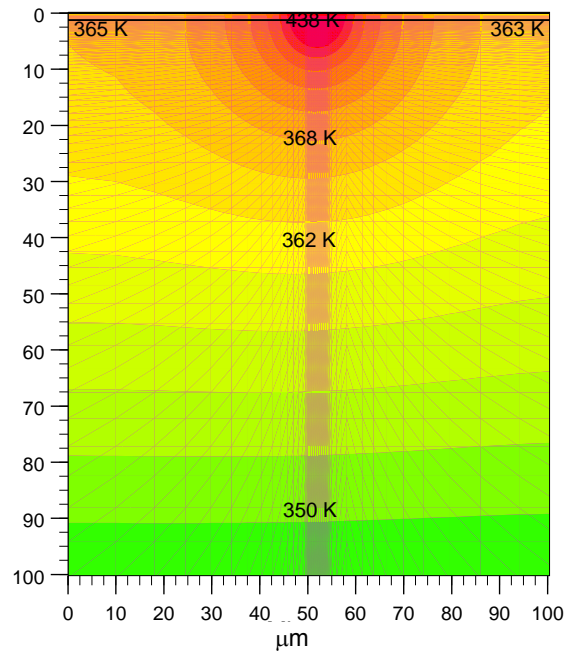
Figure 82.—True shape of the isotherms for 20 V.

Temperature contours under gate
SiC (V_d = 20 V)
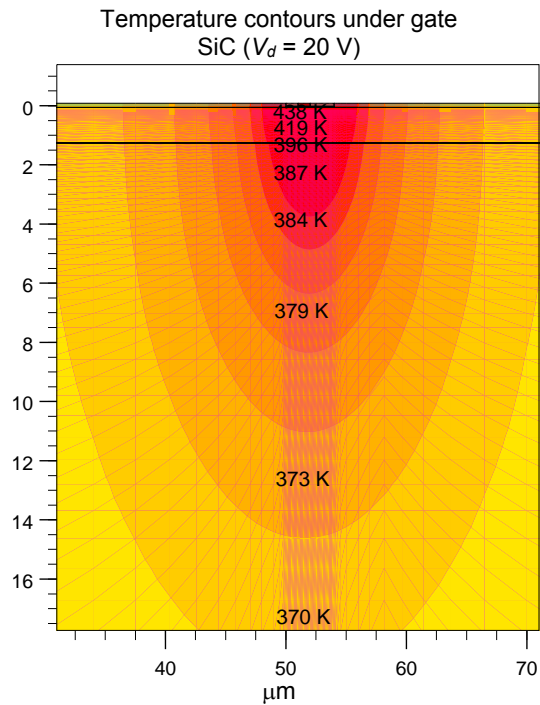
Figure 83.—Contours of temperature centered on the plane of the gate edge for 20 V bias, the gate is at 0 V.

Temperature contours for entire device
SiC (V_d = 20 V, I_d = 91 mA)
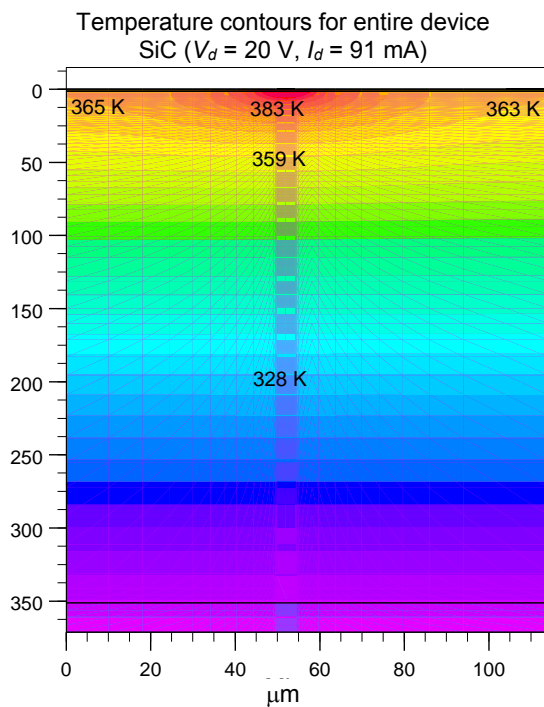
Figure 84.—Contour plot of the entire device. The temperatures at the upper edges are around 60° hotter than the heat sink. The isotherms are parallel for depths below 50 µm.
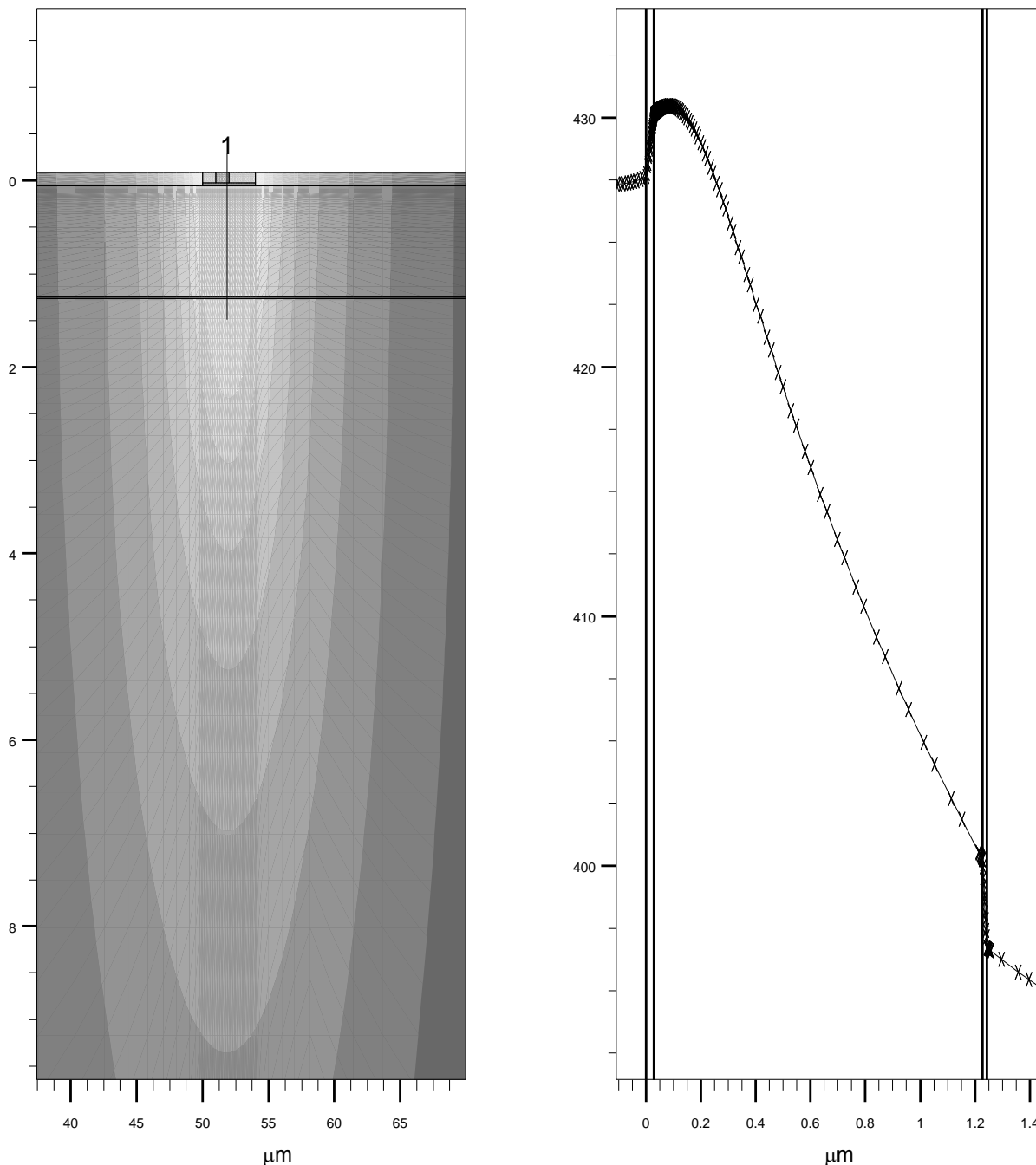
Figure 85.—Temperature profile though the upper portion of the HEMT. The AlGaN and AlN layers are on the left and right sides in the right panel.

The final group of figures investigates the "singularity" behavior just under the gate edge. Figure 86 displays a very thin portion of the heterojunction; the contours are those of total current density. The spike region is extremely devoid of current. Notice it extends below the transition layers which means the "channel" no longer exists along the heterojunction. In other words the carriers are in a channel to the left, then they dip down into the bulk GaN (go around the notch) then return to the heterojunction channel on

the right. Figure 87 shows this effect from a wider vantage point. The horizontal cutline (designated 1 in the left panel) demonstrates the reduction of current at the gate edge plane ($x = 52$ µm) as seen in the right panel. The value at the notch is 4000 A/cm^2, which is three orders of magnitude below that on either end of the cutline. Figure 88 shows the conduction band edge along this plane, and observe the notch has been removed by the electric field due to the gate and drain potentials. Figure 89 is a closer view of the band edge which demonstrates the effective dissolution of the channel in this region. Figure 90 illuminates the behavior of the magnitude of the electric field. The value at the notch is 4.6×10^4 V/cm. The panel on the left is a horizontal cut at the plane $y = 0.0502$ and $50.4 < x < 53.4$. While that on the right is a vertical one with $x = 51.7$, $0.0494 < y < 0.0535$. The step in the field is due to the sheet charge placed at the heterojunction.

   Finally figure 91 demonstrates the singularity in another fashion. The two vertical cutlines are given in the left panel. The middle panel shows the carrier density at the heterojunction to be about 2×10^{14}/cm^3 at the singularity. However, at the midpoint of the access region it is about 4×10^{19}/cm^3, which is typical of that in the channel in most devices.
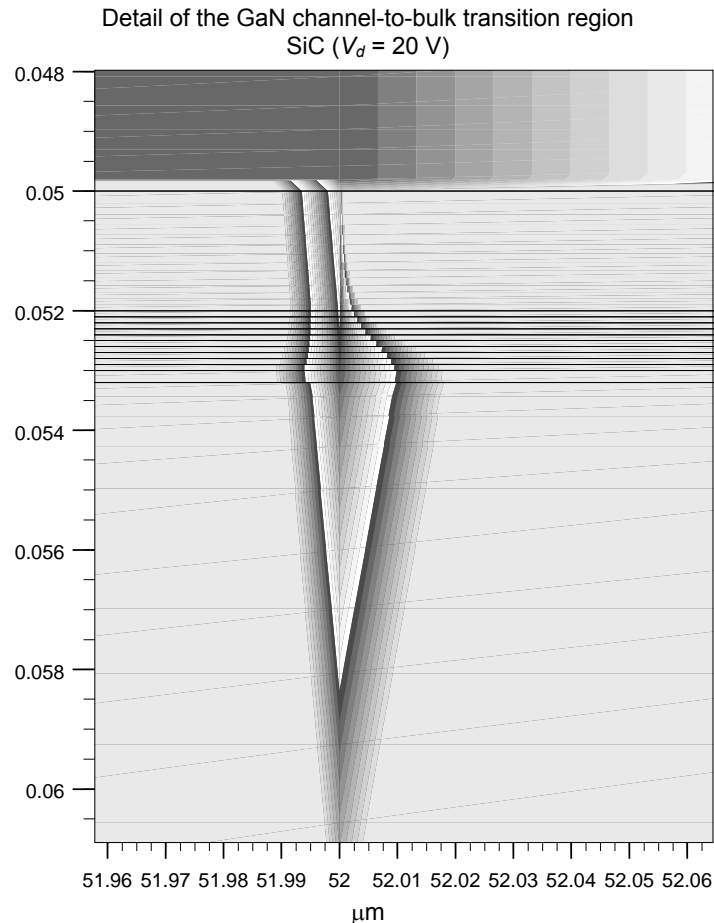
Figure 86.—Close view of the AlGaN/GaN heterojunction plane at 0.05 µm and the thin transition layers separating the "channel" properties from the bulk GaN properties.

Current density under gate edge
SiC (V_d = 20 V)
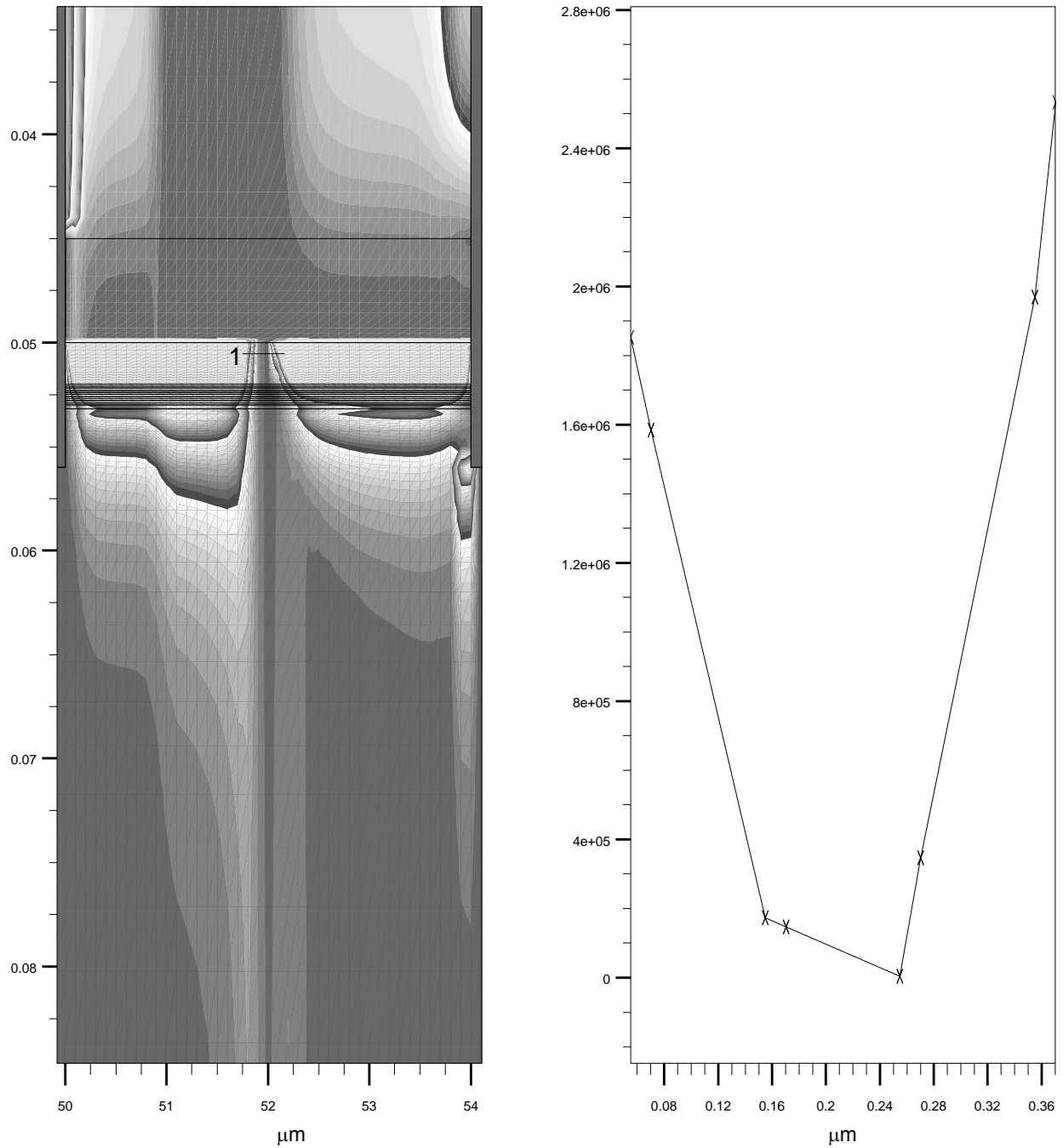
Figure 87.—Current density variation horizontally in the singularity region. The value at the notch is 4000 A/cm^2.
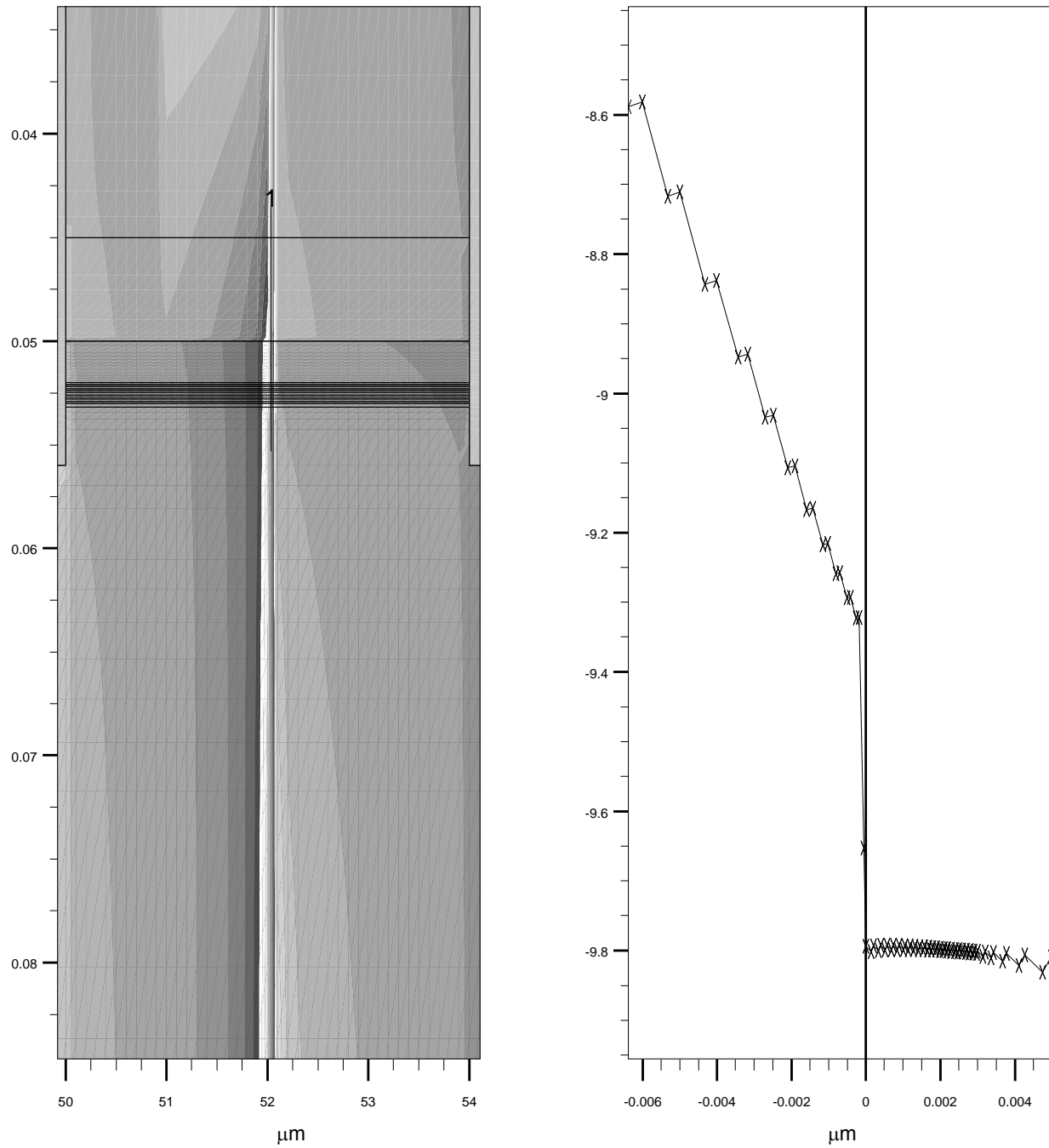
Figure 88.—Conduction energy band edge illustrating the dissolution of the notch to contain the 2DEG.
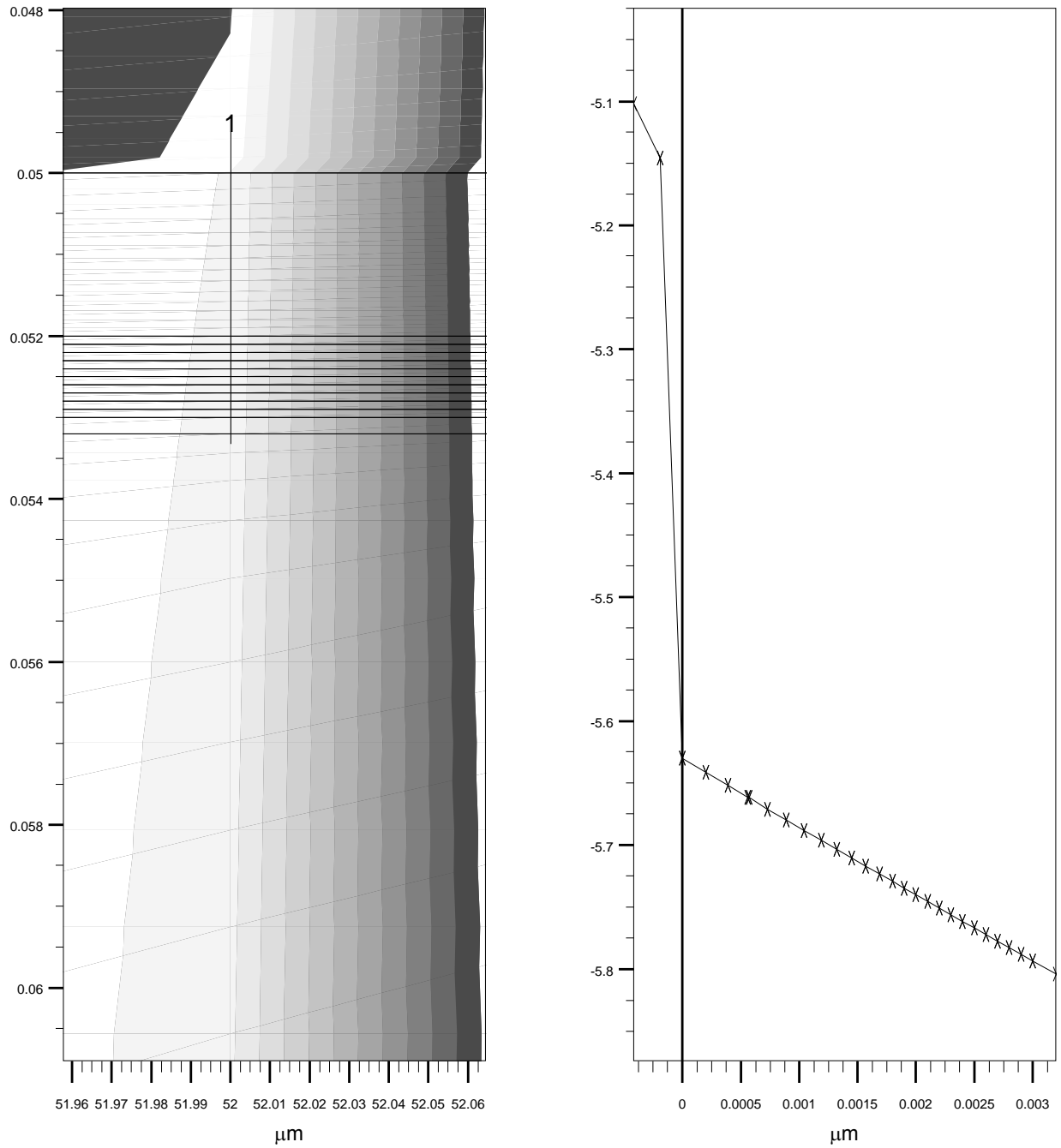
Figure 89.—A closer view of the conduction band edge in the region of the singularity.
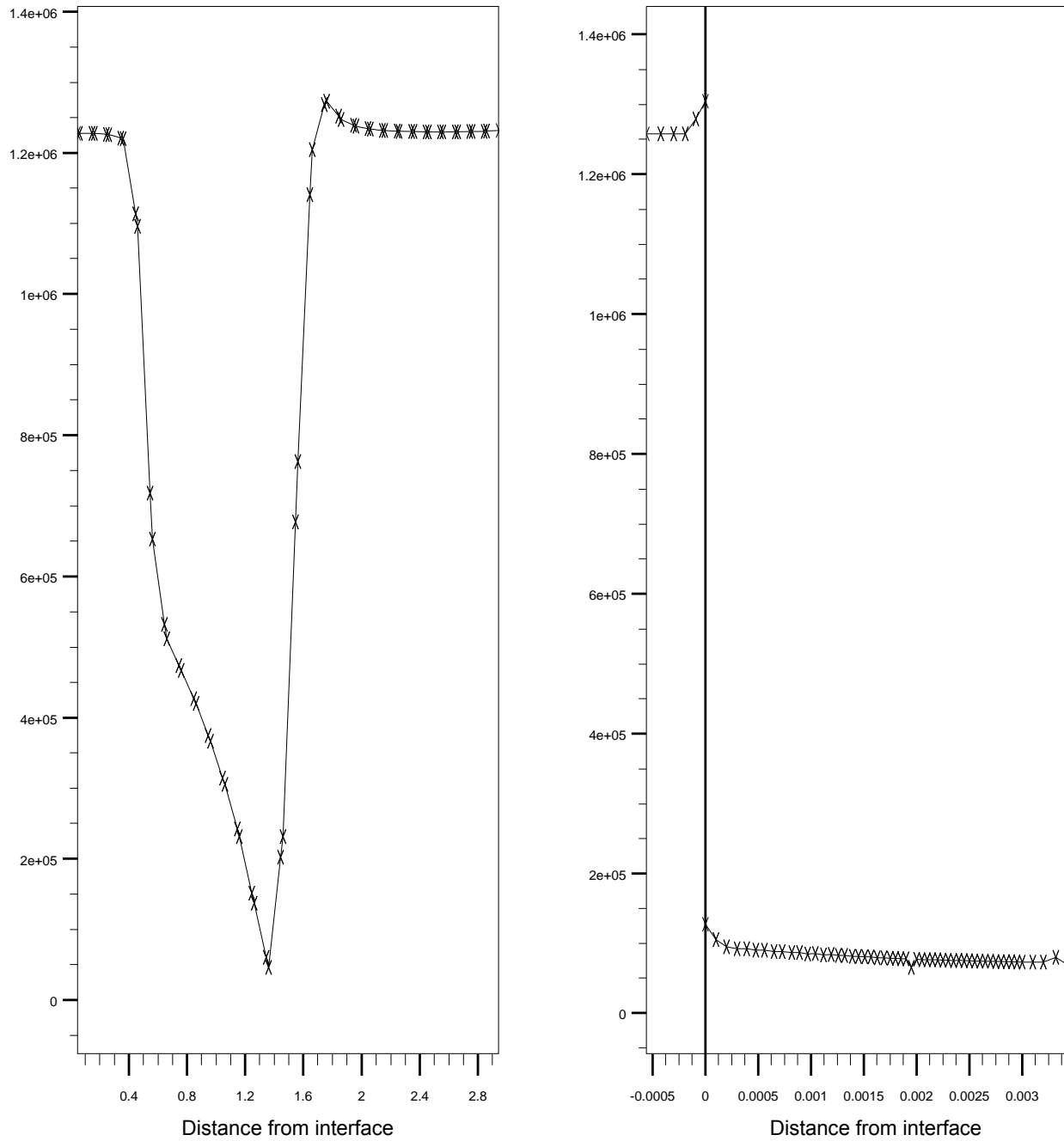
Figure 90.—Variation of the magnitude of the electric field in the singularity region. The left and right panels are horizontal and vertical cuts respectively.

Figure 91.—The carrier density at the gate edge and midway the gate-drain access region. Notice the carriers in the singularity region are about 5 orders of magnitude below the normal value contained in the conduction band notch of a typical heterojunction.

X. Multiconductor Results

This section covers the multi-finger comparisons with Kuball's data (ref. 17). The measured temperatures and schematic of the device are given in figure 92. The dotted curves that blend with the measured solid peaks were derived from a thermal simulator. The device is designated as the 8×250 μm^2 unit with 25 μm spacing between gates. Table 17 displays the measured temperatures on all eight gates.

Gate no.	1	2	3	4	5	6	7	8
T, °C	207	215	233	224	234	215	218	206

Close scrutiny reveals an interesting pattern; the two gates in the center (numbers 4 and 5) differ by 10°. Yet gates 3 and 5 are at the same temperature. This either demonstrates the uncertainty in the measurements or a nonuniformity in the device. At any rate, we can say the outermost gates are at the same temperature and those in the center are about 20° hotter.

In table 18 we present the ratios of temperatures; the second column gives that for the measured values; while columns 3 and 4 display the predicted values using either the distributed or partial inductance approaches.

TABLE 18.—RATIOS OF GATE TEMPERATURES; MEASURED, AND PREDICTED
BY THE TWO INDUCTANCE METHODS (DISTRIBUTED AND PARTIAL)

Ratio	Measured	Distributed inductance	Partial inductance
T_2/T_1	1.04	1.09	1.03
T_3/T_1	1.13	1.14	1.04
T_4/T_1	1.08	1.16	1.05
T_5/T_1	1.13	1.16	1.05
T_6/T_1	1.13	1.14	1.04
T_7/T_1	1.05	1.09	1.03
T_8/T_1	1	1	1

Figure 92.—Kuball's measured temperatures (°C) on an eight gate device on SiC. The perspective shows the gates numbered from left to right, along with the dimensions of the chip. The gate length and S-D separation are 0.8 and 5 μm respectively.

Figure 93.—Display of the ratios of measured temperatures
and the corresponding ratios for the distributed and
partial inductance approximations. $T(5)/T(1)$ is the ratio
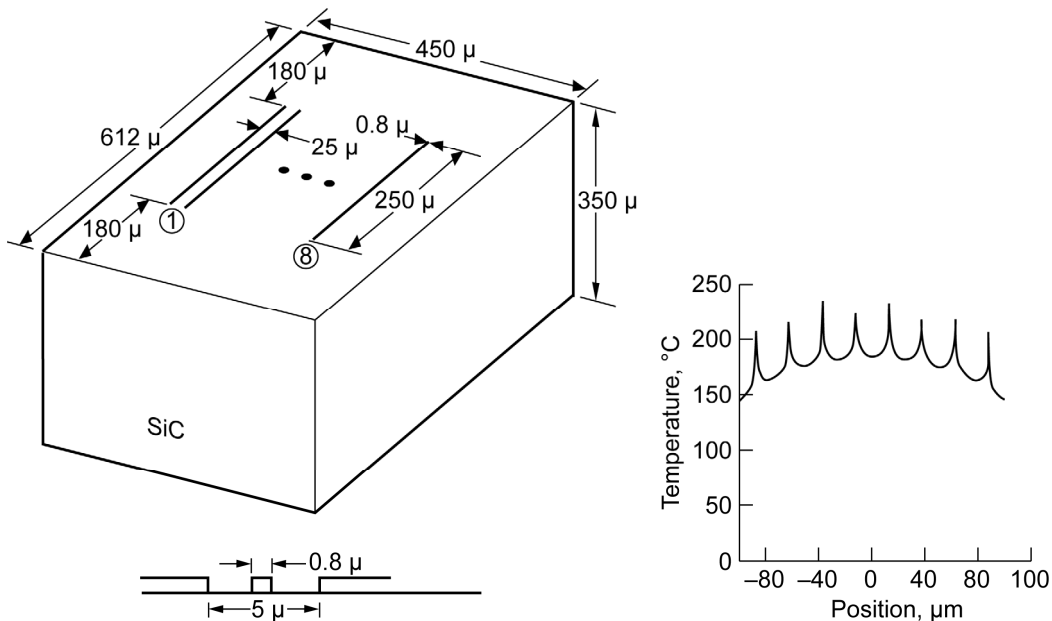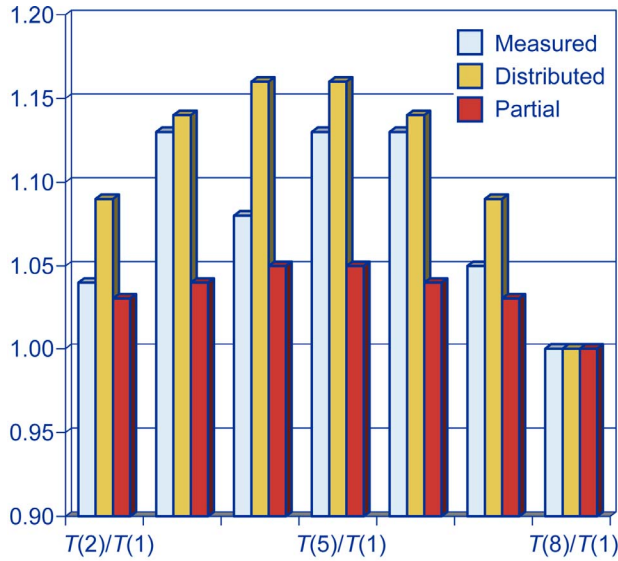of the temperatures on gates 5 and 1.

Inspection of the first column shows that a nearly symmetrical pattern exists, and some discrepancy exists for gate 4 (it is too low). Comparison of all three columns shows that the distributed approach gives a stronger variation, but the scatter in the data tends to make the results fall between the distributed and partial inductance approaches. Thus either approach will predict the actual ratio to within 1 to 10 percent.

Recall the prescription given in section IV for multiple fingers assumes the R_{11} matrix element is known, and it is assumed to be the thermal resistance of a single gate on the given substrate. The remaining elements are then determined from scaling by the factors of the mutual inductances between the gates. Therefore, to have any chance at good correlation, the value of R_{11} must be accurate. We arrive at R_{11} in the following manner. First we use the results from the simulation. At 20 V the simulation found the drain current to be 91 mA, so the dissipated power was 1.82 W. Table 19 provides a summary of the temperatures determined for a single stripe on SiC.

TABLE 19.—TEMPERATURES AT THE INTERFACES FOR THE CASE OF
A SINGLE STRIPE ON SiC. THE DISSIPATED POWER WAS 1.82 W

Location	Base	SiC, top	AlN	GaN, top	AlGaN
T, °C	32	123	126	148	148.5
T, K	305	396	399	421	421.5

The actual temperature on the top surface of the SiC is 123 °C. The corresponding linearized temperature θ=96 °C. In the simulation we used $\kappa(T) = 5.2(300/T)^{2.4}$. Thus the thermal resistance, $R_{th} = (96 - 32)/1.82 = 35.2$ K/W. The gate length is 1 μm, and if we use the footprint that results from assuming 45° spreading in the GaN, we have the value 3.4 μm for the source on the top surface of the SiC. Table 20 displays the thermal resistances versus the gate length $2l_x$.

TABLE 20.—THE CHANGE IN THERMAL RESISTANCE WITH
GATE LENGTH FOR A SINGLE STRIPE ON SiC

$2l_x$, μm	3.8	3.4	3.2	0.5	0.25	0.125
R_{th}, K/W	18.8	19.3	19.6	28.5	31.9	35.3

Notice that the last entry gives the value determined from the simulation. Similarly, the actual temperature on the GaN is 148 °C, with corresponding linearized value being $\theta = 147$ °C. The assumed

variation of kappa was $\kappa(T)=1.6(300/T)^{1.4}$. Then $R_{th} = (147 - 123)/1.82 = 13.2$ K/W. By sweeping $2l_x$ we obtain $R_{th} = 13.6$ at $2l_x = 3$ μm. This is exactly the gate-drain separation.

From the above calculations we may draw the following conclusions. The best way to determine R_{11} is to use the temperatures found from the simulation; thereby eliminating the step of attempting to estimate the size of the effective heat source. The procedure is to start with the temperatures developed by simulation, then use the Kirchhoff transform to find the corresponding linearized temperatures. Also from the simulations one may determine the heat flux into the sink by using the equations and method outlined in the companion memo. Then calculate R_{11} from its definition; change in linearized temperature divided by heat flux. The tables above have shown that the "effective" heat source is some value between a fraction of the gate length and the source-drain separation. However, the final calculated temperature is too sensitive to the chosen value to be reliable. Once R_{11} is determined from the 2–D simulation, then the multiconductor calculation will yield very good values for gate temperatures for multi-gate devices.

XI. Discussion and Conclusions

The modeling of AlGaN/GaN HEMTs is not easy as there are many gray areas that have not been resolved at this time. Due to this situation, the present work necessarily had many arbitrary assumptions. We discuss many of the problematic points that can/should be further investigated to improve the modeling of this promising technology.

Problematic Issues

1. The AlGaN/GaN HEMT is a semiconductor device that couples properties of heterojunctions, mechanical strain, piezoelectric charge, thermal and electric fields. A simulator needs to be developed that self-consistently solves for all of the above mentioned constraints. At the present time (August 2008) none exist.

2. We observed the sensitivity of temperature with $\kappa(T)$, and this must be known accurately for all layers. Apparently the growth and processing steps significantly alter this parameter, so this must be quantified for future work. The representation for $\kappa(T)$ of SiC was expressed as the reciprocal cubic as stated in section VII. The (κ,T) pairs chosen are given on page 35; the temperatures selected were 350, 400, and 450 K. When extrapolated back to 300 K, the formula yields 5.24 W/cm-K for κ. The SiC for Kuball's devices were from Cree (the only source they mentioned), and measurements from Cree indicate κ is near 4.85 at 300 K for 4H-SiC (SI). Thus our best fit used a value (5.24) that was 8 percent high. There are several reasons for this; (a) we assumed the baseplate remained at 300 K, whereas it actually drifted up in temperature, and there is no way to allow it to drift upwards during a simulation run. Thus to get correlation with their measured points, we had to use a slightly higher value for κ. (b) The device had some heat escaping from the sides and metal pads on the top; these heat paths will lower the gate temperatures from those under the assumption that all heat must leave via the baseplate. (c) We could have chosen the 300 K value for κ in the curve-fitting, rather than allowing the extrapolation back to 300 K to perhaps appear out of bounds. In the literature one often finds 3.3 to 3.5 as values for κ, but that is for partially conducting material (6H-SiC) where the doping is near 1.0×10^{17} cm^{-3}, not SI (semi-insulating). (d) Part of the 8 percent is due to the 2–D and 3–D effective differences. Therefore we are comfortable with the curve-fit chosen.

3. The papers by Kuball's group are the only ones in the open literature with enough data to permit validation of modeling with experiments; more are needed. We could not make an unambiguous comparison as the baseplate temperature was not fixed. We chose to keep the gate in the middle of our simulation space, although the experimental gate was not centered. We assumed this difference to be inconsequential.

4. A significant problem is the source of the carriers in the notch of the conduction band. At the present time there are several theories that address this issue, but none have been justified. Without

knowing the true fixed charge density, Poisson's equation cannot be solved; which is the heart of the semiconductor simulator. We used a supply layer in the AlGaN layer, and the mobile charges inserted along with the sheet charge placed at the heterojunction. ATLAS automatically inserts them to keep charge neutrality. Many practical devices are unintentionally doped (UID), so the source of the carriers is unknown. The source for (some of the) carriers has been speculated to be donors on the upper surface of the AlGaN. Most (if not all) devices require a passivation layer on the top surface, which chemically interacts with the donors (neutralizes them?).

5. The device has many traps, and they are apparently distributed in all layers and interfaces. The interplay between traps, surface donors, and free carriers in the 2DEG channel cause considerable variation while in operation. The phenomena of current collapse, rf slump, knee walk-out, and other non-ideal effects are assumed to be related to the traps, unknown donors, and other effects. Current collapse is assumed to be due to traps in the GaN, whereas rf slump is due to surface traps.

6. We used a very simple model for the 2DEG channel; just a layer of GaN with appropriate mobility. We performed a calculation using the Poisson-Schroedinger solver, and determined the I–V curve for 0 V on the gate. The curve was close to what we obtained using the simple model, so it is justified.

7. The density of carriers in the notch, n_s, apparently change with many design parameters. The interaction is complex as gate length changes (all other parameters held constant) strongly alter the saturation drain current (experimental finding). Since the source-drain separation is constant, apparently the amount of exposed surface area between them affects the current. One speculates this may be due to the change in the number of donors or traps (not covered, and hence neutralized by gate metal) with change in available AlGaN surface area. To account for this and other effects (for example the change in strain with applied voltage and the corresponding change in polarization charge density, and thus change in 2DEG charge density), the following prescription could be used. Write the 2DEG carrier density as (see refs. 80 and 81) $n_s = f(V_{gs},T)$, where to first order, n_s varies linearly with V_{gs}. Since the simulator charge sheet has a strong affect on the 2DEG density, one has the freedom to vary it to change n_s for different gate voltages. This could act along with changes in the supply layer to generate the appropriate 2DEG density. This would enable better correlation with SiC than we were able to achieve. The device on the sapphire substrate was larger and hotter than that on SiC, and the same value for σ_s, was sufficient for all gate values. However, the SiC device, being smaller, was more sensitive to gate voltage. Another possible option could be the fact that the sapphire unit, being hotter, had most, if not all traps emptied; whereas the cooler SiC had traps remaining, which caused some of the droop. By adjusting the sheet density, we are indirectly taking into account the reduction in channel current due to charge now held in traps. However, we are not directly including this trapped charge in Poisson's equation.

8. Many semiconductor properties were not included; presence of holes (some simulations in the literature, due to their arbitrary assumptions, predict a substantial number), no tunneling between 2–D and 3–D (normal) electrons in and out of the well, and no traps. The presence of traps on the surface may pin the Fermi level; this was not considered. Also some of the droop in the I–V could be due to trapping. No hot electrons were included since the D-D model was used. However, some experts in the field think hot electrons don't exist in the devices. This is based on experimental data.

9. Basically we tweaked about 14 basic material parameters to achieve satisfactory agreement with the simulator and measurements. This is needed, as many of them are uncertain by up to 30 percent, as well as the shortfalls of the program; i.e., no strain, thus the piezoelectric effects are masked in just a uniform sheet charge, and a 2–D, not a 3–D self-consistent solver. The supply layer in the AlGaN serves a critical need in a simulation. In actual devices the carriers that populate the channel may come from either a supply layer or unintentional dopants in the AlGaN layer. In either case, dopants must be present. Three publications (refs. 73 to 75) have argued that the electrons in the channel cannot come from the bulk, and therefore must come from intentional or unintentional dopants in the AlGaN. The dopant density is a dominant parameter, as it serves to adequately supply the notch with sufficient carriers. Relatively small changes in the supply layer density produce enough carriers to cause the I–V curves to rise steeply. In the UID devices reported, there has been speculation that the dopants are on the upper surface of the AlGaN. Then the details of the passivation layer become important; as it may restrict the dopant density and thus

the available drain current. The passivation layers stabilize the drain current with time and temperature; and we speculate that the mechanism is essentially the changing of the dopant density activation level. The number of available carriers adjusts the shape and depth of the notch in the conduction band edge, and therefore the I–V curves significantly. In one simulation, a negative sheet charge was placed on the top AlGaN surface, and the drain current was reduced by 40 percent of that without the sheet. The sheet was assumed to model the negative spontaneous polarization charge layer that must exist at the surface. However, apparently in actual devices this charge is neutralized with positive charge, due to dopants or other unknown sources. The interaction of the surface/passivation layer interface and the channel parameters is a topic for future investigation with ATLAS.

Since experiments have shown that irreparable damage occurs when the channel approaches about 230 °C (or 600 °C, depending on reference), our model can be used to determine the maximum DC power that can be dissipated safely for various designs. Also the singularities about the gate edge can be studied for both excess temperature and field (to eliminate the possibility of avalanche) simultaneously. Then the maximum drain voltage (and hence maximum RF power theoretically obtainable) may be estimated. We attempted to use the Barnes model (a choice for negative differential mobility) in the SiC cases, as we had difficulty reproducing the large experimental droop. We did not get satisfactory results; perhaps instability problems were occurring (a warning of such was stated in the users' manual).

Figure 94 gives the entire energy band (from gate to heatsink) for both substrates. The values of energy in eV at selected points are referenced to the Fermi level. The slope in the SiC region is due to the Schottky barrier height being applied to the bottom of the SiC (since in contact with a metal), as SiC is recognized as a semiconductor in ATLAS. This contact potential should not alter our results; however its effects may be seen in some plots, wherein the potentials in the drain area are a few volts above 20 V, even though the drain is biased to 20 V. The sapphire is treated as a dielectric and thus has no contact potential.
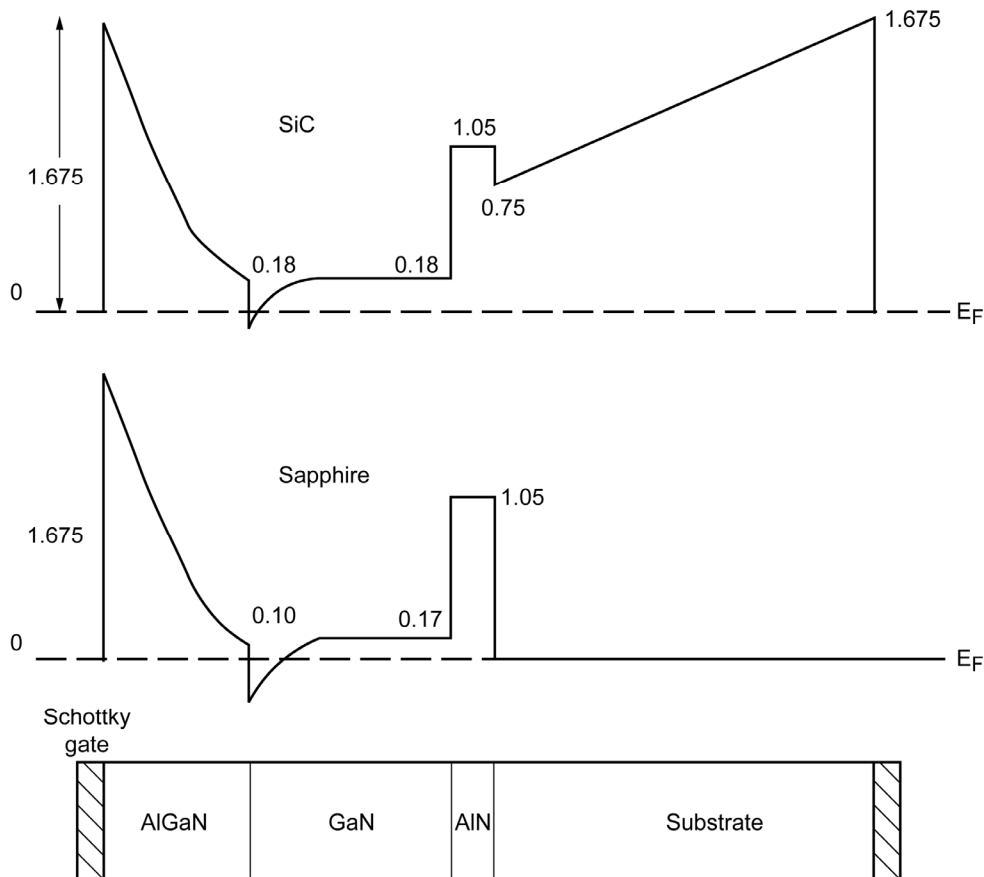

Figure 94.—Energy band profile through entire device for SiC and sapphire substrates.

The conduction band edge shape in the vicinity of the heterojunction is one of the major components that determine the characteristics of a HEMT. The step height and shape of the notch determines many of the 2DEG properties. The step is due to the difference in bandgaps in the materials on either side of the junction. The change in lattice parameter is the fundamental cause for the difference. At the material interface the two space lattices must transition over a short distance, and the details of the transition are not well known. The following calculation determines the effective dipole needed to model the step *if the step were due to classical static charge layers*. From (ref. 76) we showed the step, or more accurately, the linear drop across two infinite sheet charges that form a dipole to be

$$\Delta\phi = \sigma\, d/\varepsilon$$

Where σ is the magnitude of the sheet charge density on one sheet, d is the separation between them, and ε is the dielectric constant. For our case, the step is 0.45 V, $\varepsilon = 9.5\ \varepsilon_o$, and $d = 1.92\times10^{-8}$ cm, which yields $\sigma = 1.23\times10^{14}$ electrons/cm^2. The separation was approximately the distance between three mesh points. Observe that this is about two orders of magnitude larger than the sheet charge used at the heterojunction to model the piezoelectric fields. The step, being of quantum mechanical origin, apparently has no effective charge associated with it, so only the real positive sheet charge and the mobile carriers in the notch create electric fields in the region of the heterojunction. Thus our model implies a "clean" heterojunction with no free or bound charge due to the lattice change. The only bound charge is that which creates the piezoelectric field, and it exists in all regions in the vicinity of the heterojunction where the crystal is strained. We have shown that this distributed effect may be adequately modeled with a single sheet charge at the heterojunction. The electric potential field associated with the bound charges due to strain, along with other terms mentioned in (ref. 76) constitute the "other" terms that constitute the conduction band edge energy profile.

Figures 95 through 99 display the device current at several vertical planes. The vertical cutlines are at the center of the S-G access region, the gate edge, and the center of the G-D access region. The total, channel, AlGaN and bulk layer currents are displayed. The supply layer doping value is 2×10^{18} cm^{-3}.

Figures 100 through 103 are similar plots, but now the doping is 3×10^{18} cm^{-3}, and the gate is at –2 for all cases.
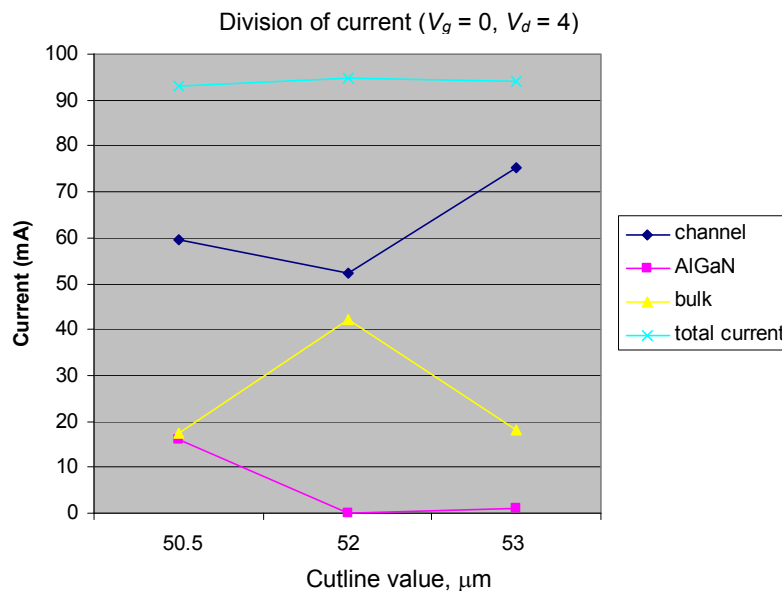
Figure 95.—The division of current at three vertical cutlines. Observe the total value should be absolutely flat, but the small variation is due to deviations in the numerical integration of the current density due to non-uniform mesh densities.
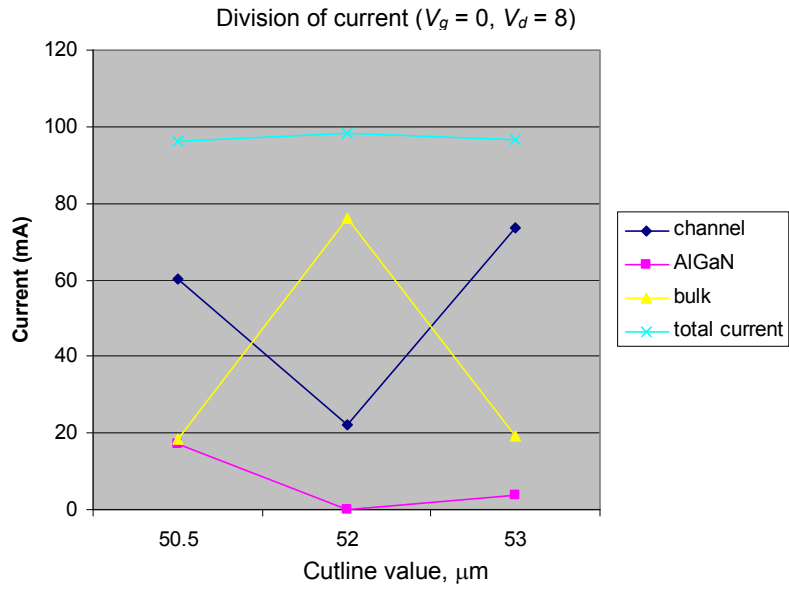
Figure 96.—Current division at 8 V.
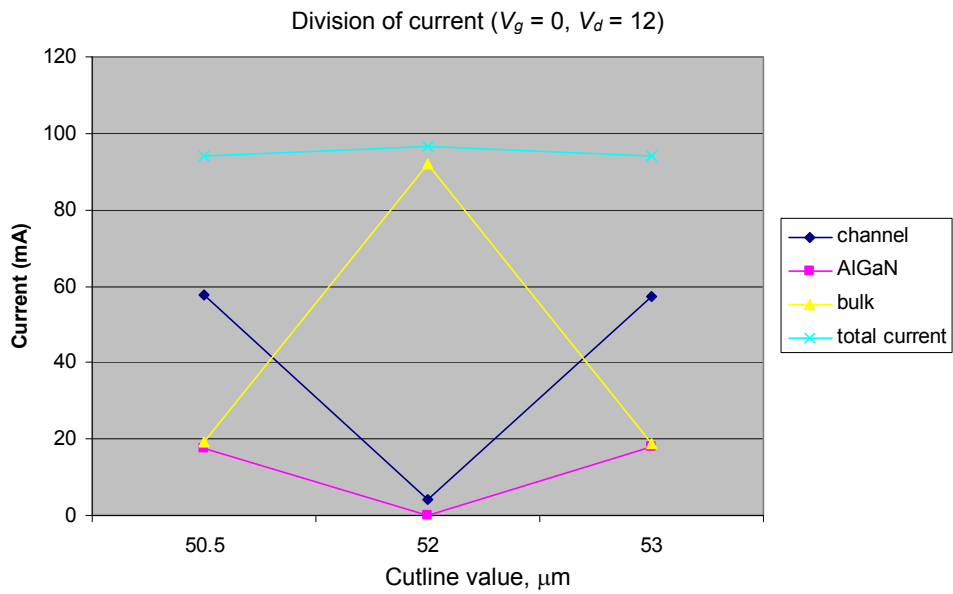
Figure 97.—Division of current at 12 V.
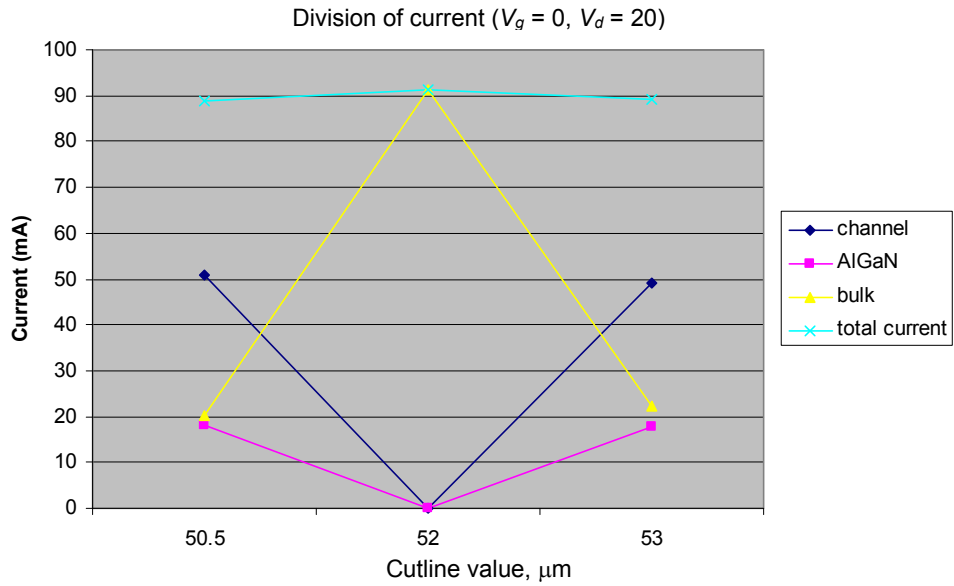
Figure 98.—Division of current at 20 V.
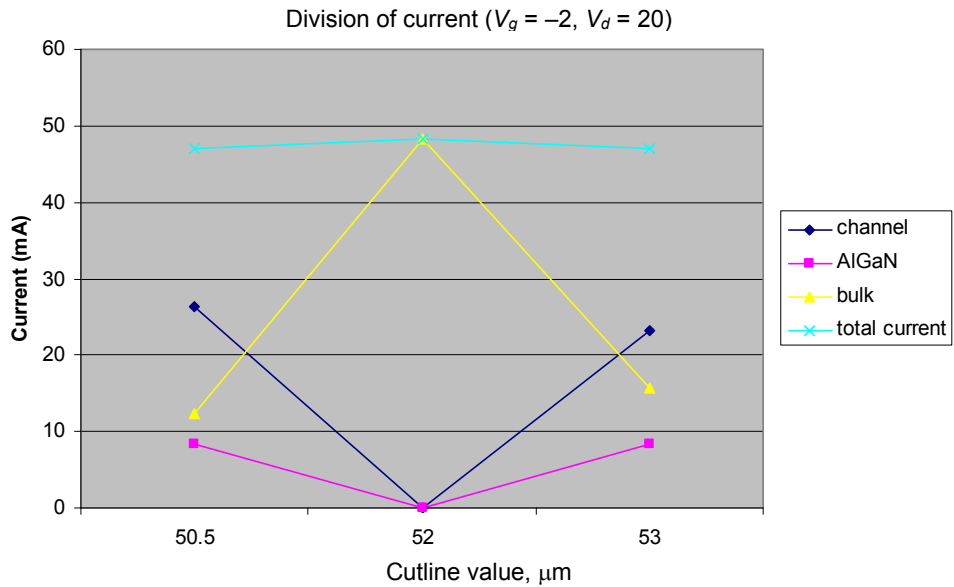
Figure 99.—Division of current for $V_g = -2$ V and $V_d = 20$ V. Notice all of the current is in the bulk at the gate edge (52 μm).
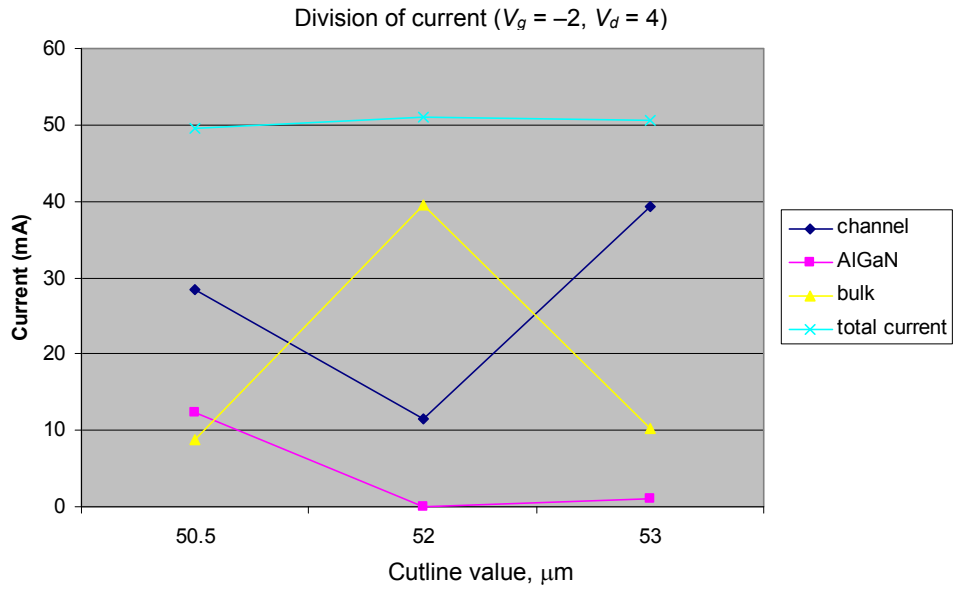
Figure 100.—Division of current for $N_d = 3 \times 10^{18}$ and gate at -2 V.
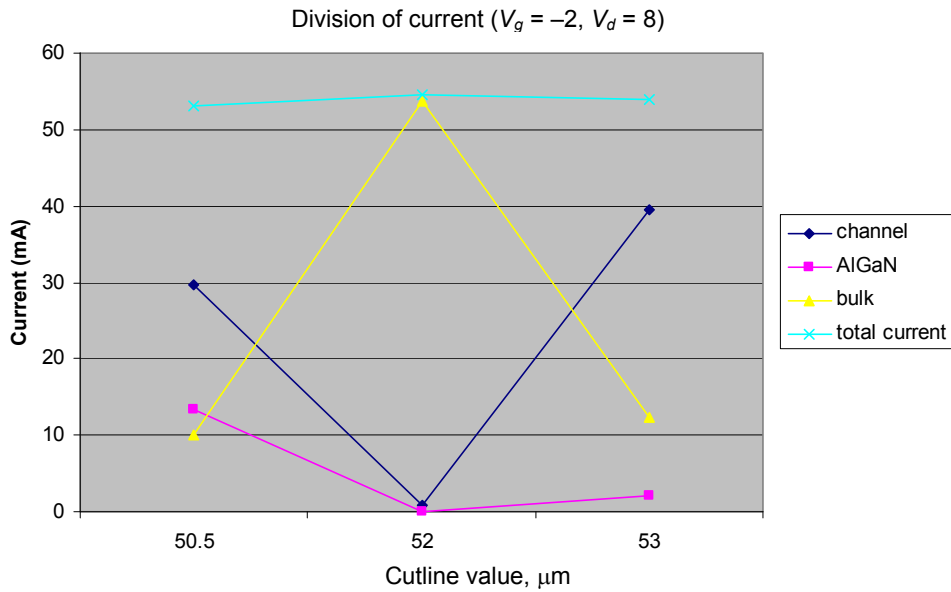
Figure 101.—Division for drain at 8 V. Notice as the drain increases, the channel becomes depleted at the gate edge.
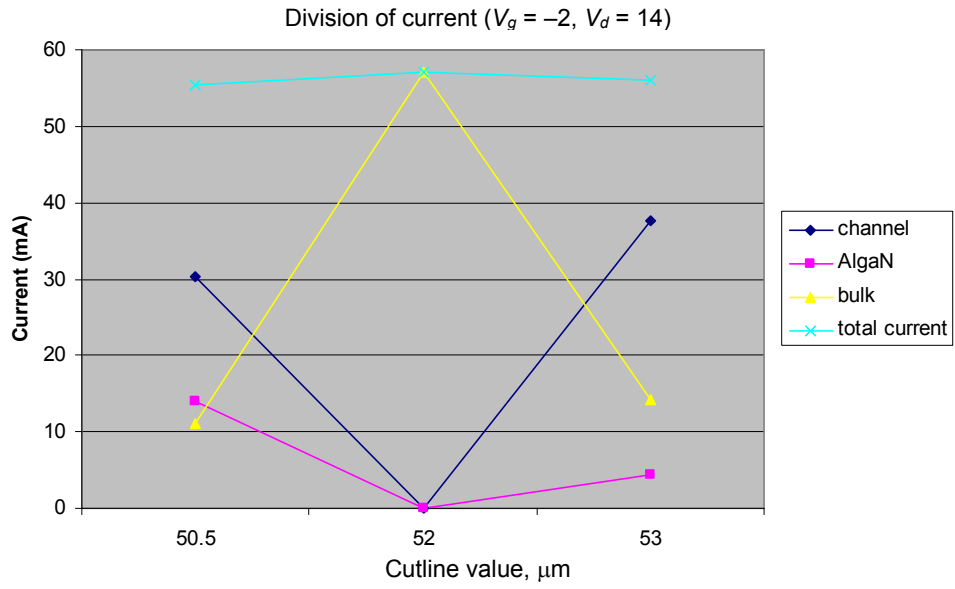
Figure 102.—Similar division at 12 V.
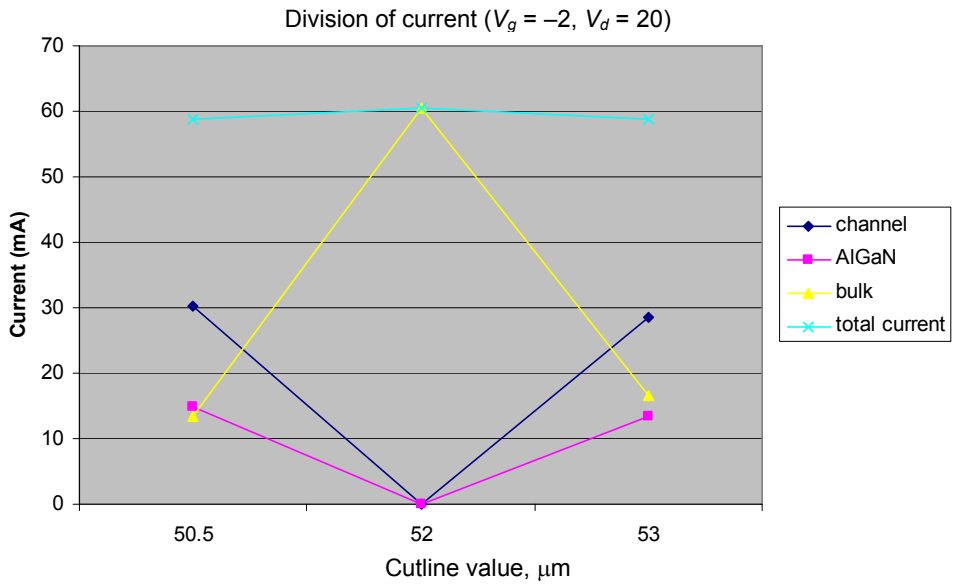
Figure 103.—Current division for SiC device at bias point (–2,20). The channel is completely empty of carriers at the gate edge.

The above sequence of plots shows that the 2DEG channel is devoid of carriers over a small region beyond the gate in the saturation region. Thus the conductivities of the bulk GaN and AlGaN layers are important in device design.

We have used Masana's equation set as the basis of our analytical efforts, since it appeared to be the most flexible. However, by referring to figure 104 we observe the large variation of thermal resistance with the "effective gate length $2l_x$", for most of the closed-form expressions published in the literature. The legend contains the works by Meeks (ref. 77), Cooke (ref. 78), and Fukui (ref. 79), along with others that we have already discussed. While all show a decrease in R_{th} with increasing $2l_x$, the spread is too large if one is attempting to develop accurate results. For a 0.5 µm gate (heat source) we observe a spread of about 3:1 from Royet's to Darwish's equations. Notice also, that Darwish's results are not applicable for heat sources greater than 1.5 µm. With this new insight, we decided that our first attempts to find "effective" gate values, as presented in section V, with many reservations, was not the best way to proceed.

We have concluded that one must abandon the "effective gate length $2l_x$" approach, and determine instead, R_{th} directly from the simulations. That is we determine R_{th} from its definition; change in temperature between the planes of interest, divided by the power dissipation. We found this to be necessary, as the heat generation region is not adequately modeled by a uniform heat source strip with the dimensions equal to the actual gate, or some constant times the gate length, or some value near the source-drain spacing. The simulations show that there are in general 4 spikes in the heat generation function; which are located at the metallization edges. Their relative intensities change with bias point, which makes determining an effective length for all reasonable bias points nearly impossible. In addition there is the distributed portion that also changes with current path through the device. The details of the determination of R_{th} via the simulation will be presented in another memorandum. Also presented there in the appendix is the determination of the heat flux $\dot{q}$ between the ends of a 1–D flow regime with known temperatures at either end, and the thermal conductivity described by an easily integratable function of temperature. This is necessary, as $\dot{q}$ is not immediately available from ATLAS. We found that $\dot{q}$ may be only about 60 percent (with a sapphire substrate) of the I–V product of the bias point. This gives an
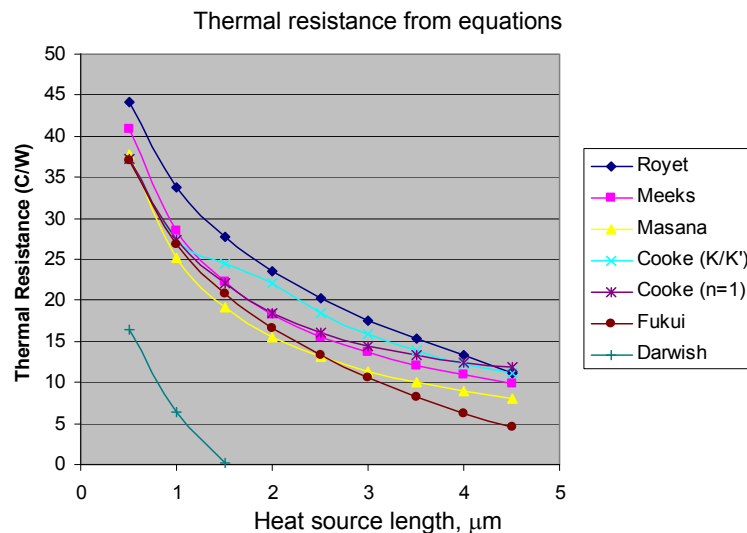

Figure 104.—The thermal resistance versus the effective gate length $2l_x$, for seven of the basic references that calculate it in closed-form equations. This chart should be nearly exhaustive, as the literature was probed to great depth.

indication of the amount of heat that leaves via the sides, and metal pads on the surface. Notice also that both components in equation (1) R_{th} and P_{diss}, (where it is assumed that $P_{diss} = \dot{q}$), are not accurately found from formulas or the I–V product of the bias point! This is a significant result obtained in this study.

Accurate temperature predictions are critical, as lifetime estimates can change by large values as the temperature changes by 10°. While we were able to get agreement, there are areas that leave the door open for speculation. First of all the actual devices had 3–D heat spreading as opposed to the 2–D simulation. For example, the top surface of the device had dimensions 297×179 μm^2. The 200 μm wide gate was 70 μm from the edge. However, in the simulations, the areas were 120×200 (sapphire) and 114×200 (SiC) μm^2, and the gate was symmetrically located in the center. This was due to the upper limit of mesh points available in ATLAS. In the simulation the heat can only flow perpendicular to the long dimension of the gate electrode, and not "along" the gate. The short sides of the simulations were dictated by the number of available mesh points and the maximum separation between them needed for accuracy. Thus the ratios of the true surface area to the simulation areas were 2.2 (sapphire) and 2.3 (SiC). Thus the actual devices had more area upon which to dissipate heat. Thus we realize our values for κ are too large; however, once the *effective value* is determined (to compensate for the discrepancy in areas and the lack of spreading along the gate width), then the simulations tracked the measured values very well. The anticipated future work includes the following tasks. The incorporation of traps will be the next major hurdle in the simulation effort. The behavior with traps is a complex and not well understood phenomenon. The effects of trapped charge alter both the DC and rf characteristics in complex ways. We have studied and summarized the literature concerning physical locations, excitation levels, surface and bulk densities, and fill-empty times for all traps that have been measured. Once the trap incorporation is completed, we will be able to accurately determine the benefits, drawbacks, etc. of alternate gate shapes, single or double recess gate designs, fieldplates, and passivation layers. Another exercise is to compare results of ATLAS 2–D (with just the thermal simulator) and ANSYS 3–D to quantify the differences in temperature. One can use both uniform stripes as well as the more realistic four spikes and a smooth portion of $g(x,y)$. Favorable agreement could resolve the magnitude of the error in the 2–D case.

XII. Summary

This memo has described the development of a baseline model for simulation of AlGaN/GaN HEMTs with the ATLAS package from Silvaco, Inc. We have sought to understand the basic physical principles underlying the device, and apply the available tools in ATLAS to allow reasonable simulation. We used the enhanced drift-diffusion model, as experiments have indicated that hot electrons are not plentiful in the devices, and the hydro-dynamic model is not necessary. A single sheet charge at the heterojunction is sufficient to model most of the stress/strain, and perhaps trap effects. The channel supporting the 2DEG was modeled with a uniform slice of GaN with appropriate mobility parameters. A supply layer is needed in the buffer to guarantee sufficient carriers in the device. Apparently the carriers in the 2DEG channel are insufficient to carry all of the measured drain current, (this fact has been stated in the literature). We have demonstrated many of the sensitivities between various parameters in the system. The I–V and thermal characteristics of single gate devices on sapphire and SiC substrates were developed. The self-heating included the dependence of the thermal conductivities of all materials. The 2–D simulations for single finger devices agree very well with published data in both the I–V characteristics and channel temperatures. Therefore we think the basic model and parameter set is adequate for predicting I–V and temperature values in all part of the transistor as device parameters and geometry are changed.

We have presented and used data from published measurements, simulations, and theoretical studies, to develop the channel temperature estimation procedure. We strove for self-consistency, as the dispersion in parameter values is very large. This dispersion is to be expected due to the various growth methods, processes, and other procedures. Our simulations have shown that the current in the channel is the dominant portion in the linear regime of the I–V curve, and then in saturation, the channel is severed

by the large field at the gate edge, and the current is then carried in the bulk GaN and AlGaN. We assume the step height in the conduction band at the heterojunction includes any variations due to dipoles, excess charges, etc. While the details of the notch in the band edge are important, the contact resistivity for the source and drain contacts, and the doping in the AlGaN supply layer are also very critical parameters. For our software version, we were at the limit of the number of mesh points; which necessitated the simulation of just a single gate device. Since the simulator was restricted to 2–D calculations, the analytical portions that include 3–D effects was needed to complete the study. We have determined that the major difficulty in matching analytical predictions with measurements resides in choosing the appropriate size of the heat source in the established closed form equations found in the literature. The effective gate length must adjust as the heat generation $g(x,y,z)$ changes with bias. The change in thermal conductivity with temperature must be included in any simulation or analytical calculation or significant error will result. The channel temperatures are dominated by the substrate, since the GaN region is very thin compared to the substrates.

The electric fields and electron velocities were very large at the contacts; with the source being the larger. The fields were up to 7 MV/cm, which are slightly above the accepted avalanche values of 3 to 4 MV/cm. The carrier velocities were as high as 4×10^7 cm/sec, even with the designated saturation velocity set at 2×10^7 cm/sec. These minor effects were assumed unimportant, and did not detract from the overall favorable outcomes. We found the channel carries about ½ of the total drain current; with the remainder nearly split between the AlGaN and bulk regions. In a small region about the gate edge on the drain side, the channel is broken for voltages above 12 V. It recovers at somewhere between the gate edge and the middle of the G-D access region. We have demonstrated that the analogy between the heat conduction and Poisson's equation may be used for developing the thermal resistance matrix. The effects of finite width gates can be incorporated using the partial inductances between the gates. It was demonstrated that the partial inductance procedure gives a less severe change in temperature between gates; which seems physically correct, as heat is allowed to escape along the gates, which should bring them all to lower as well as closer temperatures.

The major predictive nature of is work is as follows. Suppose one wants to construct a multi-finger power device. First construct a single finger device and measure the I–V curves. Use the simulator to duplicate those curves. Once this step is completed, the temperatures at different regions in the device are known. Determine the thermal resistance for the single finger from the results of the simulation; temperature change divided by the heat flux. Then R_{11} is known, and the remaining analytical steps have been discussed herein. Then the temperature on each finger of the predicted array is calculated. This enables design changes with minimal effort, and circumvents the very difficult task of accurately measuring the temperature. The accuracy of the technique should be within 5 to 7 percent.

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14. ABSTRACT
Numerical simulation results (with emphasis on channel temperature) for a single gate AlGaN/GaN High Electron Mobility Transistor (HEMT) with either a sapphire or SiC substrate are presented. The static I-V characteristics, with concomitant channel temperatures (T_{ch}) are calculated using the software package ATLAS, from Silvaco, Inc. An in-depth study of analytical (and previous numerical) methods for the determination of T_{ch} in both single and multiple gate devices is also included. We develop a method for calculating T_{ch} for the single gate device with the temperature dependence of the thermal conductivity of all material layers included. We also present a new method for determining the temperature on each gate in a multi-gate array. These models are compared with experimental results, and show good agreement. We demonstrate that one may obtain the channel temperature within an accuracy of ±10 °C in some cases. Comparisons between different approaches are given to show the limits, sensitivities, and needed approximations, for reasonable agreement with measurements.

15. SUBJECT TERMS
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