

This Biasable Subharmonic Mixer for the RF range of 520 to 600 GHz consists of a monolithic integrated circuit on a GaAs membrane held in a precision-machined waveguide block.

- The short wavelengths in the intended operating-frequency range translate to stringent requirements for precision of fabrication and assembly of the circuits; these requirements are even more stringent for wide-bandwidth circuits. This consideration is addressed in two ways: (1) As much as possible of the mixer circuitry is fabricated in the form of a monolithic integrated circuit on a GaAs membrane, employing a modified version of a process used previously to fabricate a non-subharmonic mixer for a frequency of 2.5 THz and frequency multipliers for frequencies up to 2 THz. (2) The remainder of the

circuitry is precision machined into a waveguide block that holds the GaAs integrated circuit.

- Generation of a local-oscillator (LO) signal having sufficient power to pump a mixer requires more DC power as the LO frequency increases; this is because the only wide-band LO sources available in this frequency range are Schottky-diode frequency multipliers, and their efficiencies decrease with frequency. This consideration is addressed in two ways: (1) Unlike the prior 2.5-THz GaAs-membrane mixer, this mixer is subharmonically driven, meaning that the LO operates at half the frequency of the incoming signal to be measured [denoted the radio frequency (RF) in traditional frequency mixer parlance]. (2) The diodes are arranged so that they can be biased to operate closer to their switching voltage so that less LO power is needed to switch the diodes between the conducting and nonconducting states. This switching is what makes the diodes act as a frequency mixer.

The Schottky diodes are fabricated in an antiparallel configuration, using beam leads, such that one electrode of each diode is grounded. One diode is AC grounded through a capacitor to allow the diodes to be biased. A simple probe picks up the LO signal from a

waveguide shown on the left side of the figure. The LO signal bypasses an RF filter comprised of two vertical stubs and is coupled into the mixer diodes. Similarly, another probe picks up the RF signal from a waveguide shown on the right side of the figure and the RF signal flows leftward to the diodes.

The on-chip circuitry also conveys the lower-frequency mixer output signal [also denoted, variously, as the intermediate-frequency (IF) signal or the down-converted version of the RF signal in traditional frequency-mixer parlance] to an off-chip circuit board on the right side. The stub filter to the left of the diodes prevents the leakage of the RF signal past the diodes to the LO waveguide. Leakage of the LO signal into the RF waveguide is inherently blocked as it is below the cutoff frequency of the RF waveguide. There is also a filter in the output channel, implemented as shunt capacitors (not shown here), to prevent leakage of RF and LO signals to the off-chip circuitry that processes the IF signal.

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## Hardware Implementation of Serially Concatenated PPM Decoder

Error-rate performance approaches channel capacity.

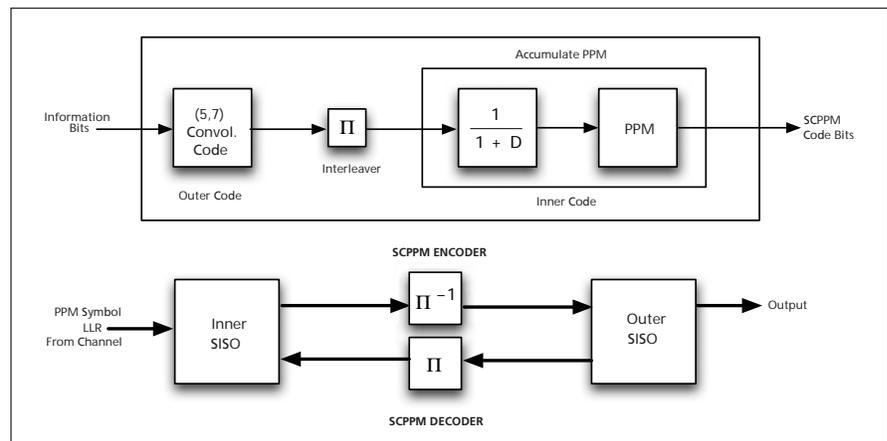
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A prototype decoder for a serially concatenated pulse position modulation (SCPPM) code has been implemented in a field-programmable gate array (FPGA). At the time of this reporting, this is the first known hardware SCPPM decoder. The SCPPM coding scheme, conceived for free-space optical communications with both deep-space and terrestrial applications in mind, is an improvement of several dB over the conventional Reed-Solomon PPM scheme. The design of the FPGA SCPPM decoder is based on a turbo decoding algorithm that requires relatively low computational complexity while delivering error-rate performance within approximately 1 dB of channel capacity.

The SCPPM encoder consists of an outer convolutional encoder, an interleaver, an accumulator, and an inner

modulation encoder (more precisely, a mapping of bits to PPM symbols). Each code is describable by a trellis (a finite di-

rected graph). The SCPPM decoder consists of an inner soft-in-soft-out (SISO) module, a de-interleaver, an outer SISO



The SCPPM Decoder is designed according to a decoding algorithm that includes interleaving and de-interleaving algorithms in conjunction with SISO subalgorithms for decoding inner and outer codes.

module, and an interleaver connected in a loop (see figure). Each SISO module applies the Bahl-Cocke-Jelinek-Raviv (BCJR) algorithm to compute *a-posteriori* bit log-likelihood ratios (LLRs) from *a-priori* LLRs by traversing the code trellis in forward and backward directions. The SISO modules iteratively refine the LLRs by passing the estimates between one another much like the working of a turbine engine. Extrinsic information (the difference between the *a-posteriori* and *a-priori* LLRs) is exchanged rather than the *a-posteriori* LLRs to minimize undesired feedback. All computations are performed in the logarithmic domain, wherein multiplications are translated into additions, thereby reducing complexity and sensitivity to fixed-point implementation round-off errors.

To lower the required memory for storing channel likelihood data and the amounts of data transfer between the decoder and the receiver, one can discard the majority of channel likelihoods, using only the remainder in operation of the decoder. This is accomplished in the receiver by transmitting only a subset consisting of the likelihoods that correspond to time slots containing the largest numbers of observed photons during each PPM symbol period. The assumed number of observed photons in the remaining time slots is set to the mean of a noise slot. In low background noise, the selection of a small subset in this manner results in only negligible loss.

Other features of the decoder design to reduce complexity and increase speed

include (1) quantization of metrics in an efficient procedure chosen to incur no more than a small performance loss and (2) the use of the max-star function that allows sum of exponentials to be computed by simple operations that involve only an addition, a subtraction, and a table lookup. Another prominent feature of the design is a provision for access to interleaver and de-interleaver memory in a single clock cycle, eliminating the multiple clock-cycle latency characteristic of prior interleaver and de-interleaver designs.

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