



Alternative Packaging for Back-Illuminated Imagers

Electrical contacts are made accessible from the back side.

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An alternative scheme has been conceived for packaging of silicon-based back-illuminated, back-side-thinned complementary metal oxide/semiconductor (CMOS) and charge-coupled-device image-detector integrated circuits, including an associated fabrication process. This scheme and process are complementary to those described in "Making a Back-Illuminated Imager With Back-Side Connections" (NPO-42839), *NASA Tech Briefs*, Vol. 32, No. 7 (July 2008), page 38.

To avoid misunderstanding, it should be noted that in the terminology of imaging integrated circuits, "front side" or "back side" does not necessarily refer to the side that, during operation, faces toward or away from a source of light or other object to be imaged. Instead, "front

side" signifies that side of a semiconductor substrate upon which the pixel pattern and the associated semiconductor devices and metal conductor lines are initially formed during fabrication, and "back side" signifies the opposite side. If the imager is of the type called "back-illuminated," then the back side is the one that faces an object to be imaged.

Initially, a back-illuminated, back-side-thinned image-detector is fabricated with its back side bonded to a silicon handle wafer. At a subsequent stage of fabrication, the front side is bonded to a glass wafer (for mechanical support) and the silicon handle wafer is etched away to expose the back side. The front-side integrated circuitry includes metal input/output contact pads, which are

rendered inaccessible by the bonding of the front side to the glass wafer. Hence, one of the main problems is to make the input/output contact pads accessible from the back side, which is ultimately to be the side accessible to the external world. The present combination of an alternative packaging scheme and associated fabrication process constitute a solution of the problem.

The divergence between the alternative packaging scheme and fabrication process and prior such schemes and processes begins at the stage at which the integrated circuitry has been fabricated on the front side and the handle substrate is still attached. First, an outer oxide layer on the front side as fabricated thus far is planarized, then bonded to the glass wafer, as shown in the upper part of the figure. The remainder of the process can be summarized as follows. Through multiple steps of patterning, etching, and deposition, holes are formed in the silicon integrated-circuit substrate from the back side to expose metal traces and thereby form back-side contact pads. An ancillary benefit of the selective etching to expose the metal traces is that it cleans the exposed back surfaces of the traces, thereby making it possible to achieve low-resistance contact. Additional contact pads for electrical biasing of the silicon device substrate are also formed on the back side. The lower part of the figure depicts the finished product.

This work was done by Bedabrata Pain of Caltech for NASA's Jet Propulsion Laboratory.

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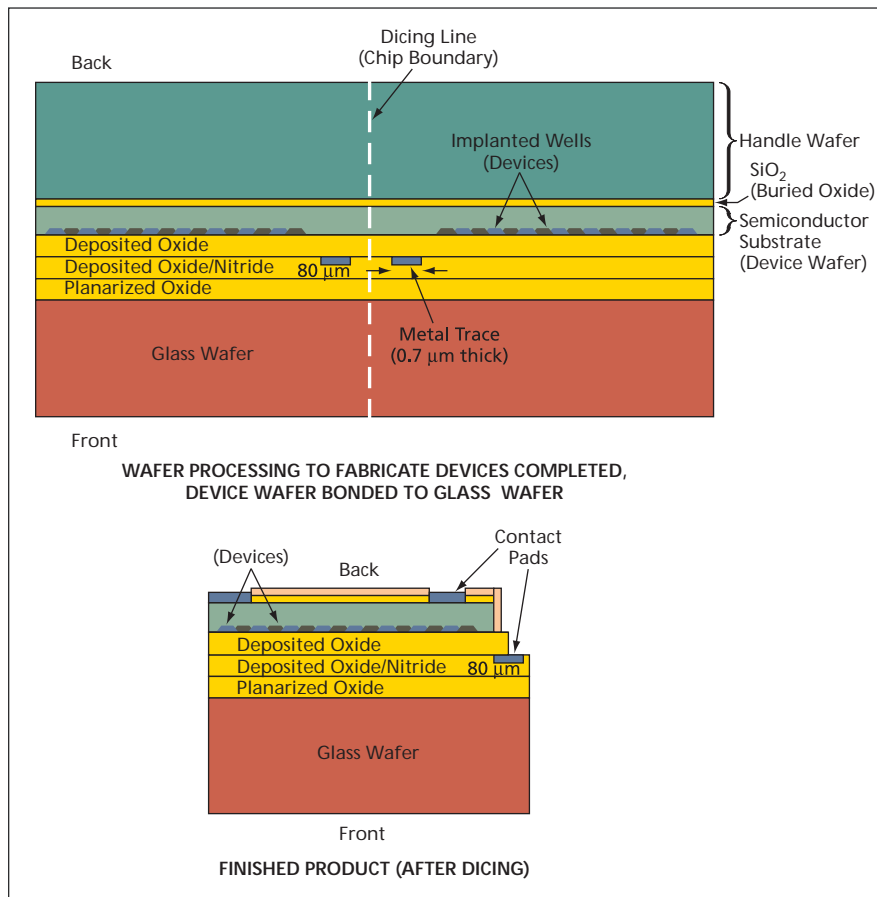
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These Simplified Cross Sections depict an intermediate stage and the final stage in the fabrication of an imager according to the alternative scheme described in the text.