charge signal as in a prior operational-amplifier-based signal chain). Hence, the charging and discharging of the bus is not slowed by the Miller effect, enabling reduction of the bias current from the value that would otherwise be needed. The elimination of the ohmic drop across the column-selecting switch reduces the output voltage offset to a minimum, eliminates nonlinearity, and makes the small-signal gain approach its ideal value of unity.

This work was done by Bedabrata Pain, Bruce Hancock, and Thomas Cunningham of Caltech for NASA's Jet Propulsion Laboratory.

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

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SOI CMOS Imager With Suppression of Cross-Talk

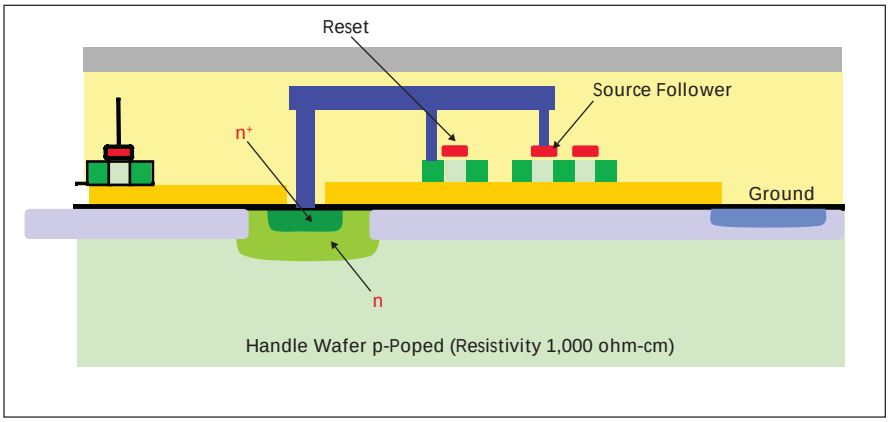
Potential applications are diverse, ranging from astronomy to medical imaging.

NASA's Jet Propulsion Laboratory, Pasadena, California

A monolithic silicon-on-insulator (SOI) complementary metal oxide/semiconductor (CMOS) image-detecting integrated circuit of the active-pixel-sensor type, now undergoing development, is designed to operate at visible and near-infrared wavelengths and to offer a combination of high quantum efficiency and low diffusion and capacitive cross-talk among pixels. The imager is designed to be especially suitable for astronomical and astrophysical applications. The imager design could also readily be adapted to general scientific, biological, medical, and spectroscopic applications.

One of the conditions needed to ensure both high quantum efficiency and low diffusion cross-talk is a relatively high reverse bias potential (between about 20 and about 50 V) on the photodiode in each pixel. Heretofore, a major obstacle to realization of this condition in a monolithic integrated circuit has been posed by the fact that the required high reverse bias on the photodiode is incompatible with metal oxide/semiconductor field-effect transistors (MOSFETs) in the CMOS pixel readout circuitry.

In the imager now being developed, the SOI structure is utilized to overcome this obstacle: The handle wafer is retained and the photodiode is formed in the handle wafer. The MOSFETs are formed on the SOI layer, which is separated from the handle wafer by a buried oxide layer. The electrical isolation provided by the buried oxide layer makes it possible to bias the MOSFETs at CMOS-compatible potentials (between 0 and 3 V), while biasing the photodiode at the required higher potential, and enables independent optimization of the sensory and readout portions of the imager.



A **Photodiode Is Formed in the Handle Wafer** between an implanted n-doped well and the rest of the handle wafer, which is p-doped. This arrangement makes it possible to apply a high reverse bias to the diode, as needed for high quantum efficiency and low diffusion cross-talk.

The figure presents a simplified and partly schematic cross section of one pixel. The photodiode is formed, in the handle wafer, between an implanted deep n-doped well and the rest of the handle wafer. An n^+-doped cathode contact region in the well is electrically connected by a tungsten via plug to the source of a reset FET residing on the SOI layer. The bottom of the handle wafer is reverse-biased to 30 V, while the n^+-doped cathode contact region is subject to potential excursions of 1 to 2 V, which are within permissible voltage limits. The reverse bias of the handle wafer is brought in from the front side (the top side in the figure) through a p^+-doped anode guard ring positioned and dimensioned to prevent breakdown of Si or SiO_2 in the presence of the bias potential. An implanted boron pinning layer, biased at a small negative potential, holds the interface between the buried oxide and the handle-wafer silicon in equilibrium and thereby helps to minimize dark current.

The potential difference ($\oplus$30 V) between the pinning layer and the bottom of the handle wafer could result in undesired ohmic conduction between them. Therefore, the doping profiles are chosen in conjunction with the device geometry (including the dimensions of, and spacing between, the n-doped wells) to shape the electric field to create a pinch-off region (a potential barrier) that prevents such conduction. The pinch-off region also prevents electric-field coupling between adjacent n-doped wells, thereby eliminating inter-pixel capacitance and the associated capacitive cross-talk between pixels.

The reset FET is, more specifically, an n-type FET, chosen to prevent inadvertent forward-biasing of the sensory node during reset-switch turn-off. The back and front gates of the reset FET are connected to each other in order to set the minimum anode potential such that the pinch-off condition is maintained for all illumination conditions.

This configuration also increases the reverse bias of the reset FET, preventing parasitic conduction in the FET channel, thereby suppressing sensory-node leakage.

This work was done by Bedabrata Pain, Xinyu Zheng, Thomas J. Cunningham, Suresh Seshadri, and Chao Sun of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

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