spatially-low-pass subband. The resulting data are converted to sign-magnitude form and compressed in a manner similar to that of a baseline hyperspectral-image-compression method. The mean values are encoded in the compressed bit stream and added back to the data at the appropriate decompression step. The overhead incurred by encoding the mean values — only a few bits per spectral band — is negligible with respect to the huge size of a typical hyperspectral data set.

The other method is denoted modified decomposition. This method is so named because it involves a modified version of a commonly used multiresolution wavelet decomposition, known in the art as the 3D Mallat decomposition, in which (a) the first of multiple stages of a 3D wavelet transform is applied to the entire dataset and (b) subsequent stages are applied only to the horizontally-, vertically-, and spectrally-low-pass subband from the preceding stage. In the modified decomposition, in stages after the first, not only is the spatially-low-pass, spectrally-low-pass subband further decomposed, but also spatially-low-pass, spectrally-high-pass subbands are further decomposed spatially.

Either method can be used alone to improve the quality of a reconstructed image (see figure). Alternatively, the two methods can be combined by first performing modified decomposition, then subtracting the mean values from spatial planes of spatially-low-pass subbands.

This work was done by Matthew Klimesh, Aaron Kiely, Hua Xie, and Nazeeh Aranki of Caltech for NASA's Jet Propulsion Laboratory. For further information, contact iaoffce@jpl.nasa.gov.
NPO-41381

Improved Signal Chains for Readout of CMOS Imagers

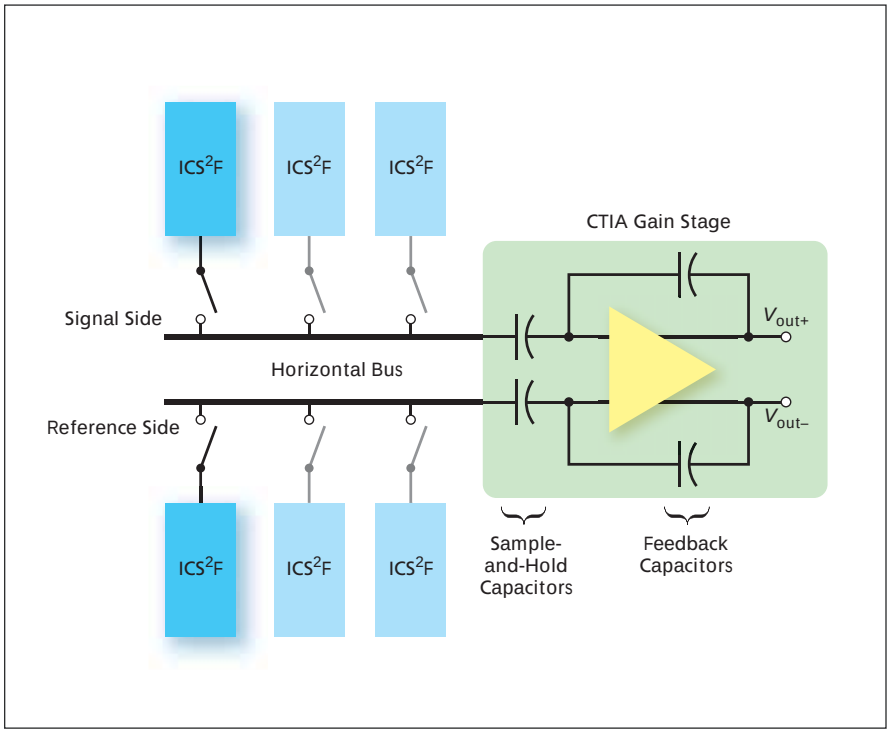
Two major imitations of prior readout signal chains are overcome.

NASA's Jet Propulsion Laboratory, Pasadena, California

An improved generic design has been devised for implementing signal chains involved in readout from complementary metal oxide/semiconductor (CMOS) image sensors and for other readout integrated circuits (ICs) that perform equivalent functions. The design applies to any such IC in which output signal charges from the pixels in a given row are transferred simultaneously into sampling capacitors at the bottoms of the columns, then voltages representing individual pixel charges are read out in sequence by sequentially turning on column-selecting field-effect transistors (FETs) in synchronism with source-follower- or operational-amplifier-based amplifier circuits.

The improved design affords the best features of prior source-follower-and operational-amplifier-based designs while overcoming the major limitations of those designs. The limitations can be summarized as follows:

- For a source-follower-based signal chain, the ohmic voltage drop associated with DC bias current flowing through the column-selection FET causes unacceptable voltage offset, nonlinearity, and reduced small-signal gain.
- For an operational-amplifier-based signal chain, the required bias current and the output noise increase superlinearly with size of the pixel array because of a corresponding increase in the effective capacitance of the row bus used to couple the sampled column charges to the operational amplifier. The effect of the bus capacitance is to simultaneously slow down the readout circuit and increase noise through the Miller effect.



The **Improved Design** affords the best features of prior source-follower and operational-amplifier designs.

The improved design (see figure) provides a switched source follower in each column, one each for the signal and reference samples [denoted an in-column switched source follower (ICS^2F)], followed by a single capacitive transimpedance amplifier (CTIA) gain stage. The ICS^2F consists of a different configuration of the column-selecting FET such that no DC bias current flows through it, and hence, without the associated ohmic voltage drop. Unlike in a prior operational-amplifier-based design involving direct connection of the sample and hold capacitors to the row-bus, the input terminals of the amplifier present CTIA gain stage are not in direct contact with the bus and, therefore, this stage produces voltage gain without the bandwidth reduction and noise multiplication that is caused by the Miller effect. Secondly, as a result of using ICS^2Fs, the bus carries a predominantly voltage signal, (as opposed to a predominantly

charge signal as in a prior operational-amplifier-based signal chain). Hence, the charging and discharging of the bus is not slowed by the Miller effect, enabling reduction of the bias current from the value that would otherwise be needed. The elimination of the ohmic drop across the column-selecting switch reduces the output voltage offset to a minimum, eliminates nonlinearity, and makes the small-signal gain approach its ideal value of unity.

This work was done by Bedabrata Pain, Bruce Hancock, and Thomas Cunningham of Caltech for NASA's Jet Propulsion Laboratory.

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SOI CMOS Imager With Suppression of Cross-Talk

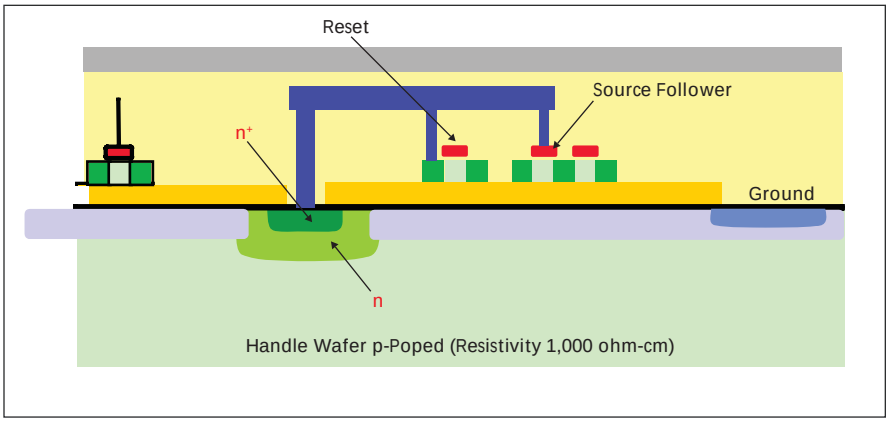
Potential applications are diverse, ranging from astronomy to medical imaging.

NASA's Jet Propulsion Laboratory, Pasadena, California

A monolithic silicon-on-insulator (SOI) complementary metal oxide/semiconductor (CMOS) image-detecting integrated circuit of the active-pixel-sensor type, now undergoing development, is designed to operate at visible and near-infrared wavelengths and to offer a combination of high quantum efficiency and low diffusion and capacitive cross-talk among pixels. The imager is designed to be especially suitable for astronomical and astrophysical applications. The imager design could also readily be adapted to general scientific, biological, medical, and spectroscopic applications.

One of the conditions needed to ensure both high quantum efficiency and low diffusion cross-talk is a relatively high reverse bias potential (between about 20 and about 50 V) on the photodiode in each pixel. Heretofore, a major obstacle to realization of this condition in a monolithic integrated circuit has been posed by the fact that the required high reverse bias on the photodiode is incompatible with metal oxide/semiconductor field-effect transistors (MOSFETs) in the CMOS pixel readout circuitry.

In the imager now being developed, the SOI structure is utilized to overcome this obstacle: The handle wafer is retained and the photodiode is formed in the handle wafer. The MOSFETs are formed on the SOI layer, which is separated from the handle wafer by a buried oxide layer. The electrical isolation provided by the buried oxide layer makes it possible to bias the MOSFETs at CMOS-compatible potentials (between 0 and 3 V), while biasing the photodiode at the required higher potential, and enables independent optimization of the sensory and readout portions of the imager.



A **Photodiode Is Formed in the Handle Wafer** between an implanted n-doped well and the rest of the handle wafer, which is p-doped. This arrangement makes it possible to apply a high reverse bias to the diode, as needed for high quantum efficiency and low diffusion cross-talk.

The figure presents a simplified and partly schematic cross section of one pixel. The photodiode is formed, in the handle wafer, between an implanted deep n-doped well and the rest of the handle wafer. An n^+-doped cathode contact region in the well is electrically connected by a tungsten via plug to the source of a reset FET residing on the SOI layer. The bottom of the handle wafer is reverse-biased to 30 V, while the n^+-doped cathode contact region is subject to potential excursions of 1 to 2 V, which are within permissible voltage limits. The reverse bias of the handle wafer is brought in from the front side (the top side in the figure) through a p^+-doped anode guard ring positioned and dimensioned to prevent breakdown of Si or SiO_2 in the presence of the bias potential. An implanted boron pinning layer, biased at a small negative potential, holds the interface between the buried oxide and the handle-wafer silicon in equilibrium and thereby helps to minimize dark current.

The potential difference ($\oplus$30 V) between the pinning layer and the bottom of the handle wafer could result in undesired ohmic conduction between them. Therefore, the doping profiles are chosen in conjunction with the device geometry (including the dimensions of, and spacing between, the n-doped wells) to shape the electric field to create a pinch-off region (a potential barrier) that prevents such conduction. The pinch-off region also prevents electric-field coupling between adjacent n-doped wells, thereby eliminating inter-pixel capacitance and the associated capacitive cross-talk between pixels.

The reset FET is, more specifically, an n-type FET, chosen to prevent inadvertent forward-biasing of the sensory node during reset-switch turn-off. The back and front gates of the reset FET are connected to each other in order to set the minimum anode potential such that the pinch-off condition is maintained for all illumination conditions.