trolyte formulation (comprised a 3:1 AN/DX blend), it was found that dc charging and discharging at a temperature as low as –75 °C is possible, albeit with capacitance reduced to about half its room-temperature value. By tailoring the nature of the co-solvent and the concentration of the salt used, the ESR can be minimized as well (see figure).

This work was done by Erik J. Brandon, William C. West and Marshall C. Smart of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

Innovative Technology Assets Management
JPL
Mail Stop 202-233
4800 Oak Grove Drive
Pasadena, CA 91109-8099
E-mail: iaoffice@jpl.nasa.gov

Refer to NPO-44386, volume and number of this NASA Tech Briefs *issue, and the page number.*

Making a Back-Illuminated Imager With Back-Side Contact and Alignment Markers

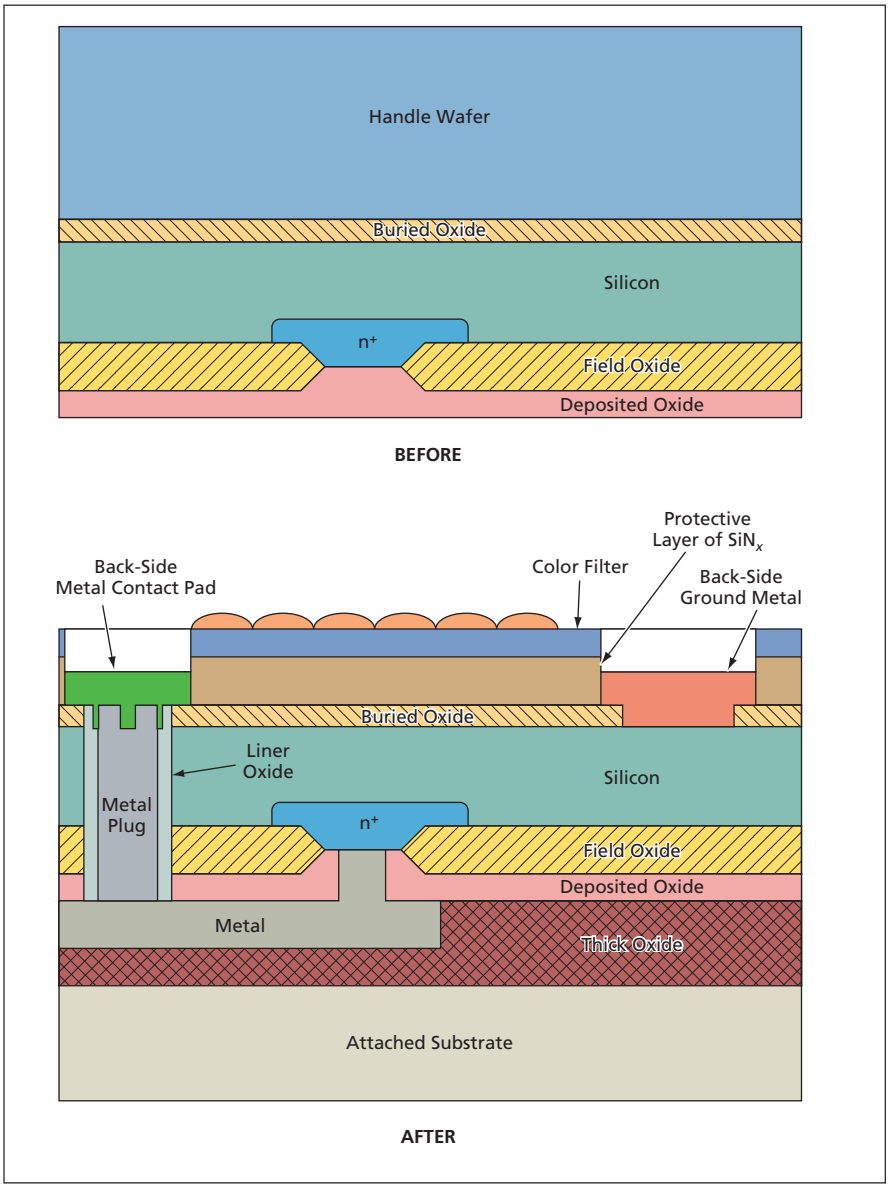
Metal plugs provide both electrical contact and alignment.

NASA's Jet Propulsion Laboratory, Pasadena, California

A design modification and a fabrication process that implements the modification have been conceived to solve two problems encountered in the development of back-illuminated, back-side-thinned complementary metal oxide/semiconductor (CMOS) image-detector integrated circuits. With respect to such an integrated circuit to be fabricated on a silicon substrate, the two problems are (1) how to form metal electrical-contact pads on the back side that are electrically connected through the thickness in proper alignment with electrical contact points on the front side and (2) how to provide alignment keys on the back side to ensure proper registration of back-side optical components (e.g., microlenses and/or color filters) with the front-side pixel pattern. (In this special context, "front side" signifies that face of the substrate upon which the pixel pattern and the associated semiconductor devices and metal conductor lines are formed.)

The essence of the design modification is to add metal plugs that extend from the desired front-side locations through the thickness and protrude from the back side of the substrate. The plugs afford the required front-to-back electrical conduction, and the protrusions of the plugs serve as both the alignment keys and the bases upon which the back-side electrical-contact pads can be formed.

The fabrication process for implementing this design modification would be complex and would be subject to variation as needed for different image-detector applications. Immediately before the beginning of this process, the integrated circuitry would already have been fabricated on the front side of the sub-



These **Simplified Cross Sections** (not to scale) depict the effect of the design modification and process on part of one pixel.

strate, as shown in the upper part of the figure. In terms that are necessarily oversimplified for the sake of brevity, the process can be summarized as follows: Through multiple steps of patterning, etching, and deposition, holes through the substrate would be formed at the desired front-side locations and the metal plugs and their protrusions would be formed in the holes. In subsequent steps, the back-side metal pads would be deposited on the metal plug protrusions, then color filters and/or microlenses would be formed between and in alignment with the metal contact pads, yielding the device structure shown in the lower part of the figure. (Not shown in the figure is a back-side antireflection coat that would be added near the end of the process.)

This work was done by Bedabrata Pain of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

Innovative Technology Assets Management
JPL
Mail Stop 202-233
4800 Oak Grove Drive
Pasadena, CA 91109-8099
(818) 354-2240
E-mail: iaoffice@jpl.nasa.gov

Refer to NPO-42839, volume and number of this NASA Tech Briefs *issue, and the page number.*

Compact, Single-Stage MMIC InP HEMT Amplifier

This amplifier exhibits gain of 5 dB at 340 GHz.

NASA's Jet Propulsion Laboratory, Pasadena, California

Figure 1 depicts a monolithic microwave integrated-circuit (MMIC) single-stage amplifier containing an InP-based high-electron-mobility transistor (HEMT) plus coplanar-waveguide (CPW) transmission lines for impedance matching and input and output coupling, all in a highly miniaturized layout as needed for high performance at operating frequencies of hundreds of gigahertz. This is one in a series of devices that are intermediate products of a continuing effort to develop advanced MMIC amplifiers for submillimeter-wavelength imaging systems, scientific instrumentation, heterodyne receivers, and other applications.

The amplifier is designed for operation at a nominal frequency of 340 GHz. The HEMT in this amplifier has a gate length of 35 nm and two fingers each 15 μm wide. The CPWs have a ground-to-ground spacing of only 14 μm. The inclusion of quarter-wavelength-long CPWs for impedance matching and of on-chip shunt capacitors makes it possible to obtain about 5 dB of gain with respectable values of input and output return losses at the design frequency of 340 GHz (see Figure 2). This is among the highest gains per stage at this frequency reported to at the time of this work. Moreover, the measurement data suggest potential for further increase in gain with frequency beyond the 345-GHz limit of the test equipment used to perform the measurements.

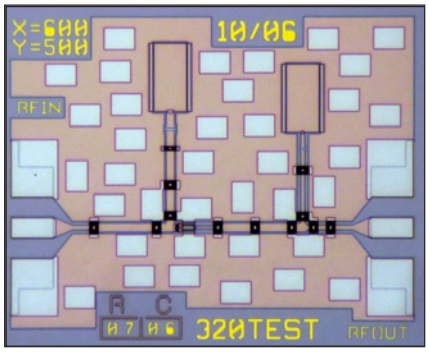


Figure 1. This **MMIC Single-Stage Amplifier** is a prototype of larger, multistage MMIC amplifiers that will incorporate HEMTs of 35-nm gate length.

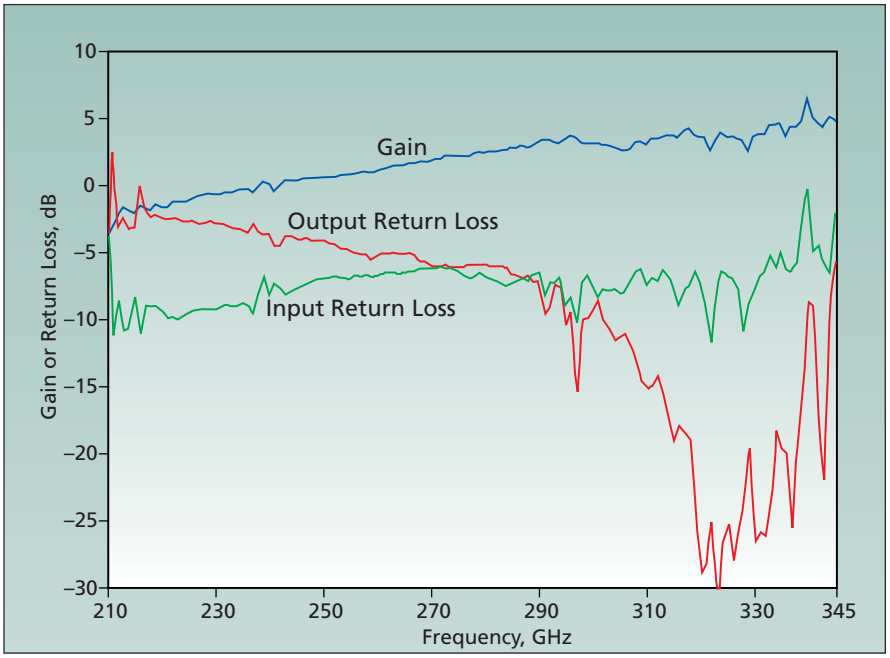


Figure 2. **Gain and Input and Output Return Losses** of the amplifier of Figure 1 were measured as a function of frequency.

This work was done by David Pukala, Lorene Samoska, King Man Fung, and Todd Gaier of Caltech and W. R. Deal, Gerry Mei, Vesna Radisic, and Richard Lai of Northrop Grumman Corporation for NASA's Jet Propulsion Laboratory. The contributors would like to acknowledge the support of Dr. Mark Rosker and the Army Research Laboratory. This work was supported by the DARPA SWIFT Program and Army Research Laboratory under the DARPA MIPR no.06-U037 and ARL Contract no. W911QX-06-C-0050. Further information is contained in a TSP (see page 1).

NPO-44962