responding locations on, and as an integral part of, this integrated circuit; or (2) following a flip-chip approach, fabricate the array of energy-storage elements on a separate integrated-circuit chip and then align and bond the two chips together.

This work was done by Mohammad Mojarradi, Mahmoud Alahmad, Vinesh Sukumar, Fadi Zghoul, Kevin Buck, Herbert Hess, Harry Li, and David Cox of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

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Lower-Dark-Current, Higher-Blue-Response CMOS Imagers

Semiconductor junctions are relocated away from Si/SiO_2 interfaces.

NASA's Jet Propulsion Laboratory, Pasadena, California

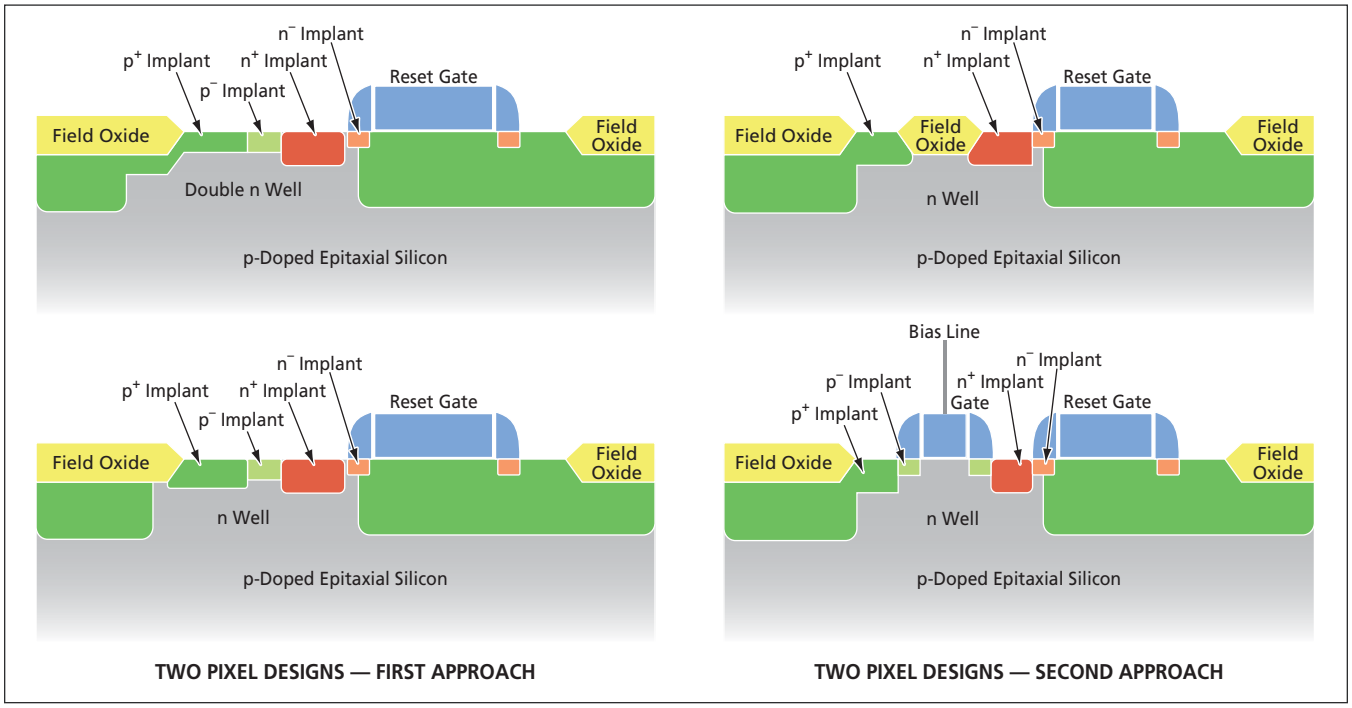
Several improved designs for complementary metal oxide/semiconductor (CMOS) integrated-circuit image detectors have been developed, primarily to reduce dark currents (leakage currents) and secondarily to increase responses to blue light and increase signal-handling capacities, relative to those of prior CMOS imagers. The main conclusion that can be drawn from a study of the causes of dark currents in prior CMOS imagers is that dark currents could be reduced by relocating p/n junctions away from Si/SiO_2 interfaces. In addition to reflecting this conclusion, the improved designs include several other features to counteract dark-current mechanisms and enhance performance.

The left half of the figure illustrates two of the improved designs, in which p-doped implants are added, variously, underneath and/or at the edges of the field oxide regions. These implants hold the Si/SiO_2 interfaces in thermal equilibrium and prevent generation of dark current at the interfaces. In covering the field oxide, the p implants separate the p/n junctions from the Si/SiO_2 interfaces, so that the interfacial component of the dark current (which is the major component) is greatly reduced.

Beyond a certain electric strength, the leakage current depends very strongly on the strength of the electric field. In order to reduce electric fields in the reverse-biased junctions, the p wells are separated from the n wells. A double n well in each pixel is preferred, both for increased photocarrier-collection efficiency and for tailoring the doping so that the electric field in the transition region between p^+-to-n-well region is low.

For electrical connections to the photodiodes, which also act as the sources of reset field-effect transistors, n^+ implants are necessary. Unfortunately, the p^+/n^+ junctions heretofore associated with such implants are undesirable because they contain high electric fields, which give rise to significant tunneling currents, which, in turn, are components of dark currents. In these designs, p-implants are added at the surfaces to tailor the doping from p^+ accumulation layers to n^+ source layers, thereby reducing tunneling currents.

Two of the improved designs illustrated in the right half of the figure follow an alternative approach to tailoring



These **Cross Sections of a Pixel** in a CMOS imager represent four designs that provide for reduction of dark currents in different ways.

appropriate transitions between surface p^+ accumulation layers and n^+ source layers. In this approach, field oxide regions or gates are positioned to separate the p^+ and n^+ regions. A gate separating the p and n regions can be DC-biased to prevent conduction of current underneath the gate, thereby providing sufficient isolation between the p and the n regions. Alternatively, instead of being DC-biased, the p/n-separating gate in each pixel can be electrically tied to the reset gate of that pixel to obtain a more-compact layout.

According to each of these designs, a double p/n junction is formed in each pixel: one junction near the surface between the p^+ and the n well, the other in the bulk between the n well and the p-doped epitaxial silicon. The near-surface junction provides increased response to blue light because blue photons are absorbed close to the surface. In addition, the double junction increases the pixel capacitance, thereby imparting larger signal-handling capacity to a pixel. This increase in capacitance is particularly beneficial in an imager having small pixels, wherein the limited size of photodiodes causes pixel capacitance to be extremely small.

This work was done by Bedabrata Pain, Thomas Cunningham, and Bruce Hancock of Caltech for NASA's Jet Propulsion Laboratory.

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

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