guide bridges at the junction; the inductive behavior of the bridges, in addition to CPW parasitic resonances, degrades the passband performance of the balun.

The new double-Y balun transitions from a microstrip line with truncated ground plane to a CPS line. The balun does not employ CPW lines; hence, CPW bridges are not required at the junction. In addition, the balun does not exhibit CPW parasitic resonances, thereby improving passband performance.

Figure 1 illustrates the new version of the double-Y balun designed to feed a complementary spiral antenna. Panels on the right illustrate an expanded view of the balun junction. Preliminary voltage standing-wave ratio (VSWR) and insertion loss data are illustrated in Figure 2. Measured data were compared with numerical results computed using Momentum. It is seen that the balun exhibits a VSWR of less than 1.5 from 400 MHz to 8 GHz and a VSWR of less than 1.8 up to 13 GHz. The VSWR can be reduced further by reducing reflections from the balun junction and load resistor. Also, the balun is seen to exhibit an insertion loss of less than 1.5 dB up to 12 GHz. Further work involves characterizing the balun's performance when feeding a complementary spiral antenna.

This work was done by Jaikrishna Venkatesan of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).
NPO-42763

A Topographical Lidar System for Terrain-Relative Navigation

Demand for memory is reduced by digitizing over a limited altitude range.

NASA's Jet Propulsion Laboratory, Pasadena, California

An imaging lidar system is being developed for use in navigation, relative to the local terrain. This technology will potentially be used for future spacecraft landing on the Moon. Systems like this one could also be used on Earth for diverse purposes, including mapping terrain, navigating aircraft with respect to terrain and military applications. The system has been field-tested aboard a helicopter in the Mojave Desert.

The use of imaging lidar systems to generate digital data sets equivalent to topographical maps is well established. Such systems are commercially available and often denoted simply as topographical or topographic lidar systems. As in other imaging lidar systems, a gimballed, actuated mirror is used to raster-scan a narrow laser beam across a field of view, the laser beam is emitted in short laser pulses, the pulses are reflected from the terrain, and the distance to the terrain in a given direction is determined from the total time of flight from the emission of the outgoing pulse to the receipt of the reflected pulse. Then the combination of direction (azimuth and elevation angles associated with the mirror orientation) and the range (distance) for each such direction constitute raw data that can be used to generate a topographical map of the terrain.

When this system was designed, digitizers with sufficient sampling rate (2 GHz) were only available with very limited memory. Also, it was desirable to limit the amount of data to be transferred between the digitizer and the mass storage between individual frames. One of the novelty design features of this system was to design the system around the limited amount of memory of the digitizer. The system is required to operate over an altitude (distance) range from a few meters to ≈1 km, but for each scan across the full field of view, the digitizer memory is only able to hold data for an altitude range no more than 100 m. Therefore, the acquisition of data is limited to an altitude range 100 m wide in the following way: Initially a pulse is emitted and digitized over an altitude range of 5 km. This process is repeated four more times, and the median time of the first return pulse of all five measurements is computed as the distance from which to expect future laser pulse to be reflected. A distance of 50 m is subtracted from the expected distance and the resulting distance is fed as a programming input to a programmable-delay pulse generator, which is triggered by the outgoing laser pulse and which, in turn, turns on the digitizer after the programmed delay. Thus, the digitizer is started at 50 m before the expected receipt of the return pulse. The digitizer then operates over an altitude interval of 100 m; it is stopped at 50 m after the expected return of the receipt of the return pulse.

This work was done by Carl Christian Liebe, Gary Spiers, Randy Bartman, Raymond Lam, James Alexander, James Montgomery, Hannah Goldberg, Andrew Johnson, Patrick Meras, and Peter Palacios of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-44586

Programmable Low-Voltage Circuit Breaker and Tester

This system could also detect some faults before turning on power.

John F. Kennedy Space Center, Florida

An instrumentation system that would comprise a remotely controllable and programmable low-voltage circuit breaker plus several electric-circuit-testing subsystems has been conceived, originally for use aboard a spacecraft during all phases of operation from pre-launch testing through launch, ascent, orbit, descent, and landing. The system could also be adapted to similar use aboard aircraft. In comparison with remotely controllable circuit breakers heretofore commercially available, this system would be smaller, less massive, and capable of performing more functions, as needed for aerospace applications.

The circuit breaker in this system could be set open or closed and could be monitored, all remotely. Trip current could be set at a specified value or could be made to follow a trip curve (a specified trip current as a function of time). In a typical application, there might be a requirement to set a lower trip current

or lower trip-curve values to protect circuits during initial testing, and to set a default higher trip current during subsequent pre-launch and launch operations.

In the open state of the circuit breaker, one of the circuit-testing subsystems could obtain electrical-resistance readings on the load side as indications of whether faults are present, prior to switching the circuit breaker closed. Should a fault be detected, another circuit-testing subsystem could perform time-domain reflectometry, which would be helpful in locating the fault. On the power-line side, still another circuit-testing subsystem could take a voltage reading, as an indication of whether the proper voltage is present, prior to switching the circuit breaker closed.

The system would be contained in a housing, with input, output, and data/control connectors on the rear surface. All monitoring, control, and programming functions would ordinarily be performed from a remote console. On the front surface, there would be a push-button switch for optionally locally setting the circuit breaker in the open or closed state, plus a lamp that would provide a local visual indication of whether the circuit breaker was in the open (initially set), closed, or open (tripped) state.

The aforementioned monitoring, testing, state-setting, and trip-current-setting functions would be effected by circuitry on an integrated-circuit card inside the housing. Also on the card would be (1) input and output circuitry for remote monitoring and control and (2) a tag random-access memory as an electronic means of identifying the system by serial number, location, a reference designation, and operational characteristics.

This work was done by Terry Greenfield of ASRC Aerospace Corp. for Kennedy Space Center. For further information, contact the Kennedy Innovative Partnerships Program Office at (321) 861-7158. KSC-12742

Electronic Switch Arrays for Managing Microbattery Arrays

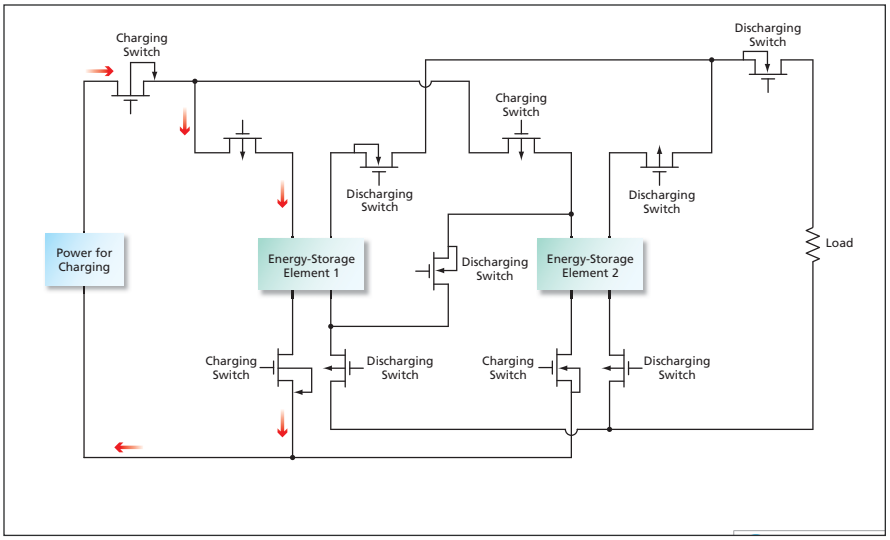
Array circuitry is dynamically configured to optimize performance and disconnect defective elements.

NASA's Jet Propulsion Laboratory, Pasadena, California

Integrated circuits have been invented for managing the charging and discharging of such advanced miniature energy-storage devices as planar arrays of microscopic energy-storage elements [typically, microscopic electrochemical cells (microbatteries) or microcapacitors]. The architecture of these circuits enables implementation of the following energy-management options:

- Dynamic configuration of the elements of an array into a series or parallel combination of banks (subarrays), each array comprising a series or parallel combination of elements;
- Direct addressing of individual banks for charging and/or discharging; and
- Disconnection of defective elements and corresponding reconfiguration of the rest of the array to utilize the remaining functional elements to obtain the desired voltage and current performance.

One of the reasons for fabricating microbattery and microcapacitor arrays is that the array form affords partial immunity to defects in individual energy-storage elements. Defective energy-storage elements act as loads on the functional ones, thereby reducing the capacity of an overall array. By enabling the disconnection of defective elements and reconfiguration of the rest of the array, the present invention offers practical means to realize this partial immunity. In addition, the invention provides for interrogating individual cells and banks in the array and charging them at the current-vs.-time or voltage-vs.-time characteristics needed for maximizing the life of the array.



Two Energy-Storage Elements can be connected, individually or together in series or parallel, to the power source or the load by closing or opening the appropriate subset of switching transistors. This example has been greatly oversimplified for the sake of illustrating the basic principle; a typical practical circuit would contain many more energy-storage elements and switches.

An integrated circuit according to the invention consists partly of a planar array of field-effect transistors that function as switches for routing electric power among the energy-storage elements, the power source, and the load (see figure). To connect the energy-storage elements to the power source for charging, a specific subset of switches is closed; to connect the energy-storage elements to the load for discharging, a different specific set of switches is closed.

Also included in the integrated circuit, but omitted from the figure for the sake of simplicity, is circuitry for monitoring and controlling charging and discharging. The control and monitoring circuitry, the switching transistors, and interconnecting metal lines are laid out on the integrated-circuit chip in a pattern that registers with the array of energy-storage elements. There is a design option to either (1) fabricate the energy-storage elements in the cor-