



Radiation Effects on Emerging Technologies: Implications of Space Weather Risk Management

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39th Aerospace Sciences Meeting & Exhibit
26-29 September 2000
Long Beach, California

RADIATION EFFECTS ON EMERGING TECHNOLOGIES: IMPLICATIONS OF SPACE WEATHER RISK MANAGEMENT

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Abstract

As NASA and its space partners endeavor to develop a network of satellites capable of supporting humankind's needs for advanced space weather prediction and understanding, one of the key challenges is to design a space system to operate in the natural space radiation environment. In this paper, we present a description of the natural space radiation environment, the effects of interest to electronic or photonic systems, and a sample of emerging technologies and their specific issues. We conclude with a discussion of operations in the space radiation hazard and considerations for risk management.

Introduction

Among the most challenging aspects of developing systems for space is the performance of electronic and photonic systems in the natural space radiation environment.¹ One should note that the radiation hazard for a specific mission is not generic: each mission orbit, timeframe, duration, and spacecraft design implications (i.e., the varying amount of structural shielding in differing satellite configurations) derive unique requirements and challenges to the system design. This natural space radiation hazard varies significantly:

- from missions with severe requirements that fly in the heart of the Van Allen belts where trapped energetic particles lurk. One such example would be a medium earth orbit or MEO.
- to avionics systems in the upper atmosphere that are protected from many energetic particle concerns, but still must deal with secondary particles such as neutrons. The concept of an error occurring in critical electronics of a manned aircraft is unsettling at best.

Long and short term radiation effects such as total ionizing dose (TID), displacement damage dose (DDD), and single event effects (SEE) provide aerospace designers' a myriad of challenges for reliable system design.

Adding complication to this concern is the use of new, emerging, and in some cases unproven technologies that often have new or increased susceptibility to radiation concerns.² In this paper, we attempt to provide a basic understanding of the natural space radiation environment's effects on technology as well as a discussion of the implications of such effects and risk management techniques available to cope with them.

Two items should be noted as well. The first is that we are discussing the natural space radiation environment and not the induced radiation environment that is of concern for military applications. The second is that the technology focus of this paper is on electronic and photonic technologies. This is not to say that other technology concerns do not exist, simply that it is outside the scope of this presentation.

The Natural Space Radiation Hazard

The near-Earth natural radiation environment can be divided into two categories, the particles trapped in the Van Allen belts and the transient environment. Fig. 1 shows a representation of the environment population. The particles trapped in the near-Earth environment are composed of energetic protons, electrons, and heavy ions. The transient radiation consists of galactic cosmic ray particles and particles from solar events (coronal mass ejections and flares). The cosmic rays have low-level fluxes with energies up to TeV and include all ions in the periodic table. The solar eruptions produce energetic protons, alpha particles, heavy ions, and electrons. To the first order, all of these particle populations are omnidirectional and isotropic.

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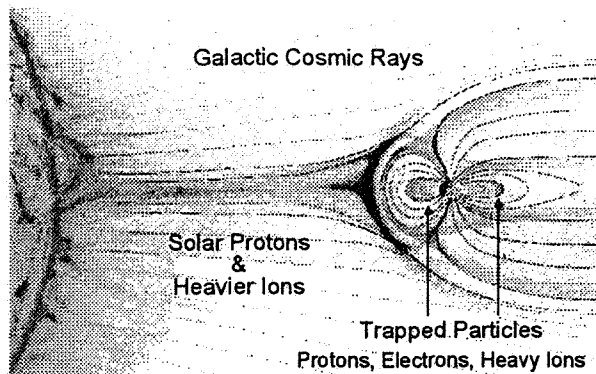


Fig. 1: A representation of the radiation environment.

K. Endo, Nikeii Corporation

Space also contains a low energy plasma of electrons and protons with fluxes up to 10^{12} cm²/sec. In the trapped particle regions, the plasma is the low energy (< 0.1 MeV) component of the charged particles. In the outer regions of the magnetosphere and in interplanetary space, the plasma is associated with the solar wind. Because of its low energy, the plasma is easily stopped by thin layers of material so it is not a hazard to most spacecraft electronics. However, it is damaging to surface materials and can contribute to spacecraft surface charging and discharging problems.^{3,4} All particles are isotropic and omnidirectional.

Complete discussions of the radiation environment, its measurement, and models can be found in Barth and Dyer.^{5,6}

Trapped Protons and Electrons

The trapped particles pose a significant radiation threat to electronic systems and humans. There are large variations in the level of hazard depending on the orbit of the spacecraft, solar activity, and magnetospheric conditions. Both the protons and electrons contribute to total ionizing dose damage. For some electronic parts, single event effects induced by protons are also a hazard. Protons also contribute to degradation due to non-ionizing energy loss. Protons are especially problematic because of their high energies and penetrating power. As mentioned above, low energy electrons are the cause of electrostatic discharging which can be a serious problem for spacecraft in higher altitude orbits (e.g., geostationary) where they are exposed to more intense electron populations. Higher energy electrons can penetrate into the spacecraft, collect in insulator materials, and discharge causing damage to electronics. In fact, an analysis of system anomalies from the CRRES satellite showed that most of the anomalies were related to deep dielectric discharging.⁷

Galactic Cosmic Ray Heavy Ions

The flux levels of the galactic cosmic rays (GCRs) are low compared to the trapped particles, but they are hazardous to spacecraft electronics because their high energies make them extremely penetrating. Also, they have a high rate of energy deposition as measured by their linear energy transfer (LET) rate. A particle's LET is primarily dependent on the density of the target material and, to a lesser degree, the density and thickness of the shielding material. It is their high LET that makes cosmic rays an important contributor to single event effects problems for spacecraft, especially in orbits where the magnetosphere offers little protection.

The total dose deposition in silicon is only 10 rads/year when the GCR environment is at its peak. However, when the GCR dose is converted to dose equivalent in units of rem for biological systems, it can reach dangerous levels for humans. This can be true even for low earth orbits where the effect of the magnetospheric attenuation on the fluence levels of cosmic ray particles is significant.

Solar Particles

~~The particles from solar events are a concern for spacecraft designers.~~ In fact, for spacecraft in orbits exposed to these particles, they are often the driver for setting single event effects requirements. At this time there is no method for predicting when these events will occur. Warnings have short lead times and are not dependable. Experimenters have measured single event upsets on several satellites during solar events and quiet times. Harboe-Sørensen *et al.* measured daily SEU rates in regions of space where $L > 2$ and found that, during the October 1989 solar particle event, the rates increased by factors of 3 to 30 depending on the SRAM or DRAM memory type.⁸ Adams *et al.* measured a similar response to the October 1989 event in memories on board the Meteosat-3, which was in a geostationary orbit.⁹ Mullen and Ray also observed increased SEU rates during the March 1991 event in GaAs 1K RAMs on board the CRRES satellite.¹⁰ The solar proton component of the solar particle events must also be evaluated for the level of degradation damage for both ionizing and non-ionizing effects.

For systems that must operate during a solar particle event, the effect that both the solar protons and the solar heavy-ions has on single effects rates must be evaluated. The heavier ions make only a very small contribution to the dose levels. However, single event effects induced by solar heavy ions pose a serious problem for spacecraft systems that must operate during a solar event, because the particle levels are orders of

magnitude higher than the background galactic cosmic rays. For the systems that must operate during a solar particle event, the effect that both the solar protons and the heavy-ions has on single effects rates needs to be evaluated. It is especially important to take the peak flux levels into consideration. When setting part requirements and operational guidelines, one must remember that peak solar particle conditions exist for only a small part of the total mission time.

Protons from solar particle events also contribute to total dose and solar cell damage especially for interplanetary missions and those at geostationary and in geostationary transfer orbits. Adams *et al.* measured doses with RADFETs on the Meteosat-3 and found that doses increased a factor of 20 with the onset of the October 1989 event.⁹

Natural Space Radiation Effects on Technology

The effects from the natural space radiation environment may be divided into two categories: long-term and short-term. The long-term effects have two separate concerns: ionizing and non-ionizing damage. Short-term effects are concerned primarily with single particle ionization and/or secondary particle formation. One should note that even short-term effects may be permanent (i.e., destructive single particle events).

Alternatively, one may view ionizing radiation effects in space electronics in two parts: total ionizing dose (TID) and single event effects (SEE).¹¹ The two effects are distinct, as are their requirements and mitigation techniques. Though these effects are often a prime driver when discussing mission requirements, the non-ionizing radiation effects such as displacement damage dose (DDD) must also be considered.¹²

TID

TID is a long-term degradation of electronics due to the cumulative energy deposited in a material. Typical effects include parametric failures, or variations in device parameters such as leakage current, threshold voltage, etc., or functional failures. Significant sources of TID exposure in the space environment include trapped electrons, trapped protons, and solar protons.

DDD

DDD often has similar long-term degradation characteristics to TID, but is a separate physical mechanism. It should be noted that technologies that are tolerant to TID are NOT necessarily tolerant to DDD.

DDD is essentially the cumulative degradation resulting from the displacement of nuclei in a material from their lattice position. Over time, sufficient displacement can occur and may change the device or material performance properties. Prime sources of DDD exposure include trapped protons, solar protons, radioisotope thermoelectric generator (RTG) neutrons, and to a lesser extent for typically electronic systems, trapped electrons.

SEEs

SEEs occur when a single ion strikes a material, depositing sufficient energy either through its prime strike (e.g., direct ionization via GCR) or by the secondary particles that occur from the strike (e.g., indirect ionization via protons) to cause an effect in the device. The many types of SEE may be divided into two main categories: soft errors and hard errors.

In general, a soft error occurs when a transient pulse or bit-flip in the device causes an error detectable at the device output. Therefore, soft errors are entirely device and design specific, and are best categorized by their impact on the device. This is briefly shown in Table 1.

Table 1. Soft Errors

Event	Description	Sample Impact
Single Event Upset (SEU)	Bit-flip to a memory cell or latch structure	Location-specific: can corrupt program flow or data content.
Single Event Functional Interrupt (SEFI)	An SEU that causes a corruption in device/system operation	May halt system and require a reset or power cycling to clear
Single Event Transient (SET)	A single particle induced spike on the output of structure such as an operational amplifier or combinatorial logic.	Application-specific pending the shape of the transient and it's effect on follow-on circuitry.

Hard errors may be - but are not necessarily - physically destructive to the device, and may cause permanent functional effects. Table 2 lists some of the potential hard errors that can occur.

Table 2 Hard Errors

Event	Description
Single Event Latchup (SEL)	A potentially destructive condition involving parasitic circuit elements. During a traditional or destructive SEL, the device current exceeds the maximum specified for the device. Unless power is removed, the device will eventually be destroyed.
SEL – Microlatch	A type of SEL where the device current is elevated, but below the device's specified maximum. May or may not be destructive.
Single Hard Error (SHE)	A permanent change in the operation of the device. A common example would be a stuck bit in a memory device.
Single Event Gate Rupture (SEGR)	<i>Destructive</i> burnout of a gate insulator in a power MOSFET
Single Event Burnout (SEB)	A highly localized <i>destructive</i> burnout of the drain-source in power MOSFETs (metal oxide semiconductor field effect transistors)
Single Event Dielectric Rupture (SEDR)	<i>Destructive</i> burnout of a gate dielectric. Most common in one-time programmable devices.
Single Event Snapback (SES)	A reduction in the breakdown voltage of a parasitic transistor that is caused by the injection of minority carriers from the source diffusion to the well. Snapback also causes local loss of functional operation, along with an increase in current. However, much smaller currents generally occur as a result of snapback as compared to SEL.

Impacts of Space Radiation Effects on Satellite Systems

TID/DDD

Device parametric and permanent functional degradations are the principal failure modes of electronics associated with the TID/DDD environment. Since TID/DDD are cumulative effects, radiation tolerances of devices are akin to mean-time-to-failure (MTTF) numbers. This is where the time-to-failure is the amount of mission time until the device has encountered sufficient dose to cause failure. It should be noted that degradation may be gradual or rather abrupt. Two examples illustrate this. The first is an increase in device leakage current that might gradually double in a year's period or in a single orbit. The second is when sporadic errors begin occurring after a year in orbit as opposed to a hard failure that suddenly occurs.

Factors such as the mission's orbit, launch date, and launch length determine the external radiation environment. The device exposure to this hazard is then determined by the amount of shielding between the device and this external environment. Specific requirements and design considerations are therefore based on device location on or within the spacecraft.

SEE

Unlike TID/DDD tolerances, SEE rates are probabilistic, given as a predicted span of time within which a SEE will randomly occur. That is to say, SEE rate predictions are mean-time-between failures (MTBF) as opposed to MTTF.

The system-level impact of SEE depends on the type and location of the effect (hard or soft, recoverable or not), as well as on the specific system design. Hard errors, naturally, are of great concern to system reliability, since they may not be recoverable. Soft error effects such as the propagation of an SET or SEU through a circuit, subsystem, and system may also be of particular importance. For example, a device error or failure may propagate to critical mission elements, such as a command error affecting a thruster firing. There are also cases where SEEs may have little or no observable effect on a system level. In fact, in most designs, there are specific areas in which SEUs have less system impact from certain radiation effects. A data storage recorder utilizing a powerful error detection and correction (EDAC) code scheme would fit this category.

The more critical an SEE is to operational performance, the more strict the requirements levied on that component should be. Since SEE presents a functional impact to a device, functional analysis enables evaluation of severity. The design is viewed in terms of function, not by box or physical subsystem. Functions are categorized into defined "criticality classes", or categories of differing severity of SEE occurrence. For example, for a project, there might be three criticality groups for SEU: error-functional, error-vulnerable, and error-critical. Functions in the error-functional groups are unaffected by SEUs, whether it be due to an implemented error-correction scheme or redundancy. Functions in the error-vulnerable group might be those that the risk of a low probability is assumable. Functions in the error-critical group are functions where SEE is unacceptable.

It is important to note that, in general, shielding is not an effective mitigation tool for SEE, unless a device is soft to attenuable protons.

Sample Effects on Emerging Technologies

In an effort to increase space system performance in an era of reducing resources, many emerging technologies are being considered for space systems. Unfortunately, many of these technologies have increased or new radiation sensitivities.¹³ In addition, spacecraft size is shrinking and/or using newer composite materials. This provides less effective shielding for sensitive electronics. In summary, we are using more sensitive devices with less protection.

All is not lost, however. In this section, we'll describe a sampling of emerging technologies and some of their

radiation concerns. In the following section, we'll discuss some ways of reducing the risk of using these technologies.

A general trend will be pointed out: as systems are going faster (data rates > 1 gigabit per second or gbps), the SEU/SET sensitivities appear to be increasing. However, as will be discussed later, the impact of the error on a system must be evaluated to determine applicability.

Microelectronics are a staple of space system design. Table 3 provides a sample listing of emerging microelectronics technologies, technology trends, technology characteristics, and potential radiation issues and capabilities.

Table 3. Sample Microelectronics Technologies

Technology	Trends	Characteristics	Radiation
Complementary Metal Oxide Semiconductor (CMOS)	Shrinking feature size; Reduced voltage levels	Used in both digital and analog circuits	SEE sensitivity is suspect; TID appears improved with shrinking geometries/voltages
CMOS Ultra-Low Power (ULP)	Approaching voltages <<1V	Can enable reduced spacecraft volume/weight; May provide increased circuit performance	Design-specific; CMOS ULP Radiation-Insensitive Technology (CULPRIT) Program is aimed at a radiation tolerant version; Initial results are promising
CMOS Silicon-on-Insulator (SOI)	Improved wafer quality	Suitable for low-noise and higher performance; Mixed-signal potential	Design-specific; Potential for improved radiation tolerance has been demonstrated
CMOS Silicon-on-Sapphire (SOS)	Resurgence of older radiation hardened technology with better wafers and smaller feature size	Suitable for low-noise and higher performance; Mixed-signal potential	Test data looks promising on limited devices
Gallium Arsenide (GaAs)	???	Used in high-speed and radio frequency (RF) applications	Known TID/DDD hardness; Known SEU sensitivity; SEU-tolerance techniques have been demonstrated
Silicon Germanium (SiGe)	Shrinking feature size	Suitable for low-noise and higher performance; Mixed-signal potential; CMOS-compatible	Test data shows relatively good TID/DDD hardness; SEU sensitivity (tolerance techniques are being developed)
Indium Phosphide (InP)	???	Used in high-speed and radio frequency (RF) applications	Properties expected to be similar to GaAs and SiGe (good TID/DDD, SEU-sensitive)
Wide Bandgap (WBG)	SiC, GaN, Diamond, AlN	Expected use in power systems, detectors, tube replacement, etc.	Should be relatively good for TID/DDD, but little data exists



Another burgeoning area of technology insertion into space systems is photonics. With technologies such as exotic-doped fiber amplifiers and gbps fiber links being used, one must pay attention to radiation issues as well.

All components in a fiber system (detectors, transmitters, and optical fiber) should be considered for their radiation effects. A summary of radiation lessons learned has already been presented and we refer the interested reader to this reference for further detail.¹⁴

A second point is that most photonic links require a high-speed electrical interface. In many cases, the radiation performance of these electronics can be the limiting factor for the system.¹⁵

Managing Risk: Mitigation and Acceptance of Radiation Effects Risks^{11, 16}

TID/DDD

TID/DDD requirements are met through many avenues. Naturally, the first option is to procure devices hardened to the environment. This is also true for SEE. Unfortunately, hardened electronics technology can be difficult to obtain (cost, schedule) and lag significantly behind that of commercial technologies (two orders of magnitude or greater).

Shielding is an effective TID mitigation tool but may be costly in terms of the added weight to the spacecraft. The radiation environment external to the spacecraft is reduced and modified by the amount and types of materials between the external environment and the electronic device of interest. The spacecraft, instrument, electronic boxes, and any other material substance can all contribute to shielding. Representing these structures in a three-dimensional radiation model provides the means of calculating TID via 3-D ray trace methods at the component level or electronic box level. For critical missions or missions with high radiation environments, it is recommended to schedule a 3-D ray trace prediction close to the beginning of the preliminary design phase, when the spacecraft geometry is reasonably well defined and the boxes are arranged into the structure. With this method, component level and /or box level TID requirements can be set for the design. TID requirements stemming from this effort will be more accurate, and usually lower, than from an ideal geometry calculation, allowing for a more efficient design. Over-specifying tolerance requirements can be avoided with subsequent savings in costs. This overall process determines the effective shielding for a component and typically reduces the hardness required by a component.

It should be noted that DDD issues must be carefully looked at in this same manner. An energetic proton as it transits a material may lose energy, but that reduced energy may be more damaging than the original proton's energy. This is a very complex issue outside of the scope of this talk. Thus, we will emphasize TID mitigation techniques as opposed to the DDD issue.

Slight redesign at the spacecraft and/or subsystem level may reduce TID exposure levels without necessarily impacting the overall weight budget. Electronic boxes placed inside a spacecraft structure receive additional radiation shielding from the spacecraft when compared to those on the outside of the structure. In addition, electronic boxes placed closer together provide more shielding to each other than boxes further apart. Internal box structures and components also provide shielding. In essence, optimizing the mechanical box layout (location on/in the spacecraft) and devices within a box (where inside the box the component is located), provides a useful means of understanding or mitigating risk.

In some cases, the effective shielding may not be sufficient to reduce the TID requirement. In these cases, additional shielding may be added to the spacecraft with all the potential mechanical, thermal, and other design and cost constraints that one would expect. Some device packaging techniques are designed to increase radiation tolerance. However, these devices are typically costly and have long lead times for procurement. At a device level, spot shielding offers the least impact on the weight budget. However, for electronic boxes in which large amounts of circuitry must be protected, box-level shielding may be the only practical method of reducing dose through shielding.

Devices with unknown radiation tolerance characteristics should be replaced by alternates with known tolerance or else tested to TID or DDD as appropriate. Radiation testing of key devices with unknown tolerance early in the design phase reduces the risk of schedule and cost impacts required for circuit redesign and/or work-arounds. Although device TID tolerance may vary by a factor of two or more from lot to lot, look ahead testing of devices gives insights into their use. In later development phases, testing of the flight lot parts is critical for commercial grade devices to account for issues such as the lot-to-lot variations that often occur.

Redundancy of components is often considered as well as a means of mitigation. Redundancy with powered-on devices is not effective as mitigation, since these devices will also degrade at the same rate. Un-powered devices may or may not provide a means of mitigation (degradation may be less, more, or the same); this is very device and technology specific.

SEE

For simplicity, SEEs, may be divided into four categories: those that effect data or data streams, those that effect the operation or control of the system, transients, and destructive. There is some obvious overlap such as a bit error in a memory cell that can either be a data error or an error in a stored program (which affects operation).

It is also important to note that some SEEs may be acceptable when you look at mission requirements. An SEU rate causing a loss of 5% of the science data may be acceptable.

On the other hand, one also needs to understand when the payloads are required to gather data. For example, if a mission is looking to gather data during a solar particle event, a nominally accepted SEE rate (say, once a day) may not be acceptable during this event time period.

Data

There are several options for data-related SEU mitigation using encoding schemes on the device or data structure. First, parity checking is a "detect only" scheme, which counts the number of logic one states occurring in a data set, producing a single parity bit saying whether an odd or even number of ones were in that structure.¹⁷ This scheme will flag an SEU if an odd number of bits are in error, but not if an even number of bits are in error.

A second option, Hamming code, is known as single bit correct, double bit detect. The use of EDAC schemes such as this, known as scrubbing, is common among current solid-state recorders flying in space [for example, refs ^{18,19}]. Hamming code schemes encode an entire block of data with a check code; this method will detect the position of a single error, and the existence of more than one error in a data structure.¹⁷ Because the SEU position is known, it is possible to correct this error. This coding method is recommended for systems with low probabilities of multiple errors in a single data structure (e.g., only a single bit in error in a byte of data).

Other block error codes provide more powerful error correcting codes (ECCs). Among these, Reed-Solomon (R-S) coding is becoming widespread in its usage.²⁰ The R-S code is able to detect and correct multiple and consecutive errors in a data structure. An example [ref ²¹] is what is known as (255,223), or a 255 byte block with 223 bytes of data and 32 bytes of overhead. This particular R-S scheme is able to correct up to 16 consecutive bytes in error, and is available in a single IC designed by the NASA VLSI Design Center.²¹ A modified R-S code for a SSR has been performed by software as well.²²

Convolutional encoding differs from block coding by interleaving the overhead or check bits into the actual data stream rather than being grouped into words.²³ This provides good immunity for mitigating isolated burst noise, and is particularly useful in communication systems.

Mitigation may also be performed at the system level or with an overlying system protocol. Typical error detection schemes as described above may be used, and error correction may be accomplished by rewriting or re-transmitting data. A combination of EDAC techniques may be most effective.

The above methods provide ways of reducing the effective bit error rate (BER) of data storage areas such as solid-state recorders and communication paths or data interconnects. Table 4 summarizes sample EDAC methods for memory or data devices and systems.

Table 4. Sample EDAC Methods for Memory or Data Devices and Systems

EDAC Method	EDAC Capability
Parity	Single bit error detect
Hamming Code	Single bit correct, double bit detect
RS Code	Correct consecutive and multiple bytes in error
Convolutional encoding	Corrects isolated burst noise in a communication stream.
Overlying protocol	Specific to each system implementation

Control

The above techniques are useful for data SEUs, and may also be applicable to some types of control SEUs as well. Highly integrated devices such as VLSI circuitry or microprocessors leave the system potentially more vulnerable to hazards such as issuing an incorrect

command to a subsystem, or functionally interrupting system operations. Additionally, many newer devices, especially microprocessors, have hidden registers not accessible external to the device, which provide internal device control and may affect device or system operation. Microprocessor software tasks or subroutines dubbed Health and Safety (H&S) may provide some SEE mitigation [ref²⁴]; H&S tasks may include memory scrubbing with parity or other code methods on external devices, or on registers internal to the microprocessor. They also might use internal hardware timers to set watchdog timers (some type of message is sent indicating health of a device or system) or to pass H&S messages between spacecraft systems.

Redundancy between circuits, boxes, systems, etc. provides a potential means of recovery from an SEE on a system. Autonomous or ground-controlled switching from a prime system to a redundant spare may provide system designers an option, depending on spacecraft power and weight restrictions. Alternately, lockstep operation uses two identical circuits performing identical operations with synchronized clocking, a technique often used with microprocessors.²⁵ Errors are detected when the processor outputs do not agree, implying that a potential SEU has occurred. The system then has the option of reinitializing, etc. However, for longer spacecraft mission time frames, lockstep circuits using commercial devices may cause TID-induced problems; clock skew with increasing dosage may cause false triggers when the lockstep devices respond to the dosage differently. Voting takes lockstep systems one step further: with three identical circuits, choose the output that at least two agree upon. Katz, et al. provide an excellent example.²⁶ They have proposed and SEU-tested a triple modular redundancy (TMR) voting scheme for FPGAs. FPGAs provide higher gate counts and device logic densities than older LSI circuits; while this reduces the IC count for spacecraft electrical designs, with the TMR scheme you essentially lose over two-thirds of the available FPGA's gates.

Good engineering practices for spacecraft provide other means of mitigation.²⁷ Utilizing redundant command structures (two commands trigger an event with different data or addresses), signal power margins, etc. may aid an SEU hardening scheme. These and other good engineering practices usually allow designers to be innovative and discover sufficient methods for SEU mitigation as needed. Unknown device or system SEE characteristics provide the greatest risk to a system and conversely, the greatest challenge to an electrical designer.

SETs

Standard filtering techniques such as R-C filter circuits are effective means of reducing or eliminating SETs. Several things should be noted, however. First, SETs can be very application specific. For example, an analog comparator may have vastly different SET sensitivity in terms of transient shape and occurrence rates based on the circuit bias, power supply, etc... Second, adding filters can reduce the bandwidth of a circuit (i.e., the size of a valid pulse must be large enough to pass through the filter).

Destructive Issues

Destructive conditions may or may not be recoverable depending on the individual device. Hardening from the system level is difficult at best, and in most cases, not particularly effective, due to several concerns. First, non-recoverable destructive events such as SEGR or SEB require redundant devices or systems to be in place since the devices fail when this occurs. SEL may or may not have this same effect and is very device specific. Microlatch, in particular, is difficult to detect since the current consumption of this condition may be within that of normal device operation. LaBel has demonstrated the use of multiple watchdog timeout conditions as a potential mitigation scheme.²⁸ A similar concern exists if current limiting is performed on a card or higher integration level: a single device may see SEL at a high enough current to destroy itself, but not at a sufficient current to trigger the overcurrent protection on the card. Current limiting circuits to cycle power on individual devices are often considered, but failure modes of this protection circuit are sometimes worse than finding a less SEL-sensitive device (e.g., infinite loop of power cycling may occur). Hence, SEL should be treated by the designer on a case-by-case basis considering the device's SEL response, circuit design, and protection methods. A risky method of SEL protection on SEL-vulnerable devices involves reading the device's current periodically, and cycling power if the current exceeds a specified limit. This method can use either telemetry points or device calibration parameters to be successful.²⁹

Sample Methods of Improving Designs for SEE Performance

By changing circuit design or parameters, improved SEU performance may be gained. Marshall [ref³⁰] and LaBel [ref¹⁵] have demonstrated ways of improving a fiber optic link's BER from SEU by choice of diode material (III-V versus Si) resulting in a significantly smaller device sensitive volume, method of received signal detection (edge versus level sensitive) defining a

dynamic sensitive time window, and optical power margin (BER decreases with increased margin). These and similar techniques may apply to other designs as well.

Summary

We have presented an overview of the natural space radiation environment, its effects and how they relate to emerging technologies, and finally, a treatise on radiation risk reduction for electronics systems. The expectations are that as technologies evolve and emerge, new effects and concerns may be expected.

Acknowledgements

The authors would like to acknowledge the sponsor of this work, the NASA Electronics Radiation Characterization Project. We would also like to thank "Marvelous" Martha O'Bryan for her support in developing this paper.

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Radiation Effects on Emerging Technologies: Implications of Space Weather Risk Management

Kenneth A. LaBel, Janet L. Barth
NASA/GSFC

Presented by Kenneth A. LaBel American Institute of Aeronautics and Astronautics, September 26-29, 2000, Long Beach CA



Outline

- Introduction
- The Natural Space Radiation Hazard
- Basic Radiation Effects on Technology
- Sample Emerging Technologies*
- Managing the Radiation Risk
- Discussion
- Acknowledgements

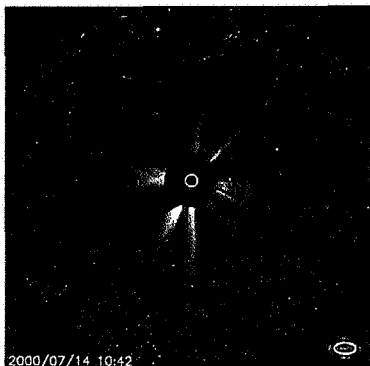
** Emphasis is on technologies applicable to electronic systems*

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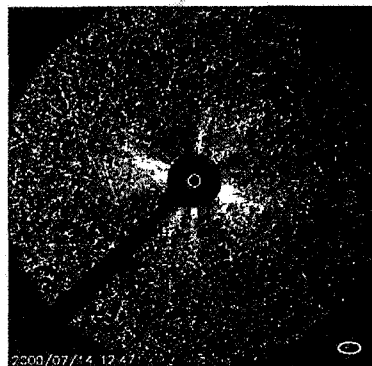
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SOHO/LASCO Images



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3



Spacecraft Design Reality

Design Considerations:

- Reduced Weight
- Reduced Power Consumption
- Increased Performance Requirements
- Increasingly Complex Sensor Arrays
- Decreased Availability of Rad-hard Devices

Programmatic Considerations:

- Reduced Cost
- Use of Flight Heritage Designs
- Mass-Buy Procurement
- Decreased Procurement Lead Times
- Overlapping Development Schedules
- Reduced Manpower

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4



Desirable Electronics Features for Future NASA Missions

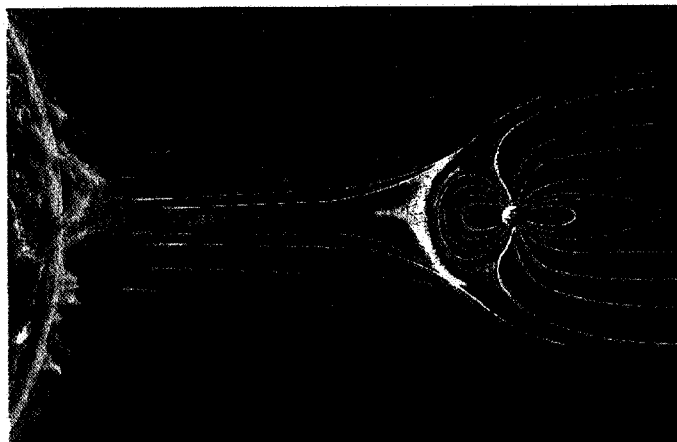
- Higher functional integration/density
 - System-on-a-chip
- Modular system design
- Advanced packaging techniques
- Low and ultra-low power
- Fault tolerant
- Reconfigurable systems
- Rapid prototyping/simulation
- Scalable real-time multiprocessing
- Operation at cold temperature
- High-bandwidth communications and free space interconnects
- Increased processing capability
 - On-board autonomy, data reduction
- Increased reliability
- Integrated power management and distribution
- Radiation tolerance
- Availability, cost, ...

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Space Radiation Environment

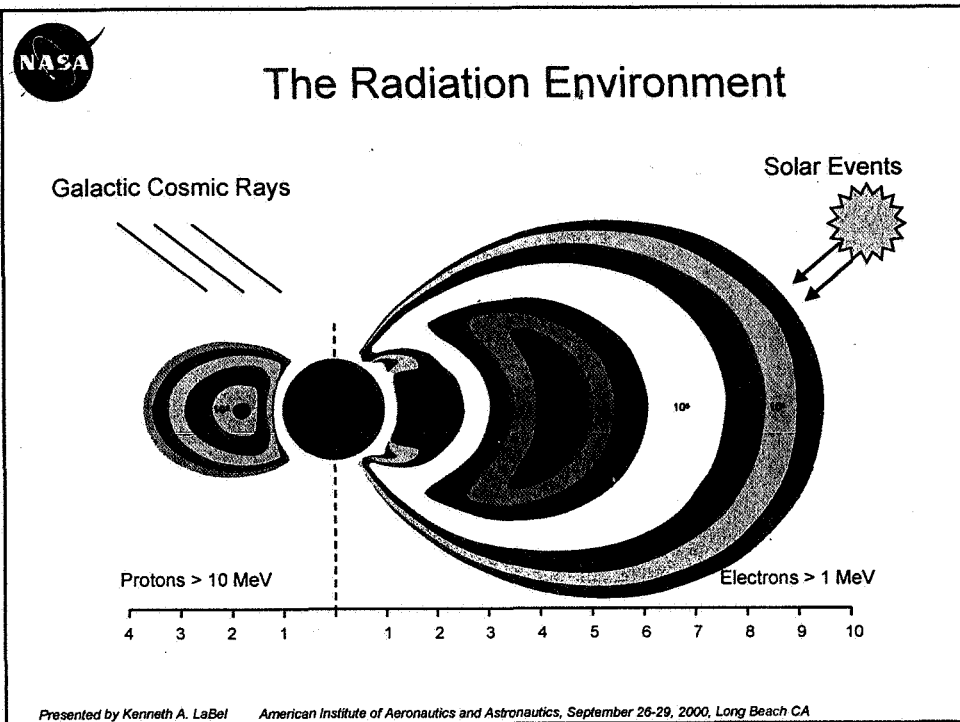



Nikkei Science, Inc. of Japan, by K. Endo

Janet Barth http://radhome.gsfc.nasa.gov/radhome/papers/apl_922.pdf

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Radiation Effects and Spacecraft

- Three areas are critical for design in the natural space radiation environment
 - Long-term effects
 - Total ionizing dose (TID)
 - Displacement damage dose (DDD)
 - Transient or single particle effects (Single event effects or SEE)
 - Soft or hard errors
- Mission requirements and philosophies vary to ensure mission performance
 - What works for a shuttle mission may not apply to a deep-space mission

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Basic Radiation Effects on Devices: Long-term Effects

- TID
 - long-term degradation due to cumulative ionizing dose deposited in a device
 - effects may include:
 - parametric changes/failures
 - increase in leakage current
 - threshold voltage shifts
 - functional failures, etc...
- DDD
 - may have similar effects as TID, but caused by non-ionizing effects

Note: TID hardness does not necessarily imply DDD hardness

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Basic Radiation Effects on Devices: Transient Effects

- SEE
 - event caused by a single ion strike depositing sufficient energy in a device to cause an effect
 - two basic categories:
 - soft errors which include: Upset (SEUs), Transients (SETs) and Functional Interrupts (SEFI)
 - examples: bit flip in a memory cell, a change of state in a program counter, a change of configuration in a RAM-based FPGA
 - hard errors which include: Hard errors (SHE), Gate Rupture (SEGR), Burnout (SEB), Dielectric Rupture (SEDR), and Latchup (SEL)

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Radiation Effects and the Hazard

- Total Ionizing Dose
 - Trapped Protons & Electrons
 - Solar Protons
- Single Event Effects
 - Protons
 - Trapped
 - Solar
 - Heavier Ions
 - Galactic Cosmic Rays
 - Solar Events
 - Neutrons
- Displacement Damage Dose
 - Protons
 - Electrons
 - Neutrons

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Microelectronics

- Trend: increased performance (re: higher speed and lower power) and/or device integration.
- Microelectronics encompasses multiple technologies including:
 - Silicon
 - Compound Semiconductor
- Rank of the available technologies by their speed performance capabilities:
 - Si, overlapped at its upper range by SiGe,
 - SiGe overlapped at its upper range by GaAs,
 - GaAs overlapped at its upper range by InP

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Radiation Issues for Newer Technologies

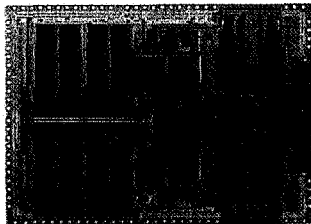
- Proton induced single event upsets
- Proton induced single event latchup
- Neutron & Alpha induced upsets
- Single events in Dynamic RAMs
- Displacement damage in electronics
- Single event functional interrupt
- Stuck bits
- Block errors in Dynamic RAMs
- Single event transients
- Neutron induced single event effects
- Hard failures & latchup conditions
- Multiple upsets from a single particle
- Feature size versus particle track
- Microdose
- Enhanced low dose rate
- Reduced shielding
- Test methods for advanced packaged devices
- Ultra-high speed & novel devices (e.g., photonics, InP lcs)
- Design margins & mitigation
- COTS variability
- At-speed testing
- Application-specific sensitivities

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Ultra-Low Power (ULP) Technology Microelectronics



1024-point
FFT processor



20bit x 20bit
Pipelined Multiplier

Prime Driver:

Hand-held products that require:
High levels of integration, and
very low power consumption

Advantages:

Reduced power consumption with VCC <1V
Allows for enabling volume shrinkage for
space application

May:

Provide true "nanosat" technology

Applications:

Mostly digital at this time

Radiation Issues:

Upset sensitivity
Rad-tolerant effort at University of New Mexico

Comment:

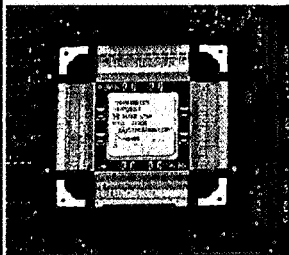
Other reliability issue such as ultra-thin
silicon dioxide gate dielectrics
Electromigration issues with minimum pitch
interconnect

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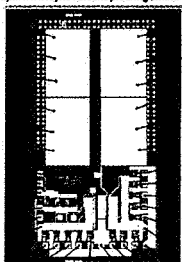


SOI Technology



Mongoose V

<http://www.synova.com/procmg5.html>



ASP1150 1/2 AMP SOLENOID DRIVER

<http://www.micsemi.com/html/asp1150.html>

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Prime Driver:

Hand-held products that require:
High levels of integration, and
very low power consumption

Advantages:

Reduced power consumption
Low noise
Performance improvements

May:

Provide commercial solution to soft error
sensitivity at reduced power supply voltages

Applications:

Digital, analog, mixed signal

Sample devices:

Mongoose V processor
256 kbit SRAM
• 1.2V operation comparable to >2V bulk device

Radiation Issues:

Robust to SEE
TID varies

Comment:

Issues of yield/production



GaAs Semiconductors



Representative cross section of a GaAs-based microbeam accelerometer. The approach combines piezoelectric thin films with micromachined structures on a GaAs substrate with MESFET electronics.

http://www.topvu.com/html/technical_information.html



32 Bit C/GaAs Adder

<http://www.personal.engr.umich.edu/~phiroze/32bitAdder.html>

Driver:

Cellular telephones and wireless communications

Advantages:

High operational speed and linearity
Ability to operate at reduced power supply voltages

Current trends:

Higher integration
Reduced substrate costs

May:

Be ideal for multi-frequency (re: dual-band) phones

Applications:

Analog, digital, or mixed signal

Radiation Issues:

SEU sensitivity

Comments:

Emergence of Complementary GaAs (CGaAs) or other
more SEU-tolerant technologies (LT buffers)
• increased density and reduced power consumption
traded with operating speed (<1GHz)

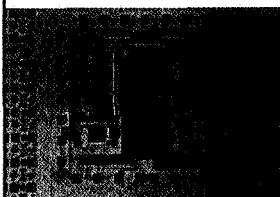
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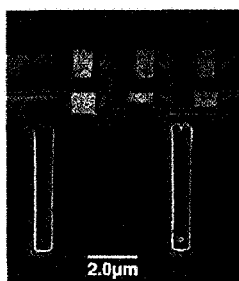
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SiGe Semiconductors



SiGe IC



SiGe SEM
Cross-Section

Driver:

Handheld products

Advantages:

Higher Speed than Si (>40 GHz possible)
Compatible with existing Si technology
Low noise floor and high power gain imply
mixed-signal (cellular phone-on-a-chip) potential
May be "tuned" by selective doping

May:

Compete with III-V semiconductors

Applications:

Digital, analog, mixed signal (cellular phone-on-a-chip)

Sample Device:

12-bit DAC with 1.2 Gbps operation
- outperforms comparable bipolar devices

Radiation Issues:

Preliminary TID and displacement damage results
look promising
SEU sensitivity demonstrated

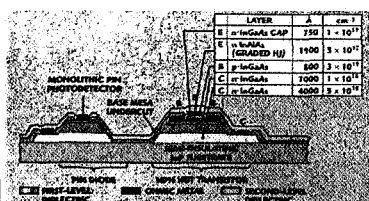
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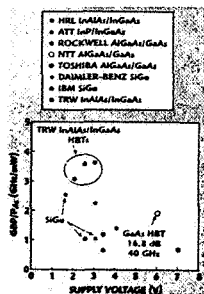
17



InP Semiconductors



A cross section of the InAlAs/InGaAs HBT Device.



A comparison of InP HBT direct-coupled amplifiers.

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Driver:

Mobile communications

Advantages:

Ultra-high Speed (>100 GHz)
Low phase noise
Excellent thermal conductivity
Compatibility with Si

May:

Provide an "ideal" space solution

Applications:

Digital, mixed signal primarily

Radiation Issues :

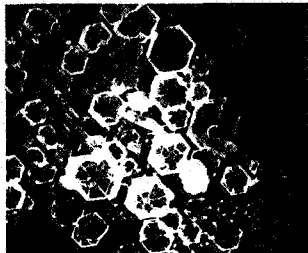
Preliminary results promising

Comments:

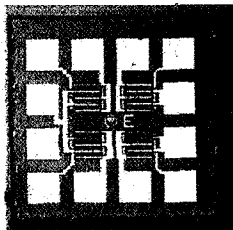
Still in prototype stage
Material quality and availability



Wide Bandgap (WBG) Semiconductors



GaN Bulk Crystal Growth



SiC IC

Sample Technologies:

SiC, GaN, Diamond, and AlN

Advantages:

High temperature and power density levels
High thermal conductance
High electron carrier velocities

May:

Replace some Si-based or high-frequency Vacuum tube technologies while reducing weight, power, and complexity

Applications:

MMICs for phased array radar power amplifier, cross-and down-link power amplifiers, power conversion products
novel packaging

Radiation Issues:

Open

Comment:

Materials fabrication issues
Material quality and availability

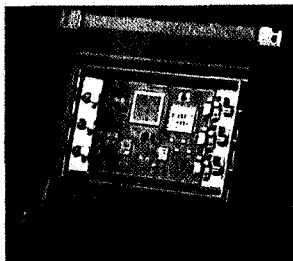
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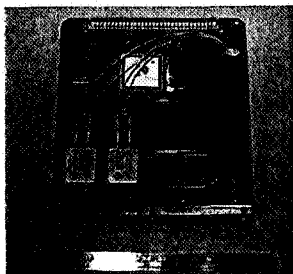
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Fiber Optic System Applications



FODB CFBIU MCM



Microelectronics and Photonics Test Bed

Prime Driver:

Terrestrial telephone and communication links

Advantages:

Reduced volume, weight
Increased performance (>1Gbps)
Reduced EMI/EMC
Architectural scalability

May:

Replace existing command and data interfaces

Applications:

Data and command transfer

Sample Developments:

PFODB, SFODB, commercial: FC, ethernet ...

Radiation Issues:

Design dependent
Associated electronics are often the radiation driver
Hardening approaches possible

Comment:

Many new technologies emerging
Several systems currently in space
Higher (ie: >1Gbps) rate systems sought
(image processing, optical processing, ...)

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Space Radiation Effects Issues for Fiber Links

- Issues include:
 - Darkening in passive optical components (fibers, lenses, etc.)
 - Choices may be made to minimize concerns such as the use of pure silica fiber and not using graded index (GRIN) lenses
 - Displacement damage
 - Primarily driven by proton fluences encountered and choice of technology (Si, GaAs)
 - Support electronics
 - May drive system tolerance to radiation effects
 - Single proton effects in receivers
 - Causes bit errors in data stream (i.e. increases, bit error rate or BER)
 - Mitigation of Single Proton Effects in Receivers
 - Choice of detector: III-V direct bandgap @ higher wavelengths vs. Si (or similar) indirect bandgap
 - Circuit hardening approaches
 - System level solutions

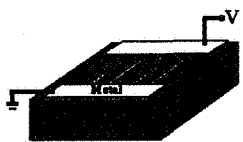
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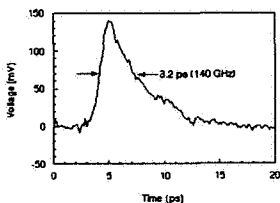
21



Metal Semiconductor Metal (MSM) Detectors



A metal-semiconductor-metal (MSM) photodetector



3.2 ps, 140 GHz MSM photodetector on silicon-on-insulator (SOI)

<http://www.tc.unn.edu/home/m017/nanolab/research/photodiode/photodiode.html>

Prime Driver:

Terrestrial communication (telephone, internet, ...)

Advantages:

High-speed photodiode with lower power consumption
Monolithic integration with FET possible
Available in multiple wavelengths

May:

Allow true monolithic receiver

Applications:

Commercial fiber links such as ethernet,
fibre channel (FC), ...
Hardened systems

Radiation Issues:

Preliminary results are encouraging

- TID tolerant
- Some SEU sensitivity

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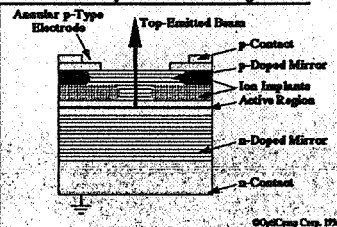
22



Vertical Cavity Surface Emitting Lasers (VCSELs)

Alternative to current edge-emitting lasers and LEDs

Vertical Cavity Surface-Emitting Laser



Advantages:

- Lower power consumption and reduced mass
- High aggregate throughput
- Integration (monolithic) with detectors and electronics

May:

- Provide a "fiber-less" system

Applications:

- Wavelength division multiplexing (WDM) for high throughput systems
- Smart pixel array (SPA) systems
- Commercial (terrestrial) data links (FC, ethernet, ...)

Sample Developments:

- HP VCSEL ethernet
- Honeywell's DARPA system

Radiation Issues:

- Preliminary data available (looks promising)

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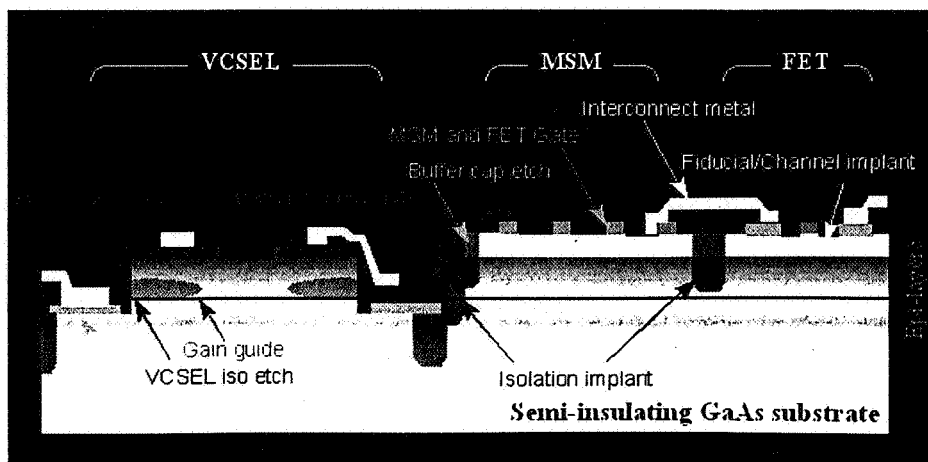
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VCSELs and MSMs Integrated on a Single Substrate

Schematic Cross Section of the Integrated Device Structures



Trend is to form a true monolithic optoelectronic IC (OEIC)

<http://co-op.gmu.edu/vcsl/oechip.html>

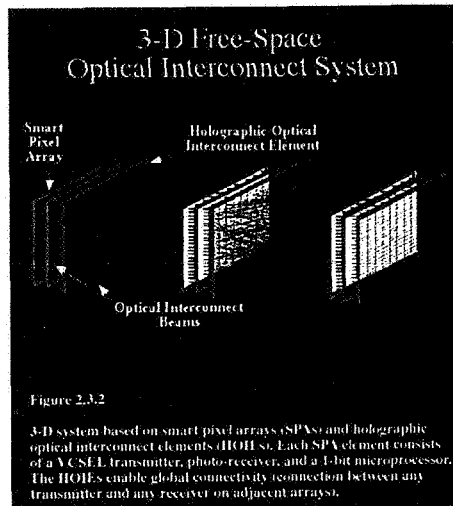
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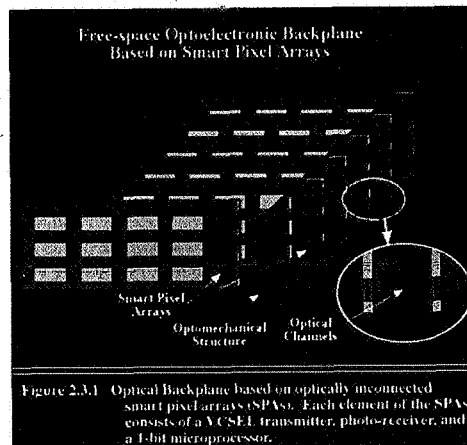
Applications of VCSEL-based Smart Pixel Arrays



<http://www-ocs.colorado.edu/~bertonsf/research.html>

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Radiation Risk Management: Levels of Hardening

- Transistor/IC*
- Circuit design/board*
- Subsystem and system
- Satellite systems (constellations)

****Emphasized in this talk***

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IC Hardening (1)

- Implies building an IC that meets system radiation requirements (call this a rad-hard or RH device)
- Features may include:
 - TID hardness or SEL immune process
 - Hardened transistors
 - Internal redundancy/voting
 - Internal error correction, etc.



IC Hardening (2)

- Advantages
 - Simplifies system design to meet radiation requirements
- Challenges
 - Performance, Cost, Schedule
- Examples
 - Hardened process
 - Compiled or hardened library design



Circuit Hardening (1)

- Implies adding radiation mitigation external to an IC
 - Shielding
 - RC filter
 - Voting logic
 - Error detection and correction (EDAC) codes
 - Watchdog timers, etc.
- Maybe be implemented or controlled by either hardware, software, or firmware

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Circuit Hardening (2)

- Advantages
 - Allows use of higher (non-radiation) performance ICs
 - Faster processors
 - Denser memories, etc...
- Challenges
 - Adds complexity (cost and schedule?) to design
 - Cost and schedule
 - Often difficult to retrofit
 - Modification to flight hardware

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Digression: Evaluating Your Internal Radiation Requirement

- The radiation hazard **INSIDE** the spacecraft may be vastly different than that **OUTSIDE** the spacecraft
- A 3-D ray trace is recommended to determine the *effective* shielding surrounding a component
- May help mitigate some TID/DDD issues (SEEs are not effectively shielded)
 - Placement of boxes closer together
 - Movement of sensitive component to center of spacecraft or box
- Note: composite structures offer less shielding when compared to old-style aluminum

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Mitigation of SEEs - SEUs

- Three types of SEUs
 - Data (Ex., bit-flip to a memory cell or error on a communication link)
 - Control (Ex., bit-flip to a control register)
 - Transient (*see paper for details)
- Some overlap: Ex., RAM with program memory stored inside

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Data SEUs - Sample Error Detection and Correction (EDAC) Methods

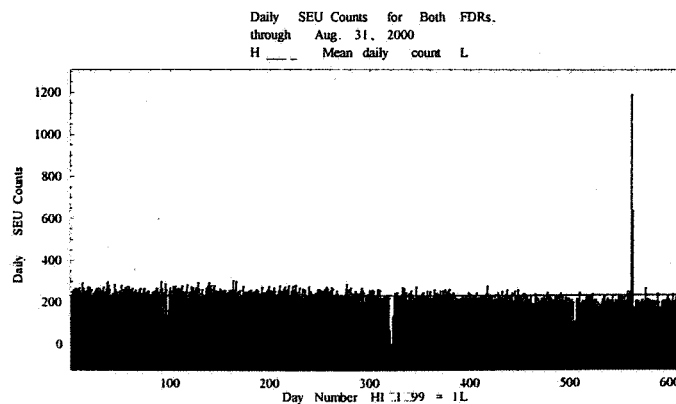
EDAC Method	EDAC Capability
Parity	Single bit error detect
Cyclic Redundancy Check (CRC)	Detects if any errors have occurred in a given structure
Hamming Code	Single bit correct, double bit detect
Reed-Solomon Code	Corrects multiple and consecutive bytes in error
Convolutional Code	Corrects isolated burst noise in a communication stream
Overlying Protocol	Specific to each system. Example: retransmission protocol

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SeaStar Flight Data Recorders (FDRs) SEU Counts



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Control SEUs - Sample EDAC Schemes

- Software-based health and safety (H&S) tasks
- Watchdog timers
- Redundancy
- Lockstep
- Voting
- IC Design techniques
- "Good engineering practices"
- Improved Designs

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Destructive Conditions - Mitigation

- Recommendation 1: Do not use devices that exhibit destructive conditions
- Difficulties:
 - May require redundant components/systems
 - Conditions such as microlatch difficult to detect
- Mitigation methods
 - Current limiting
 - Current limiting w/ autonomous reset
 - Calibration of device
- **MANY DESTRUCTIVE CONDITIONS MAY NOT BE MITIGATED**

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